Monolithic Transformers and Their Application in a Differential CMOS RF Low-Noise Amplifier

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***Abstract*—A 900 MHz low-noise amplifier (LNA) utilizing three monolithic transformers to implement on-chip tuning networks and requiring no external components has been integrated in 2.88 mm^2 in a standard digital 0.6 μm CMOS process. A bias current reuse technique is employed to reduce power dissipation, and process-, voltage-, and temperature-tracking biasing techniques are used. At 900 MHz, the LNA dissipates 18 mW from a single 3 V power supply and provides 4.1 dB noise figure, 12.3 dB power gain, -33.0 dB reverse isolation, and an input 1-dB compression level of -16 dBm. Analysis and modeling considerations for silicon-based monolithic transformers are presented, and it is shown that a monolithic transformer occupies less die area and provides a higher quality factor than two independent inductors with the same effective inductance in differential applications.**

I. Introduction

FINE-LINE CMOS technology easily provides high frequency active devices for use in RF applications (e.g., 800 MHz–2.4 GHz), but high quality passive components (e.g., inductors) present serious challenges to integration as exemplified by several recently reported CMOS RF low-noise amplifier (LNA) designs [1]–[4]. Although significant progress toward the integration of high quality inductors including many innovative structures and design techniques has been reported [5]–[9], practical planar monolithic inductors have achieved only moderate performance owing to resistive losses in the metal traces and in the underlying substrate.

Monolithic spiral transformers have been used in monolithic microwave integrated circuit and silicon radio-frequency integrated circuit designs to perform impedance matching, signal coupling, phase splitting, etc. Specific applications include low-loss feedback and single-ended-to-differential signal conversion in a 1.9 GHz receiver front end [10], and matching and coupling in an image rejection mixer [11] and in balanced amplifiers [12], [13].

In this paper, we describe a fully differential CMOS 900 MHz LNA that utilizes monolithic transformers [14]. The design is motivated by the fact that an on-chip spiral transformer comprising two coupled inductors occupies less area and exhibits a higher quality factor than two independent inductors with the same effective inductance in differential circuits. Section II overviews a modeling approach for integrated transformers, and Section III draws comparisons between various on-chip transformers and inductors. Section IV details the 0.6 μm CMOS LNA design which features three on-chip transformer tuning networks, bias current reuse to minimize power dissipation, and process-, voltage-, and temperature-tracking biasing circuits to minimize performance variations. Experimental results and conclusions are presented in Sections V and VI, respectively.

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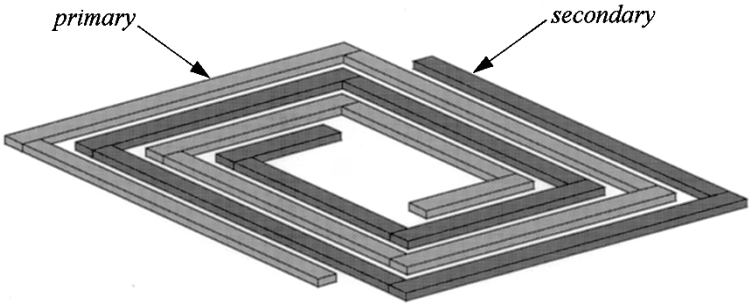
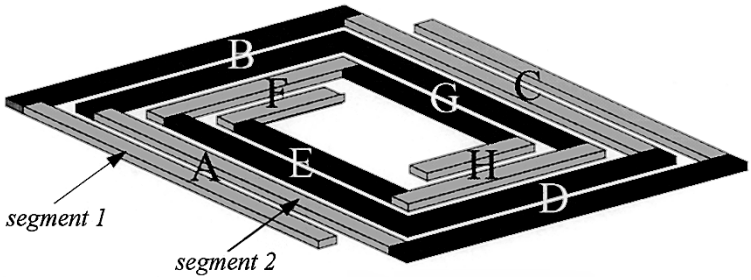
II. Monolithic Transformer Modeling

A monolithic transformer can be realized either by tapping into a series of turns of coupled microstrip lines or by interwinding two identical spiral inductors. The tapped transformer topology has been analyzed and modeled by Boulouard and Rouzic [15] and an improved layout has been proposed by Selmi and Ricco [13]. The tapped structure can provide an arbitrary turns ratio, but it is not perfectly symmetrical for the $1:1$ turns ratio case. Since the transformer is proposed as a substitute for two identical inductors in fully differential designs, the interwound structure of Fig. 1(a) is chosen due to the inherent symmetry.

One approach to transformer modeling follows the inductor modeling approach of Long and Copeland [6]. First, the primary and the secondary windings are partitioned into pairs of coupled microstrip line segments as illustrated in Fig. 1(b), and then the lumped-element circuit model of Fig. 1(c) is substituted for each pair; essentially it is a combination of inductor π models for each of the two segments plus coupling components between them. L_1 and L_2 and mutual coupling coefficient k can be computed using the three-dimensional inductance extraction program, *FastHenry* [16]. L_1 and L_2 include mutual coupling effects from all other parallel microstrip segments; coupling from perpendicular segments is ignored. Frequency-dependent R_1 and R_2, also computed using *FastHenry*, represent the metal trace resistances including the skin effect plus the loss resistances due to induced eddy current flow in the substrate. Eddy current losses are proportional to the substrate conductivity and the square of frequency; e.g., for a substrate resistivity of 0.1 Ω-cm, the loss resistance is about 0.4 Ω/mm at 900 MHz [17]. The oxide capacitances C_{oxi} and interline coupling capacitances C_c are estimated using the closed-form expressions in [18]. R_{si1} and R_{si2} account for resistive losses due to transverse



(a)



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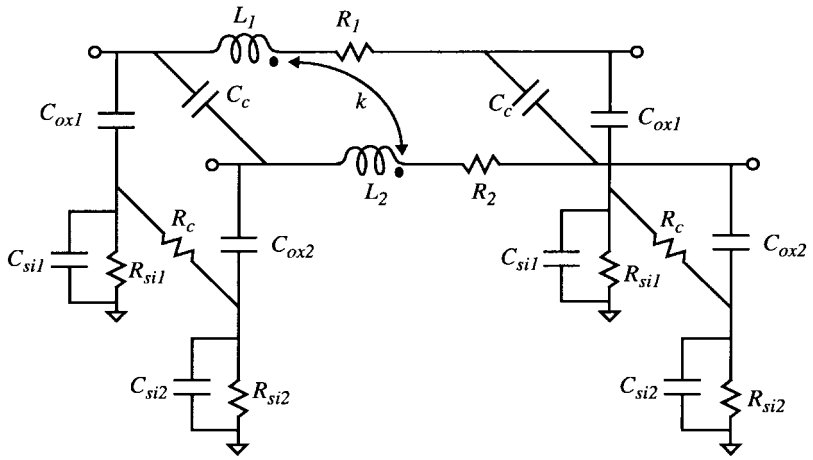
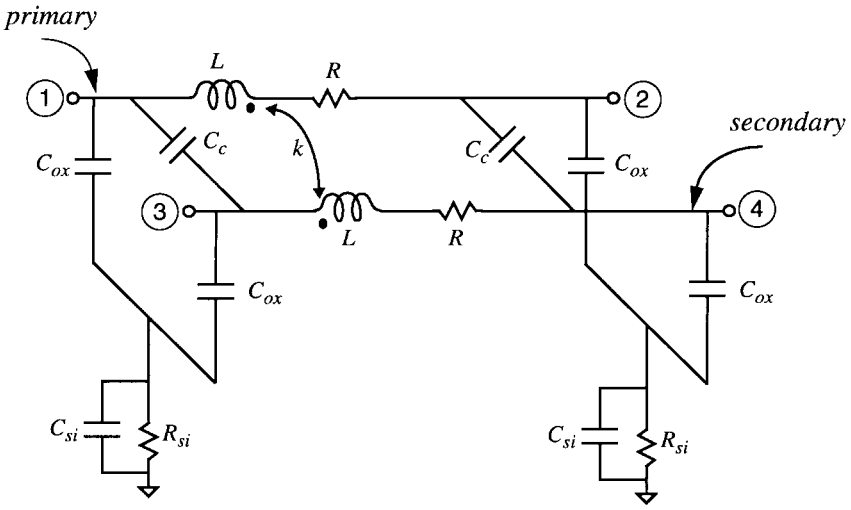


(c)



(d)

Fig. 1. (a) A transformer layout comprising two identical spiral inductors and (b) partitioned into eight parts of coupled microstrip line segments. (c) A lumped-element circuit model for one pair of coupled microstrip line segments. Eight such circuits are connected in series to model the complete transformer of (b). (d) An alternative compact circuit model for the transformer.

current flow in the lightly doped epitaxial layer. Assuming an epitaxial resistivity of 10 Ω-cm and a thickness of 7 μm, R_{si} can be estimated using the closed-form expressions in [17]. Knowing R_{si}, the shunt capacitance C_{si} of the epitaxial layer can be determined from the relationship $R_{si}C_{si} = \epsilon_o\epsilon_r\rho_{ep}$ derived from Maxwell's equations, where ρ_{ep} is the resistivity of the epitaxial layer. Note that for a ρ_{ep} of 10 Ω-cm, the time constant $R_{si}C_{si}$ is about 10 ps, indicating a cut-off frequency (at which C_{si} has the same impedance as R_{si}) of about 15 GHz. Therefore, C_{si} can be ignored for typical RF frequencies, and the heavily doped substrate can be treated as a single node to simplify the circuit model [19]. R_c represents the resistive coupling in the substrate between two microstrip lines which is usually negligible because the spacing between them is typically much smaller than their widths and lengths. Hence, R_c is treated as a short resulting in a further simplification of the lumped-element circuit model.

A series connection of lumped-element circuit models for each pair of coupled microstrip line segments [eight for Fig. 1(b)] models any interwound transformer structure. The complexity of the resulting model makes it well-suited to SPICE simulations. To facilitate analysis of and insight into transformer performance, however, a simpler model is desired comprising only one lumped-element model for the complete transformer. The element values of the compact model of Fig. 1(d) are chosen to provide a good fit between the impedance characteristics of the compact and complete models. As suggested in Fig. 1(d), the compact circuit model is symmetrical because the primary and the secondary spirals are identical. As a practical matter, the outer microstrip lines usually have larger oxide capacitance than the inner ones due to fringing effects, but we choose equal shunt parasitics to simplify the analysis.

Having established the compact circuit model of Fig. 1(d), we now derive the quality factor Q_l and self-resonant frequency ω_r for the primary (or secondary) winding. Since we intend to use the transformer as two identical inductors in differential circuits, only the differential-mode case will be considered. If equal and opposite currents flow through the transformer windings as in a fully differential circuit, then the effective inductance of the primary and secondary coils is increased to $L_{\text{eff}} = (1+k)L$. The quality factor Q_l of the primary (or secondary) is easily computed as

$$Q_l = \frac{\omega(1+k)L(1-(\omega/\omega_r)^2)}{R}\left(1-\frac{R^2C_{ox}}{(1+k)L}\right) \quad (1)$$

where the self-resonant frequency ω_r is

$$\omega_r = \frac{1}{\sqrt{(1+k)LC_{ox}}}\left(1-\frac{R^2C_{ox}}{(1+k)L}\right)^{0.5} \quad (2)$$

and the primary (or secondary) is assumed to be grounded at one port. When used as a floating transformer, Q_l is increased because the self-resonant frequency ω_r is about 1.4× higher. Although the effect of interline coupling capacitance C_c is ignored in the above derivations, it can be included by replacing C_{ox} with $(C_{ox}+2C_c)$ in (1) and (2).

From (1) and (2), decreasing R and C_{ox} increases both the quality factor and self-resonant frequency. This confirms that lower metal resistivity, lower substrate conductivity, and thicker oxides are desired for high quality monolithic inductors and transformers.

TABLE I
NEWELL 0.6 μm CMOS PROCESS PARAMETERS

Parameter	Value
Metal 3 resistivity	0.042 Ω-μm
Metal 3 thickness	1.2 μm
Oxide thickness (Metal 3 to substrate)	4 μm
Epitaxial layer resistivity	10 Ω-cm
Epitaxial layer thickness	7 μm
Substrate resistivity	0.1 Ω-cm
Substrate thickness	250 μm
Oxide dielectric constant	3.9
Silicon dielectric constant	11.9

III. MONOLITHIC TRANSFORMERS VERSUS INDUCTORS

Various monolithic inductors and transformers, fabricated in a three-metal 0.6 μm digital CMOS technology for use in LNA designs, have been modeled to compare their performance. Only the topmost third-layer metallization is used to implement both the transformers and inductors because it provides the lowest metal resistance and oxide capacitance. Table I lists the process parameters used for the inductors and transformers. Note that the resistivity and thickness of the epitaxial layer and the substrate are estimated based on the available process information. All geometric layout parameters except the number of spiral turns are kept constant for each of the transformers and inductors; namely, the metal trace width is 30 μm, the metal trace spacing is 3 μm, and the spiral center spacing is 120 μm. The operating frequency is assumed to be 900 MHz.

Matlab simulation programs were written using closed-form expressions for the shunt parasitics C_{ox}, C_c, R_{si}, and C_{si} and the substrate resistive loss due to eddy current. *FastHenry* was used to compute the self-inductance, mutual coupling coefficient, and metal resistance including the skin effect. Table II summarizes the simulation results for two different inductors and transformers in differential mode. Note that electrical parameters are listed for the transformer primary winding only since the secondary winding is identical. In realizing an effective inductance, the transformer takes advantage of the mutual coupling between its windings, and as a consequence, it exhibits less series resistance and shunt capacitance and occupies less die area than two equivalent independent inductors. From another viewpoint, the transformer primary (or secondary) spiral requires a shorter metal trace length than an equivalent inductor. Hence, the parasitics are reduced and performance is increased—an advantage that widens as the required effective inductance increases. As summarized in Table II, the improvement with the transformer is 45% in quality factor and 12% in self-resonant frequency for an effective inductance of 9.17 nH.

TABLE II
SIMULATIONS OF TRANSFORMERS (PRIMARY) VERSUS INDUCTORS IN DIFFERENTIAL MODE

	effective inductance (nH)	R (Ω)	Cox (pF)	Cc (fF)	Rsi (Ω)	Csi (pF)	Q_l	fr (GHz)	trace length (mm)
transformer (primary)	1.41	2.11	0.20	35.3	27.0	0.39	3.7	8.65	1.43
	9.17	7.48	0.71	140.3	7.7	1.37	5.2	1.80	5.03
inductor	1.41	2.58	0.25	19.0	21.9	0.48	3.0	8.25	1.76
	9.17	9.39	0.89	82.2	6.2	1.71	3.5	1.61	6.26

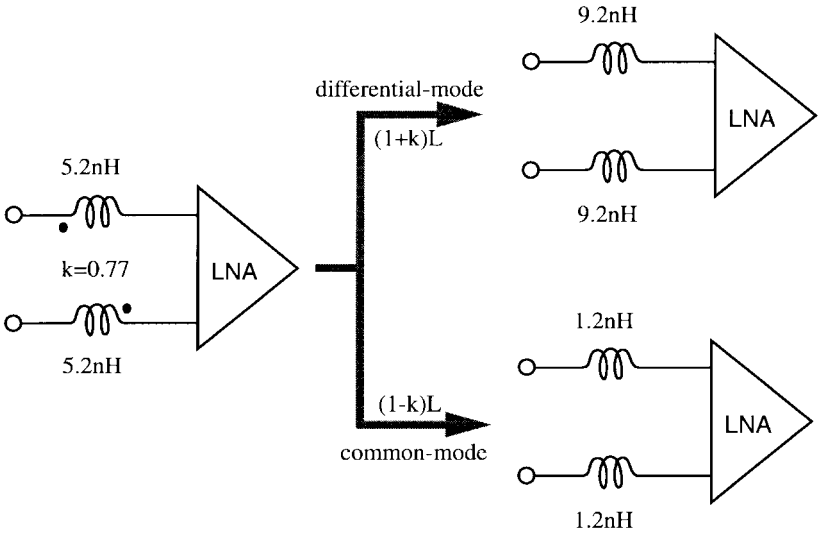


Fig. 2. Differential- and common-mode equivalent circuits for a spiral transformer used in a fully differential LNA circuit.

Another important advantage of a transformer is that it provides additional common-mode rejection in fully differential applications. As exemplified in Fig. 2, the transformer provides the required effective inductance of about 9 nH for an LC tuning network in differential mode, achieving higher quality factor and self-resonant frequency than two independent inductors. In common mode, however, the effective inductance of a transformer winding is decreased to $(1-k)L$ which is about only 1 nH. Hence, the common-mode network is effectively detuned at the frequency of interest which significantly reduces the common-mode gain of the circuit. Two independent inductors do not offer this advantage because their inductances remain constant in both modes. Moreover, because of the symmetric interwinding layout of the transformer, substrate noise coupling through parasitic oxide capacitances appears as a common-mode signal to the transformer which leads to higher substrate noise rejection.

IV. LNA CIRCUIT IMPLEMENTATION

Using the transformers described above, a 900 MHz fully differential LC tuned LNA has been implemented in a standard digital 0.6 μm CMOS process. The LNA must provide power gain (typically 10–20 dB) without over-driving the down-conversion circuits, and it must include a driver stage for the 50 Ω resistive load. Fig. 3 shows such a two-stage fully differential CMOS LNA. It comprises an input stage formed by transformer T1 and M1–M4, an interstage transformer T2, and an ac-coupled driver stage formed by M5–M6 and transformer T3; T3 provides a dc path to the supply and tunes out the output capacitance so that the LNA can drive an off-chip 50 Ω load. Inductances are required to form series resonant networks with the gate-source capacitances of input transistors M1 and M2 so that minimum noise figure can be achieved [3]. Transformer T1 provides the required inductances at the input gates, taking advantage of its higher quality factor and self-resonant frequency compared to independent inductors. Transistors M1–M4 form a cascode input stage which increases the reverse isolation of the LNA. The reverse signal path in the cascode stage contains the drain-source capacitance C_{ds} of M3 (or M4) and the gate-drain capacitance C_{gd} of M1 (or M2). Since C_{ds} is usually much smaller than C_{gd}, higher reverse isolation is achieved as compared to an input circuit without cascoded transistors in which the reverse signal path contains only C_{gd}. Another benefit of the cascode configuration is the reduced Miller effect on the input capacitance. In the cascode configuration, M1 (or M2) is a common-source (CS) stage which has a large current gain and a small voltage gain while M3 (or M4) is a common-gate (CG) stage which has unity current gain and a relatively large voltage gain. Assuming the total voltage gain of the input circuit is designed to be 20 dB, it is not difficult to show that the voltage gain of M1 (or M2) is approximately $-g_{m1}/g_{m3}$. Therefore, the input Miller capacitance is about $(1+g_{m1}/g_{m3})\,C_{gd1}$ or $2C_{gd1}$, compared to $11C_{gd1}$ if the input

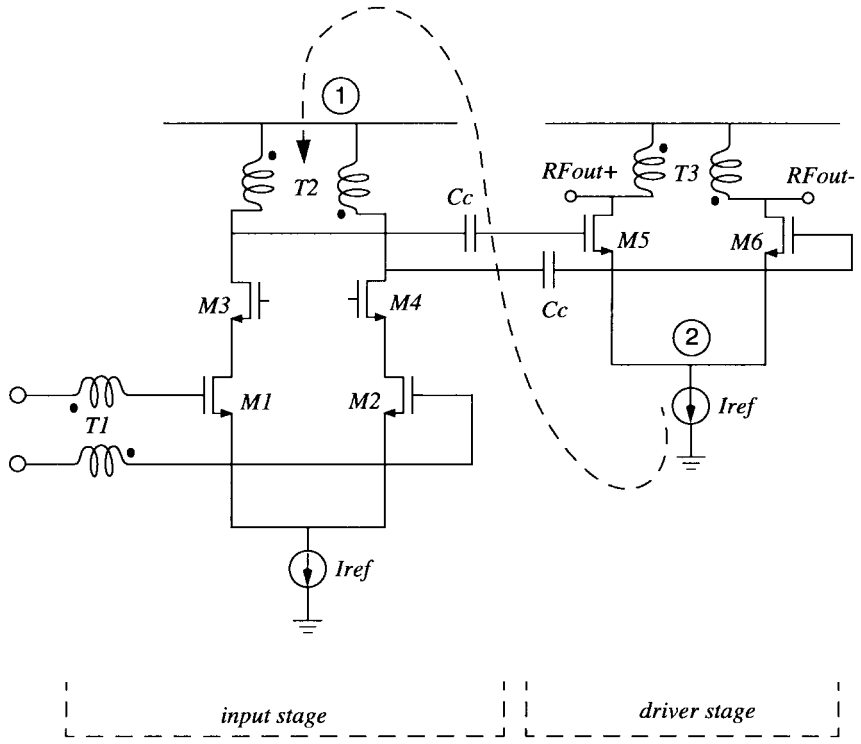


Fig. 3. Two-stage LC (transformer) tuned CMOS LNA.

circuit comprises only CS stage M1 (or M2). This is significant because Miller capacitance shunts the input RF signal and degrades circuit performance. The cascode device M3 (or M4) contributes additional noise to the circuit. However, since the impedance seen at the drain of M1 (or M2) is relatively high, about $1/g_{ds1}$ at low frequencies and $1/j\omega C_{gs3}$ at high frequencies, the channel thermal noise contribution from M3 (or M4) is small compared to that of M1 (or M2). In addition, the gate of M3 (or M4) is at ac ground and thus the induced gate current noise of M3 (or M4) is negligible.

An LNA usually dissipates a substantial amount of power in a receiving system because a large bias current is required to achieve low noise and high power gain. This not only increases the system cost but also causes excessive heat generation which reduces the effective g_m and increases the noise temperature. To reduce power consumption, a bias current reuse technique may be employed at a cost of reduced voltage headroom [20]. As can be seen from Fig. 3, both nodes 1 and 2 are ac grounds. By stacking the driver stage upon the input stage, the two stages share a single bias current I_{ref}, effectively reducing the total power consumption while still maintaining the large bias current needed for low noise and high power gain.

The complete circuit schematic of the CMOS LNA is shown in Fig. 4. The output driver is a PMOS source-follower pair M5–M6 (changed from the NMOS common-source pair shown in Fig. 3) with transformer T3. Though PMOS has lower g_m than NMOS with the same bias current, and a source-follower produces lower gain than a common-source amplifier, this implementation reduces circuit complexity by allowing dc coupling between the input and output stages. Thus, it eliminates the need for the on-chip coupling capacitors C_c shown in Fig. 3 which saves die area and avoids signal losses through the capacitive substrate parasitics of C_c. It also eliminates the need for a biasing circuit for M5 and M6. Interstage transformer T2 serves two purposes in the circuit: first, it forms the parallel resonant LC circuit with the gate capacitances of M5 and M6 and the drain capacitances of M3 and M4 to develop the necessary voltage gain for the LNA. Second, it acts as a high impedance for ac and a very low impedance for dc signals which makes the reuse of bias current feasible.

Each MOSFET has the minimum 0.6 μm drawn channel length. The widths of M1 and M2 are chosen to be 1080 μm. Although this value is larger than the optimum theoretical value, it removes the requirement for unrealistically large inductances in T1. The cascoding transistors M3 and M4 are designed with widths of 420 μm. Larger widths cause an increase in the noise contribution from M3 and M4 due to the increases in C_{gs3} and C_{gs4} which reduce the impedance seen at the drains of M1 and M2. However, smaller widths increase the voltage gains of M1 and M2 and thus the input Miller capacitances. M5–M7 are designed to have the same widths as M1 and M2. This choice is somewhat arbitrary but the large widths enable low voltage design. All three transformers are laid out on the topmost metal3 layer. Geometry parameters for the transformers were given in Section III, except for the center hole dimension of T2 and T3 which is 180 μm.

The drains of M5 and M6 are connected to one port of T2 which is at ac ground with a dc voltage of $V_{dd} - V_{sg}(\mathrm{M6})$. This dc potential provides the gate bias voltage for M1 and M2 through resistors R_{b1} and R_{b2}. R_{b1} and R_{b2} are chosen to be large enough (e.g., 40 kΩ) to block the incoming RF signal from being shunted to ac ground and to contribute negligible thermal noise current to the circuit. The circuit consisting of M22, M44, M66, and M7 is designed to track

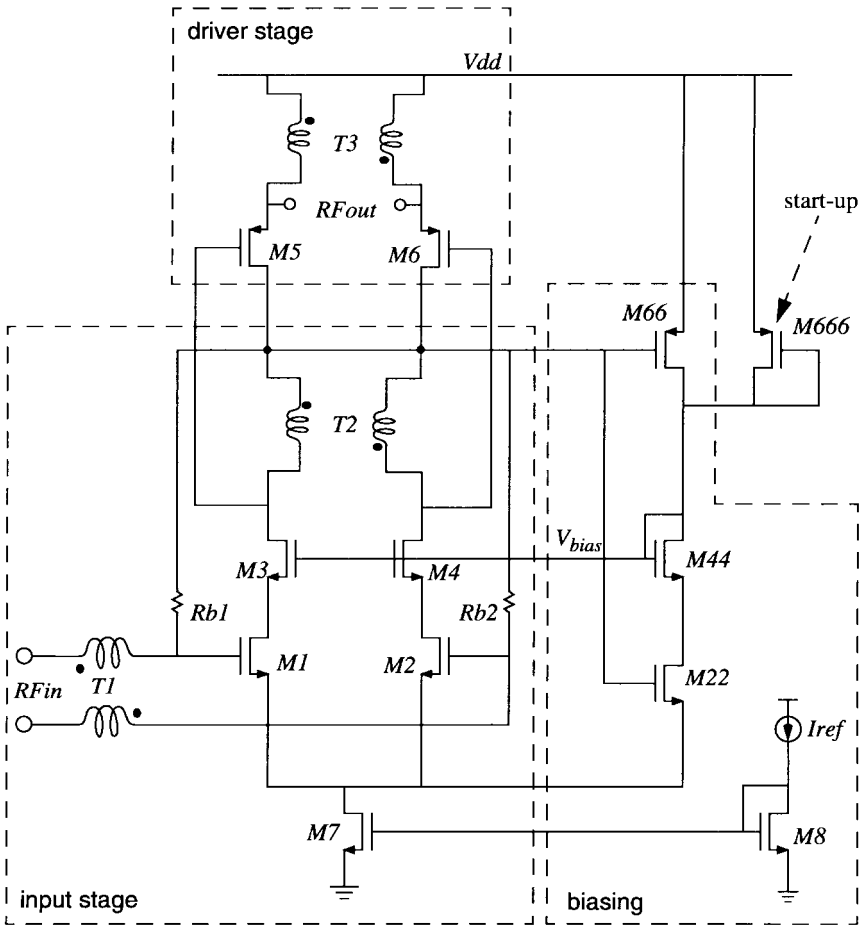


Fig. 4. Complete circuit schematic of the LC (transformer) tuned CMOS LNA in 0.6 μm CMOS.

process, voltage, and temperature variations in generating the bias voltage V_{bias} for M3 and M4. To accomplish this, we set $(W/L)_{66} = (W/L)_6/40$ and $(W/L)_{22} = (W/L)_2/40$. Note that $V_{sg}(\mathrm{M66}) = V_{sg}(\mathrm{M6})$ and $V_{gs}(\mathrm{M22}) = V_{gs}(\mathrm{M2})$. Therefore, the bias circuit consumes only 1/80 of the total bias current. Setting $(W/L)_{44} = (W/L)_4/40$, $V_{gs}(\mathrm{M44})$ and $V_{ds}(\mathrm{M22})$ are equal to $V_{gs}(\mathrm{M4})$ and $V_{ds}(\mathrm{M2})$, respectively. The voltage V_{bias} is then given by

$$\begin{aligned} V_{bias} &= V_{ds}(\mathrm{M7}) + V_{ds}(\mathrm{M22}) + V_{gs}(\mathrm{M44}) \\ &= V_{ds}(\mathrm{M7}) + V_{ds}(\mathrm{M2}) + V_{gs}(\mathrm{M4}) \end{aligned} \tag{3}$$

where

$$V_{ds}(\mathrm{M7}) = V_{dd} - V_{sg}(\mathrm{M6}) - V_{gs}(\mathrm{M2}). \tag{4}$$

It can be seen from (3) and (4) that V_{bias} tracks $V_{ds}(\mathrm{M7})$ and $V_{gs}(\mathrm{M4})$ with power supply and threshold voltage (process and temperature) variations. M666 is used to boost V_{bias} during start-up to guarantee reliable turn-on of the circuit, after which M666 is turned off.

Special precautions need to be taken in the layout of the CMOS LNA. The three transformers are separated as much as possible to minimize the interactions between them. Finger gate structures are used for the wide transistors M1–M7 (40 gate fingers for each device) to minimize noise contributed by the gate resistance [21]. To minimize substrate noise coupling into the RF circuits through the bonding pads, a grounded metal plate usually underlies the pad oxide to short the substrate noise to ground [22]. In our design, the input pads have N^+ diffusions below them which form a virtual ground so that substrate noise coupling into the pads appears as a common-mode signal to the differential LNA.

V. Experimental Results

Fig. 5 shows a chip micrograph of the 900 MHz LNA integrated in a standard digital 0.6 μm CMOS process. To exclude the effects of the package on performance, the tests were conducted with the die directly attached to a test board using pad-to-board wire bonding. External RF baluns were used at the input and output to perform single-ended/differential conversions.

The measured noise figure of the LNA is 4.1 dB at 900 MHz, higher than the 3 dB NF predicted by HSPICE. The discrepancy is partially explained by the fact that the measured resistivity of the metal3 layer was 50 mΩ/square (0.06 Ω-μm) which is 43% higher than the predicted process value listed in Table I. Consequently, the series resistance in the primary of T1 is 10.7 Ω as measured compared to 7.48 Ω as simulated. Using the higher resistance value, HSPICE predicts a NF of about 3.3 dB. Hot carrier and other short-channel effects are known to increase the channel thermal noise coefficient γ which may account for the remaining discrepancy of 0.8 dB. Other effects such as distributed substrate resistance and balun losses further degrade the NF. Of course, the simulated result

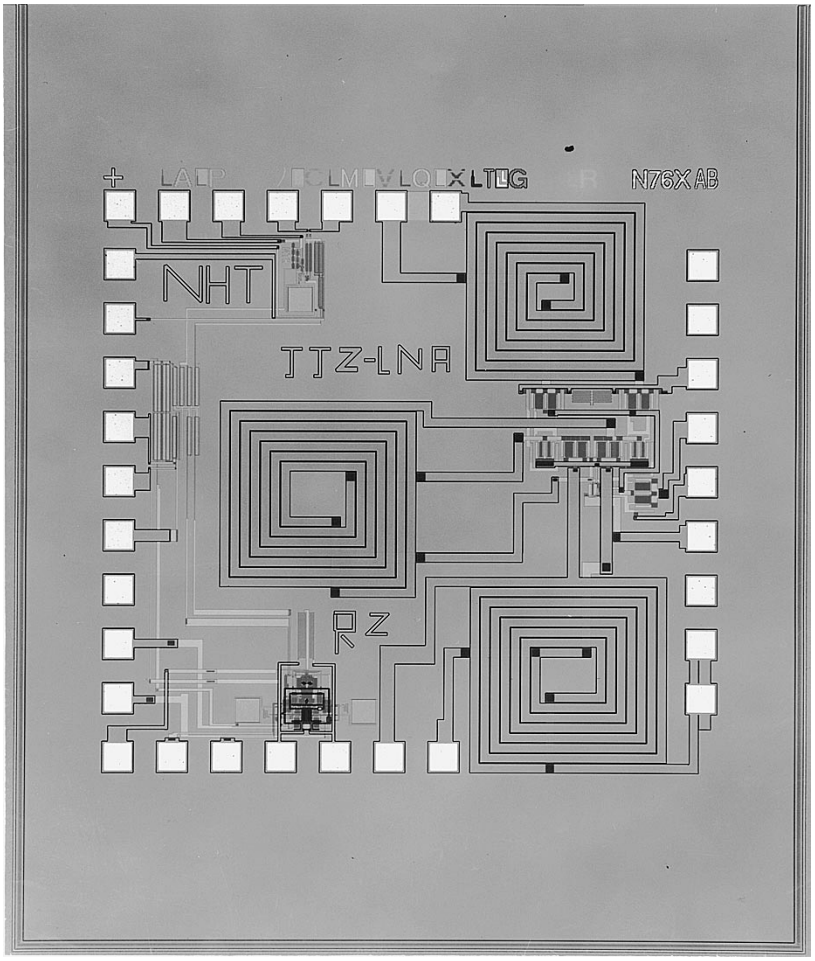
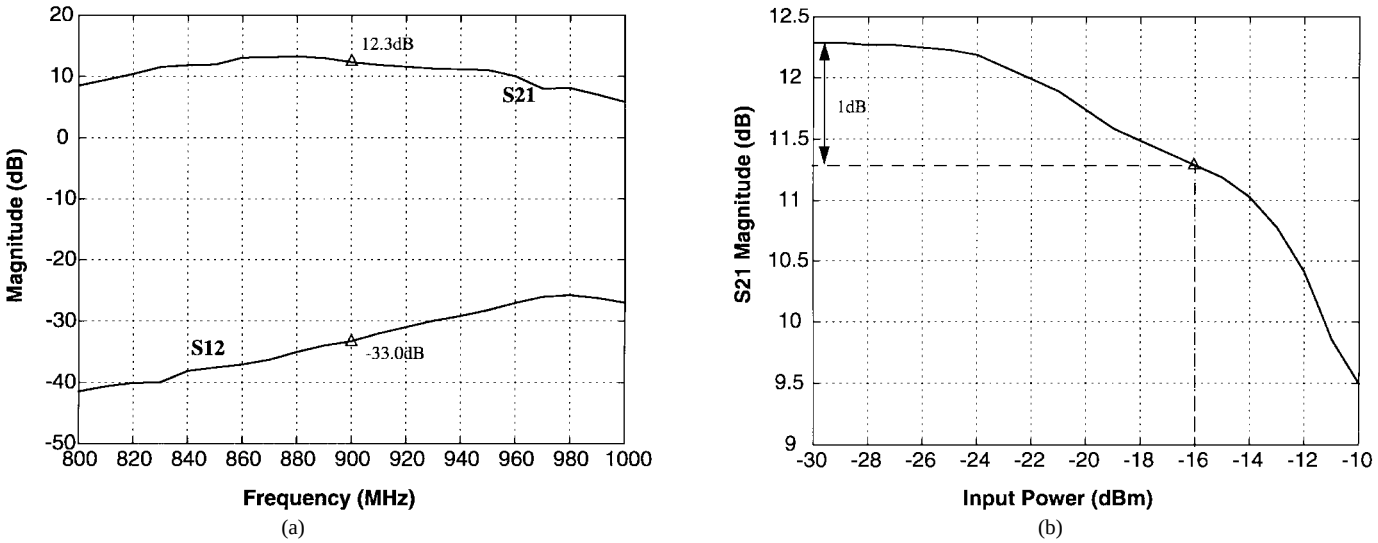


Fig. 5. LNA chip micrograph in 0.6 μm CMOS.



(a) (b)

Fig. 6. (a) S21 and S12 measurements and (b) 1-dB compression point measurements.

is expected to be optimistic since HSPICE does not include these effects. For example, with the series resistance set to the measured value of 10.7 Ω, the theoretical minimum NF of the CMOS LNA increases from 2.7 to 4.4 dB if γ increased from 2/3 to 2, or to 3.9 dB if γ increased from 2/3 to 1.5. A previous report gave experimental values for γ [23].

The measured forward power gain (S21) and reverse isolation (S12) of the LNA versus frequency are shown in Fig. 6(a); S21 is 12.3 dB at 900 MHz while S12 is −33.0 dB. The S21 curve clearly exhibits the expected bandpass characteristic with a peak value of 13.5 dB around 880 MHz. Fig. 6(b) shows the measured 1-dB compression point

TABLE III
MEASURED LNA PERFORMANCE

Supply voltage	3 V
Power dissipation	18 mW
Frequency	900 MHz
Noise figure	4.1 dB
S21	12.3 dB
S12	-33.0 dB
1dB compression (input)	-16 dBm
Technology	3-metal 0.6μm CMOS
Die area	2.88 mm^2

at 900 MHz which occurs at an input power level of -16 dBm.

The LNA dissipates 18 mW from a single 3 V supply. It occupies 2.88 mm^2 in a 3-metal 0.6 μm CMOS technology. About 90% of the die area is consumed by the three transformers. The experimental results for the LNA in a 50 Ω test environment are summarized in Table III.

VI. CONCLUSIONS

Full integration of CMOS low-noise amplifiers still presents a challenge for low-cost CMOS receiver systems. Silicon-based monolithic inductors are one bottleneck in RF CMOS design due to their poor quality factor. Analysis and modeling of silicon-based monolithic transformers was presented and it was shown that in fully differential applications, a transformer occupies less die area and achieves a higher quality factor and self-resonant frequency than two equivalent independent inductors. A fully integrated 900 MHz LNA in 0.6 μm CMOS, utilizing three monolithic transformers for input and output tuning, has been demonstrated. A bias current reuse technique was used to reduce power dissipation, and process-, voltage-, and temperature-tracking biasing techniques were employed. Experimental results show that at 900 MHz, the LNA dissipates 18 mW from a 3 V power supply and achieves a 4.1 dB noise figure, 12.3 dB power gain, and -33.0 dB reverse isolation with a 1-dB compression point at -16 dBm. No off-chip components are required. The higher performance of monolithic transformers may be exploited in other fully differential RF circuits such as bandpass filters, oscillators, etc.

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