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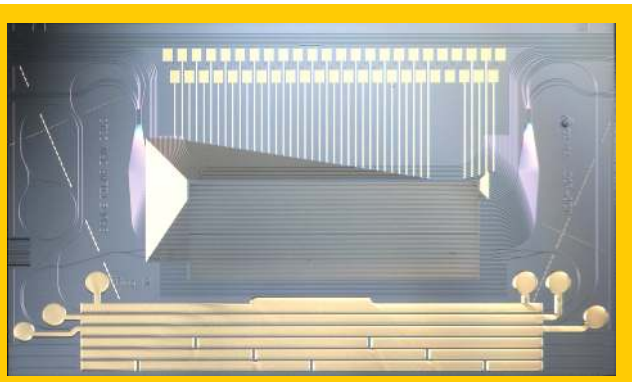
Abstract A review of the complexity development of InP-based Photonic ICs is given. Similarities and differences between photonic and microelectronic integration technology are discussed and a vision of the development of photonic integration in the coming decade is given.



Moore's law in photonics

Meint Smit[*], **Jos van der Tol, and Martin Hill**

1. Introduction

Since the early ninetees the complexity of InP-based chips has increased from a few to a few hundred components. The complexity development is reviewed in Sect. 2. Although it resembles the early development of microelectronics there are distinct differences which have prevented the success of microelectronics to be repeated in photonics. They are discussed in Sect. 3. A novel approach, which introduces the development model of micro-electronics in the photonic domain, is discussed in Sects. 4, 5, and 6. Of key importance is a highly standardized photonic integration technology. It is discussed in Sect. 4. The next step is to make this technology widely accessible via a foundry model, as described in Sect. 5. Section 6 describes the prospects of this novel approach. It will introduce the dynamics of microelectronics in the field of photonics, with every few years novel technology generations with ever more functionality. Section 7 discusses a next generation integration technology that will drive complexity levels significantly beyond the few hundred components that have been reported now. Section-VIII, finally, discusses the ultimates in photonic integration, with complexity levels approaching 1 million components per chip.

2. The development of photonic chip complexity

In microelectronics there is a clear exponential development in the number of transistors per chip, which has been doubling every two years on average during the last four decades. This phenomenon is known as Moore's law [1, 2]. In Photonics we observe a similar development, albeit in an early stage. Figure 1 and Table 1 show the complexity

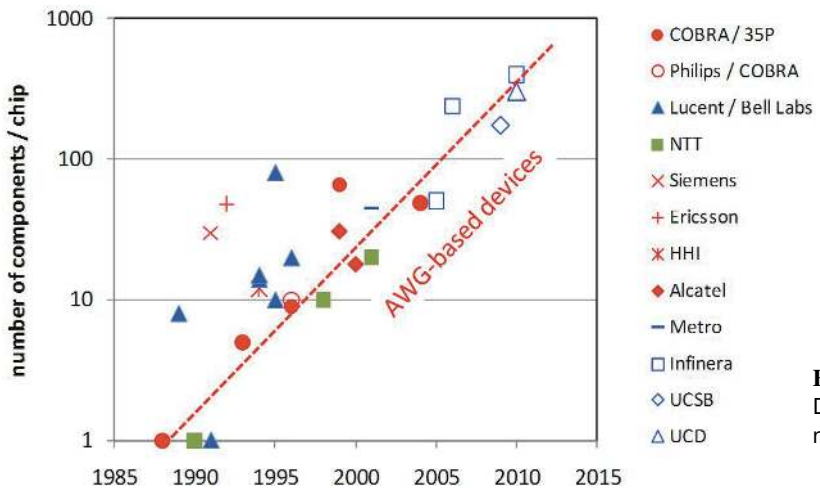


Figure 1 (online color at: www.lpr-journal.org) Development of chip complexity measured as the number of components per chip.

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Year	#comp	Short Title	1st Author	Institute	Ref.
1988	1	AWG	Smit	COBRA	[7]
1989	8	WDM source	Koren	Bell Labs	[3]
1990	1	AWG	Takahashi	NTT	[8]
1991	30	Grating Spectrograph	Cremer	Siemens	[4]
1991	1	AWG	Dragone	Bell Labs	[9]
1992	48	Switch Array	Gustavsson	Ericsson	[5]
1993	5	WDM receiver	Amersfoort	COBRA	[10]
1994	12	Heterodyne receiver	Kaiser	HHI	[6]
1994	14	WDM laser	Zirngibl	Bell Labs	[13]
1994	15	WDM channel selector	Zirngibl	Bell Labs	[16]
1995	10	WDM receiver	Zirngibl	Bell Labs	[11]
1995	81	WDM receiver and preamp	Chandrasekhar	Bell Labs	[22]
1996	9	WDM receiver	Steenbergen	COBRA	[12]
1996	20	WDM laser	Zirngibl	Lucent	[14]
1996	10	WDM laser	Staring	Philips	[15]
1998	10	WDM channel selector	Ishii	NTT	[17]
1999	66	WDM Crossconnect	Herben	COBRA	[21]
1999	31	WDM laser	Menezo	Alcatel	[18]
2000	18	WDM channel selector	Mestric	Alcatel	[19]
2001	20	WDM channel selector	Kikuchi	NTT	[20]
2003	45	WDM receiver	Tolstikhin	Metro	[23]
2004	49	WDM receiver	35 Photonics	35Photonics	[24]
2005	51	WDM transmitter	Nagarajan	Infinera	[25]
2006	240	WDM transmitter	Kato	Infinera	[26]
2009	177	Tunable WDM router	Nicholes	UCSB	[27]
2010	302	Arb. Waveform Generator	Soares	UCD	[28]
2010	400	PM-DQPSK WDM transm.	Corzine	Infinera	[29]

Table 1 Development of chip complexity measured as the number of components (#comp) per chip. The last column refers to the references listed at the end of this article.

development of InP-based Photonic ICs (PICs), measured as the number of components integrated on a single chip[1].

Early examples of complex InP-based PICs are a WDM source by Koren (1989) [3], a grating-based receiver by Cremer (1991) [4], a switch array by Gustavsson (1992) [5], and a heterodyne receiver by Kaiser (1994) [6]. The highest complexities so far have been reported in AWG-based PICs. It started with the publication of the first AWG by Smit [7] in 1988, followed by Takahashi (1990) [8] and Dragone (1991) [9]. After the invention of the AWG a number of AWG-based devices with increasing circuit complexity was reported: WDM receivers with 5–10 components by Amersfoort (1993) [10], Zirngibl (1995) [11] and Steenbergen (1996) [12]; WDM lasers with 10–20 components by Zirngibl (1994,1996) [13, 14] and Staring (1996) [15]; WDM channel selectors with 10–20 components by Zirngibl (1994) [16], Ishii (1998) [17], Menezo (1999) [18], Mestric (2000) [19] and Kikuchi (2001) [20] and a crossconnect chip with 66 components by Herben (1999) [21]. A special device is the WDM-receiver with integrated pre-amplifiers by Chandrasekhar (1995) [22] which counts 81 components, most of them electronic (transistors and resistors).

The new century brought a significant increase in complexity: WDM receiver and transmitter chips with 44–51 components by Tolstikhin (2003) [23], ThreeFivePhotonics (2004) [24] and Infinera (2005) [25]. Shortly after, in 2006, Infinera published a 40-channel WDM transmitter with 241 components [26]. Recent devices with a very high complexity are an all-optical tunable 8×8 wavelength router with more than 175 components by Nicholes [27] in 2009 and a 100-channel Arbitrary Waveform Generator with more than 300 components by Soares [28] in 2010. The latter device also contains 400 phase shifters for reducing the high crosstalk level in the very large AWG which is used to separate 100 wavelength channels. Recently, Infinera reported a PM-DQPSK transmitter with more than 400 components, the most complex PIC reported so far [29].

Figure 1 shows a more or less exponential increase in complexity, with a much larger scatter than its microelectronic counterpart. If we restrict ourselves to devices based on AWGs, with a more or less comparable technology (integrated amplifiers and/or detectors) most of the outliers disappear as can be seen in the "clean" photonic Moore's law shown in Fig. 5.

[1] Several metrics have been proposed for measuring chip complexity. We use a simple but coarse approach in which we count the number of basic components like AWGs, MMIs, SOAs, detectors and modulators. It does not count for the fact that a DFB laser is more complex than an MMI coupler, for example, so a higher number does not always mean a more complex chip. Further, we count only components that are essential for the PIC-functionality (e. g. no spare phase modulators that are not used).

3. Differences between photonics and microelectronics

There is an important difference, however, between the well known Moore's law graph [2] and the graph shown in Fig. 1. The microelectronics graph lists the complexity development of commercially applied ICs, whereas most of the points in Fig. 1 are about devices, which resulted in one or more papers but did not bring a circuit to the market. Only one of the reported devices, the chip of Infinera published in 2005 [25] is applied in a commercial product.

It is an interesting question why so few of the advanced PICs reported in the literature have made it to the market place, even though in the last two decades there has been substantial investment in the development of integration technologies in national and international projects in Europe, America and the Far East.

The problem with current project funding models is that they tie the technology development closely to an application: you get no money without a clear and challenging application. Usually the technology was fully optimized for that single application, and due to the absence of coordination, every fab developed its own processes. As a result we have almost as many technologies as applications, most of them very similar, but sufficiently different to prevent easy transfer of a design from one fab to another. Owing to this huge fragmentation, the market for these application-specific technologies is usually too small to justify their further development into a low-cost industrial volume manufacturing process. And as a result the chip costs remain too high to serve a large market.

This is quite different from micro-electronics where a huge market is served by a small set of integration technologies (most of them CMOS technologies). The solution to the problem in photonics seems obvious: apply the methodology that allowed microelectronics to change our world also to photonic integration. This requires two steps:

– Develop a few generic integration technologies that support realization of a broad range of functionalities.
– Develop a foundry infrastructure for providing low-cost open access to these generic technologies.

We will discuss them in the following paragraphs.

4. Generic photonic integration technology

In micro-electronics a broad range of functionalities is realised from a rather small set of basic building blocks, like transistors, diodes, resistors, capacitors and interconnection tracks. By connecting these building blocks in different numbers and topologies we can realize a huge variety of circuits and systems, with complexities ranging from a few hundred up to over a billion transistors.

In photonics we can do something similar. On inspection of the functionality of a variety of optical circuits we see that most of them consist of a rather small set of components: lasers, optical amplifiers, modulators, detectors and passive components like couplers, filters and (de)multiplexers. By proper design these components can be reduced to an even smaller set of basic building blocks.

As basic building blocks we need passive devices for combining and splitting of light, both wavelength dependent (filters, wavelength multiplexers) and wavelength independent (power splitters, couplers and combiners). Most of these devices can be composed of a combination of passive waveguides of different widths and lengths, so in a proper integration process that supports integration of passive waveguides a variety of passive devices, such as MMI couplers and AWG's can be realised. In addition to these passive devices we need basic building blocks for manipulating the phase, the amplitude and the polarization of the light signal, in order to support a broad range of functionalities.

Figure 2 illustrates some functionalities that can be realized in a generic Indium Phosphide technology that supports integration of four basic building blocks: passive waveguide devices, phase modulators, semiconductor optical amplifiers and polarisation converters. Most of the functionalities shown in Fig. 2 have been reported by us: compact MMI-couplers [30] and AWGs [31], optical switches [32] and modulators [33], multiwavelength and tunable lasers [34], flip-flops and ultrafast wavelength converters [35], picosecond pulse lasers [36] and polarization splitters and converters [37]. Figure 3 shows an example of an integrated discretely tunable laser with nanosecond switching speed [34], useful for packet switching applications, which has been developed in our experimental generic integration technology. The schematic on the left shows how the laser is composed

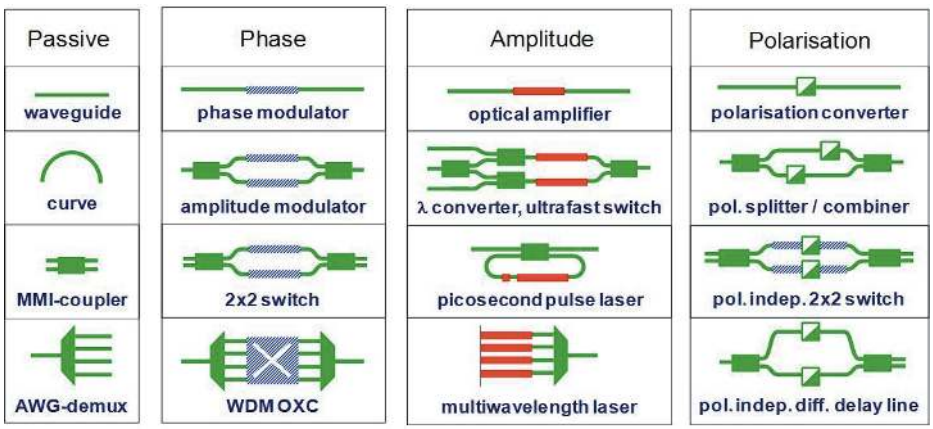

Figure 2 (online color at: www.lpr-journal.org) Example of the functionalities that can be realised in a generic integration technology that supports four basic building blocks: passive waveguide devices, (optical) phase modulators, semiconductor optical amplifiers and polarisation converters.

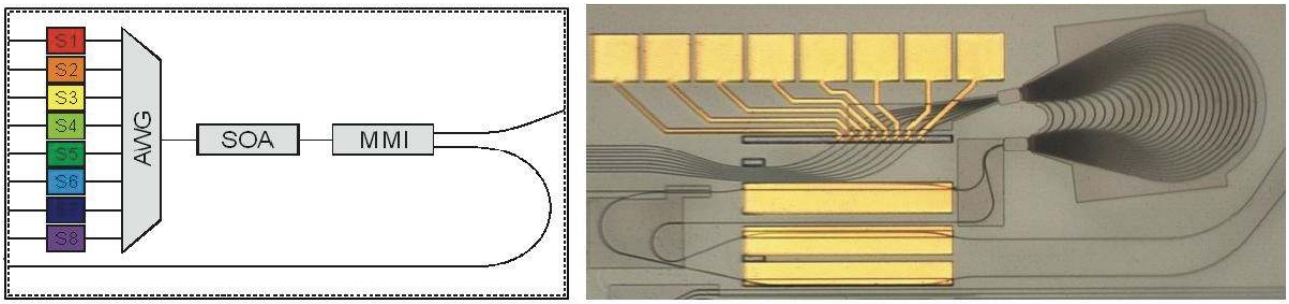

Figure 3 (online color at: www.lpr-journal.org) Circuit scheme and microscope photograph of an AWG-based fast tunable laser, which has been realised in the COBRA generic InP-based integration process. Chip dimensions are $1.5 \times 3.5\,mm^2$.

of only two basic building blocks: passive waveguides in the MMI-coupler, the AWG demultiplexer and interconnections, and Semiconductor Optical Amplifiers for amplification and switching.

An advantage of generic integration technologies is that, because they can serve a large market, they justify the investments in developing the technology for a very high performance at the level of the basic building blocks. This will make circuits realised in such a technology highly competitive. The high performance will not apply for every application, of course. Just like in microelectronics different classes of applications need different processes, e. g. for high-voltage, high speed, high power or low power, etc. In a similar way photonics will need a few different generic technologies, optimized for different kinds of applications, to cover a major part of all applications. But the number of generic technologies that is required is far smaller than the number of technologies which are presently in use.

5. A generic foundry model in photonics

Once a mature generic integration technology has been developed it needs to be made accessible with a low entry barrier to a large number of users. In microelectronics programs like MOSIS [38] in the US and EUROPRACTICE [39] in Europe organize low-cost access to commercial foundries, including documentation, training and access to design software. In Photonics such a service is not available today.

Custom foundry model

After the turn of the century, forced by the high exploitation costs and the small load of their cleanrooms, a number of photonic fab owners have opened their fabs to external, so called fabless users. These companies, which call themselves foundries, develop processes for specific customer components and specific customer requirements, in close cooperation with the customer. Usually the process is owned by the customer, who has paid for its development. We call such a foundry, therefore, a custom foundry, and the approach the "custom foundry model". This approach has led to a significant reduction of the entry costs for newcomers, because a newcomer does not have to build his own cleanroom, but shares the costs of the cleanroom with a large number of other fab users. In this model the process development is still application specific, however, so that its costs will not be shared with other users. The entry costs will, therefore, remain significantly higher than in microelectronics, where existing generic foundry processes are available for the development of Application Specific ICs (ASICs), so that not only the cleanroom costs, but also the process development costs are shared by a large number of users.

ePIXnet

In Photonics, generic foundries, offering access to generic integration processes, are non-existent today, but the first steps towards their creation have been made by the FP6 Network of Excellence ePIXnet (European network of excellence on Photonic Integrated Components and Circuits, www.epixnet.org). It started in September 2004 with a large number of academic and industrial members on an ambitious mission: to move from a model of independent research to a model of integrated research with shared use of expensive technological infrastructure. In the background were the steadily increasing costs of cleanroom facilities that restricted Photonic Integration research to the ever smaller group of institutes that could afford a cleanroom. The idea was to enlarge the group of users by stimulating cleanroom owners to organise access to their facilities for a broader circle of non-cleanroom owning partners. After experimenting for two years with facility access activities the ePIXnet Steering Committee published a vision document [40] about a foundry model in micro- and nanophotonics and it took the step to the initiation of integration technology platforms.

Integration technology platforms

Two major integration technologies were identified: InP-based integration technology, which supports the highest degree of functionality, including compact lasers and amplifiers, and Silicon Photonics technology, which offers most of the functionality offered by InP except for the compact lasers and amplifiers, but at a potentially better performance

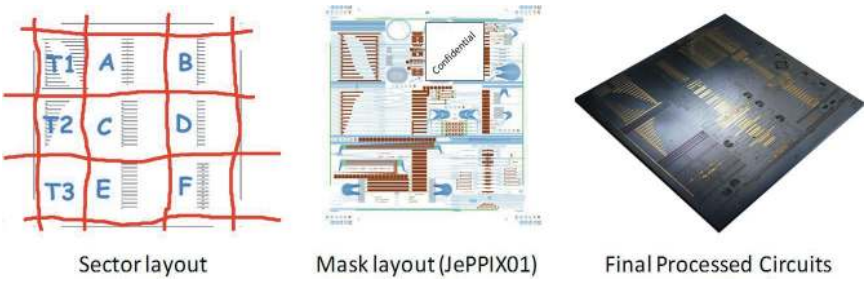

Figure 4 (online color at: www.lpr-journal.org) Example of a Multi-Project Wafer (MPW) realised in the JePPIX01 process. The wafer is subdivided in 9 sectors, three for test structures and 6 for user designs. The picture in the middle is an example of a mask layout, and at the right is a photograph of the realised wafer.

and lower cost because of its compatibility with mature CMOS technology. For both technologies a platform organization was established; JePPIX for InP-based integration technology [41], and ePIXfab for Silicon Photonics [42]. Later a third platform with dielectric waveguide technology was added (TriPleX), which offers low-loss and high-quality passive optical functions and some thermo-optic active functions, through the whole wavelength range from visible to infrared [43]. All three platforms started by providing open access for research purposes to a relatively mature integration technology: the JePPIX platform to the InP-based integration technology of the COBRA institute of TU Eindhoven, the ePIXfab platform to the SOI-technology of IMEC, and the TriPleX platform to the technology of the Dutch company Lionix.

Multi-project wafer runs

All three platforms offer access to their technologies through Multi-Project Wafer Runs (MPWs), a well-known concept in micro-electronics, but not earlier applied in Photonics. MPWs lead to a significant reduction of the costs of chip R&D by combining test versions from different users in a single wafer run, so that the costs of a run are shared by several users. Figure 4 illustrates how this is done. The figure at the left shows how a wafer is subdivided into 9 sectors, three for testing and six for user designs. The picture in the middle shows an actual mask design from a JePPIX MPW run and the picture at the right a photograph of a realised wafer sector (before cleaving of the individual user and test chips). If the pattern is repeated a number of times on a wafer each users will get several samples of his chip.

Generic foundry model

The initiatives taken by ePIXnet were first steps towards full introduction of the generic foundry model in photonics. In a fully operational model the following activities have to be addressed:

1. Access to mature and well documented commercial foundry processes via full or MPW runs.
2. Availability of dedicated design software and component libraries for enabling fast and accurate design (design kits).
3. Brokering service: assistance and training of users that are not familiar with the technology. Assembling different user designs in a mask set for an MPW-run.
4. Design houses that can help users that do not have the know how to design their own chips.
5. Access to generic test facilities.
6. Access to generic packaging facitilies.

This model is well known in microelectronics for the development and manufacturing of ASICs. The ePIXnet integration technology platforms are presently gaining experience with all these activities at a research level, but a number of projects[2] have been started for moving the foundry model from the research to the industrial stage and introducing ASICs in photonics, where we will call them ASPICs: Application Specific Photonic ICs.

6. Prospects for generic photonic integration

R&D time and cost reduction

A generic foundry model will lead to a dramatic reduction of the costs of PIC R&D and manufacturing for small or medium volumes and to a significant shortening of the R&D cycle. Through access to an existing well documented high performance process the relatively high entry costs of process development, which form a major cost contribution in the custom foundry model, are strongly reduced through cost sharing with many users. A further reduction of the R&D costs is achieved by combining designs of several users in a single MPW run, the costs of which are shared by all participating users. And through the availability of accurate design software the number of R&D cycles needed for getting a chip onto specs will be strongly reduced. Another time and cost reduction is obtained in testing and qualification of the chip, which is a major cost factor for chips for which reliable operation is required under harsh conditions. A large part of the qualification applies to the manufacturing and packaging process and this part need not be repeated for each individual product, but it applies to all ASPICs that are developed according to the design rules.

Due to these cost and time advantages the costs of PIC R&D and manufacturing in the generic foundry model will be reduced by more than a factor of ten for small and medium volumes, as compared to the custom foundry model.

[2] IST projects EuroPIC and PARADIGM for InP-technology and HELIOS, WADIMOS and PhotonFAB for Silicon Photonics. Dutch national projects MEMPHIS, IOP Photonic Devices and the STW GTIP program on Generic Technologies for Integrated Photonics. Total investments in these projects are several tens of million Euros.

More details about the cost reductions in the generic foundry model are given in [44]. Such a large reduction of R&D time and chip manufacturing costs will lead to a large growth of the share of PICs in the photonic components market.

Performance

A frequently asked question is about the performance of generic foundry processes: is it possible to develop generic processes that are competitive with application specific processes. Even though generic processes will not be the solution for any application they will be competitive for a broad range of applications. For InP-based generic integration, for example, the foundry processes that are being developed in the EuroPIC and the PARADIGM process are based on existing integration platform technologies for high-performance tunable lasers and high speed receivers. The research is focused on extending the functionality of these platform technologies without loss of performance for the individual building blocks. Table 2 gives an overview of the targeted performance for the most important building blocks in a foundry process as it should become available after successful completion of the PARADIGM project in 2014. It combines a broad functionality with a high performance on the level of the individual building blocks. And we expect that through focused investments in a few generic technologies their performance will increase steadily and outperform ever more application specific technologies, similar to what happened with CMOS in microelectronics.

Table 2 Target values for the basic building blocks in an InP-based generic foundry process.

Building block	Specification	Target value
Waveguide section	Propagation loss	< 1 dB/cm
Phase Sections	eo-efficiency	> 20 degr/V mm
	Insertion loss	< 1 dB
	Bandwidth[1]	40 GHz
Gain Sections	Small Signal Gain[2]	50 cm^{-1}
	Output power[3]	> 50 mW
Detector section	Responsivity	0.6 A/W
	Dark current@-2 V	< 20 nA
	Bandwidth[1]	> 40 GHz

[1] Bandwidth is dependent on design (section length, bondpath configuration). The number is a representative value.

[2] The number is indicative for a current injection level of 4 kA/cm.$^{-2}$.

[3] Typical value for a 500 µm long SOA-section with 200 mA injection current @ 25 °C.

Market development

So far the use PICs has been mainly restricted to some niche areas in telecom applications, where their specific functionality cannot be met by competing technologies. With the expected cost reductions through a generic foundry approach they will also become competitive in high volume markets like the telecom access network, where they may be applied in the Central Office for integration of larger numbers of circuits that have to be repeated for each subscriber or group of subscribers. In future 10 Gb/s access network they may become competitive also in the subscriber transceiver module.

But when R&D and manufacturing costs drop photonic chips will increasingly penetrate also other applications. A good example is the fibre sensor market, which was over 300 M$ in 2007 with double digit annual growth figures. A significant part of the sensor costs is in the readout unit, which contains a light source, a detector and some signal processing circuitry. Here Photonic ICs can replace a significant part of the existing modules, and enable novel sensor principles. Examples are various types of strain sensors, heat sensors and a variety of chemical sensors [45].

Optical Coherence Tomography is another potential application. Traditionally OCT is done in the 800 nm window, which is the preferred choice for retina diagnostics. For skin or blood vessel diagnostics 1500 nm is a better wavelength, because there the penetration depth is three times as large due to reduced scattering losses at this wavelength. This provides good opportunities for InP PICs in OCT equipment [46].

An interesting class of devices are pico and femtosecond pulse lasers [47]. Here PICs containing mode locked lasers, optionally combined with pulse shapers, can provide small and cheap devices that can be used in widely differing applications, such as high-speed pulse generators and clock recovery circuits, ultrafast AD-converters, and in multi-photon microscopy.

These are just a few examples. Once ASPICs get really cheap they will offer ample opportunity for small and large companies to improve their competitiveness by applying them in their products.

A more extensive discussion of a foundry model for InP-based Photonic ICs is given in [44]. Alternative visions on the development of Photonic Integration are given in [48] and [49].

Complexity development

We expect that in the second half of this decade the market for Photonic ICs will strongly increase when low-cost access to Photonic IC-technology will become available through commercial foundries. We do not expect, however, that with the present technology this market growth will be accompanied by a strong increase in chip complexity. In passive devices unavoidable component losses will restrict the total number of components that can be cascaded. And in active PICs SOAs and lasers typically have a power dissipation of several 100 mW. So their number is restricted to several tens up to a maximum of a few hundreds, because of heat sinking limitations. Secondly, although today's PICs often carry digitally modulated signals, the basic building

blocks and the circuits built from them essentially operate in an analog mode, which means that on passing a number of components the signal will accumulate noise and distortion and needs to be regenerated. Regenerators can be integrated too, but they consume space and power. We expect, therefore, a saturation of chip complexity at a level around 1000 components per chip, as indicated in Fig. 5 by the curve labeled "Generic InP".

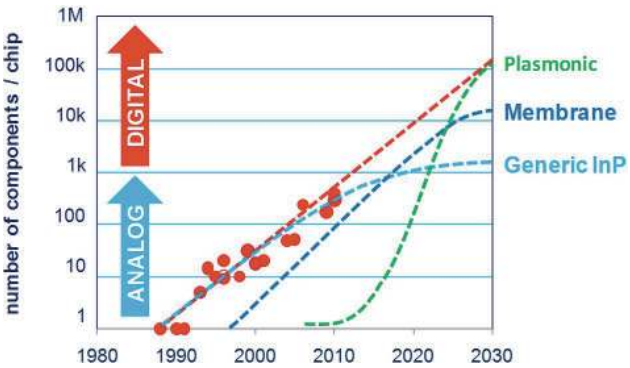

Figure 5 (online color at: www.lpr-journal.org) Vision on the complexity development of Photonic ICs.

This does not mean that the complexity development of photonic chips will end at a level of 1000 components per chip. For higher complexity levels we will have to move to other technologies, however, which will be discussed in the next section.

7. The next generation

A larger complexity can be supported, in principle, in membrane based circuits, where component dimensions and power dissipation can be significantly smaller. This is a result of the strong light confinement in thin membranes with a high vertical index contrast, as they are presently applied in Silicon Photonics. In the past years silicon membrane technology has seen a great improvement in performance and maturity.

Because in many cases smaller also means faster and lower power consumption, membrane technologies are a promising candidate for becoming the next generation generic integration technologies. A serious problem that has to be addressed is the integration of active devices. Recent research has demonstrated the feasibility of high speed modulators and detectors using SiGe technology [50]. The main remaining problem in silicon based photonic ICs is the generation and amplification of light: being an indirect semiconductor silicon is not suitable for fabricating compact and efficient light sources and amplifiers. Several interesting idea's have been pursued to obtain monolithic integration of light sources in silicon photonics. These include porous Si [51], Si nanocrystals [52], Er-doped Si [53] and using GeSn [54]. Recently MIT [55] has proposed and demonstrated that gain can be obtained from strained and heavily n-doped Ge grown on Si. So far the performance of these lasers is still far away from the performance of direct bandgap semiconductor lasers on GaAs and InP. Therefore, the most promising silicon membrane integration platforms aim at using III-V lasers. Four different approaches for this are depicted in Fig. 6. IBM [56] and MIT [57] follow an approach in which light is coupled into the silicon membrane from an external source (Fig. 6a). This is clearly the shortest route to an operational on-chip interconnect network, but the scalability is poor: without integrated light sources the complexity of PICs will remain limited. This is the main reason that up till now the complexity of silicon photonic ICs is lagging behind InP, with 86 components per chip being the highest complexity reported so far [58].

IMEC, LETI and COBRA are working on an approach in which lasers and detectors are fabricated in a III-V layer stack on top of the silicon membrane, in such a way that the light tunnels to the silicon layer through a thin low-index layer [59] (Fig. 6b). In this approach it is difficult to get efficient coupling to the silicon layer, however, especially if the devices get smaller. UCSB and Intel apply a slightly different approach, in which the silicon waveguide is provided with gain by atomic bonding of an active III-V layer stack directly onto the silicon membrane [60] (Fig. 6c). Also in this approach coupling of the light from the active layer to the passive silicon waveguide remains difficult because the requirements for high confinement and high coupling efficiency are contradictory.

We have, therefore, chosen another approach in which we replace the silicon membrane with an InP-membrane

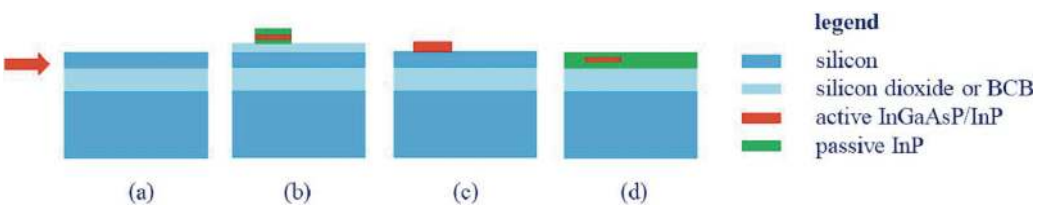

Figure 6 (online color at: www.lpr-journal.org) Schematic picture of four different ways to generate light in a photonic layer on top of a silicon IC: a) Coupling light from an external source into the (passive) circuit (IBM, MIT). Amplification is not possible in this way. b) Coupling light from a laser source which is processed on top of the passive circuit. (IMEC, LETI and COBRA). Amplification is difficult in this way. c) By bonding and processing an active InGaAsp/InP layer on top of the silicon layer which provides gain to the silicon waveguides (UCSB and Intel) d) By replacing the silicon membrane with an InP-membrane that contains both passive and active regions (IMOS).

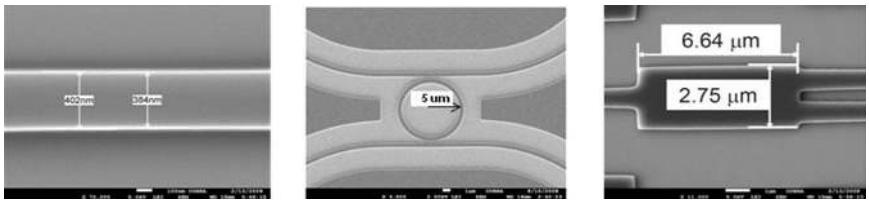

Figure 7 Passive IMOS-devices, from left to right: a) Photonic wire waveguide of 400 nm width b) Ring filter with 5 μm radius c) Ultra-small 1-by-2 MMI coupler.

(IMOS: InP Membrane On Silicon). Active regions are created locally in this membrane prior to bonding, using selective epitaxial regrowth techniques on a submicron scale (Fig. 6d). This concept promises a number of important advantages. As both active and passive functions are now realized in one membrane, coupling between them is no longer a critical issue. Also, the requirements on alignment with respect to the underlying substrate are much alleviated, because there is is only electrical coupling between the photonic membrane and the underlying electronics and the much more critical optical coupling is avoided. Finally, because we use a thick polymeric layer for bonding of the InP-membranes on a substrate, the realization becomes virtually independent of the surface morphology. This is important for future combination of IMOS photonic integrated circuits with CMOS circuitry.

The optical properties of an InP-membrane for passive optical components are very similar to those of a silicon membrane. We have already demonstrated a number of high-quality passive components in IMOS technology (see Fig. 7): photonic wires with 7 dB/cm losses, curved waveguides with only 5 μm bending radius and negligible loss, extremely small MMI-couplers with only 0.6 dB excess loss and ring filters with a Q-factor larger than 15000 [61].

However, to achieve a full set of devices for a photonic integration platform, as depicted in Fig. 2, more is needed. A passive device that is so far lacking in InP-based membranes is a polarization converter. We propose a very short device for this, which is realizable with standard InP-processing and has a length of 4 μm [62]. This fabrication tolerant polarization converter, drawn in Fig. 8, consists of two triangular waveguide sections and operates over the full L-, C-, and S-bands.

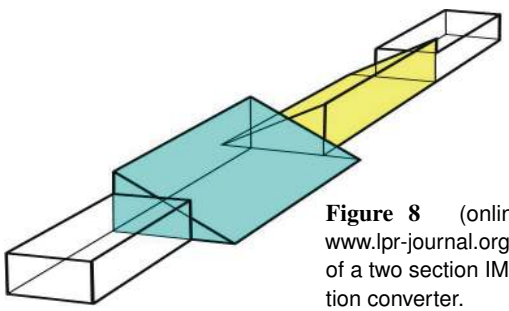

Figure 8 (online color at: www.lpr-journal.org) Schematic of a two section IMOS polarization converter.

The most important part in creating a photonic integration platform in a membrane technology is including active devices; lasers and amplifiers. We have achieved encouraging results for selective growth of very small active regions [62]. Figure 9 shows a disc-shaped active region of 250 nm radius, containing four quantum wells designed for light emission at λ=1.55 μm. After the regrowth these very small active regions indeed show light emission. To obtain the full benefit of using semiconductor lasers electrical injection is needed. This is currently under development.

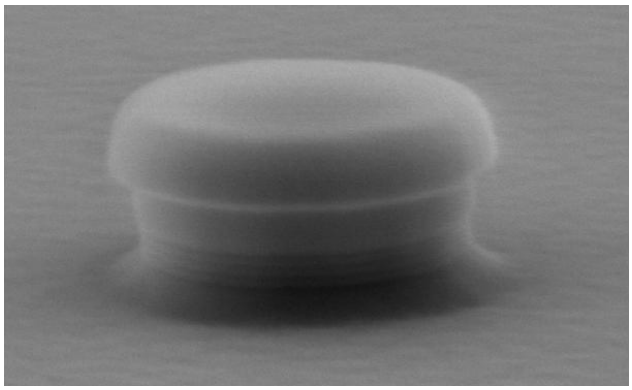

Figure 9 A sub-micron active region before regrowth.

IMOS is a merger between classical InP-based photonics and "classical" Silicon Photonics and eventually it may replace classical InP-photonics in a broad range of applications, where high power is not needed (because membranes are not suitable for high-power operation). Furthermore it will address the market that "classical" Silicon Photonics cannot address because of its inability to generate and amplify light efficiently. As the integration of components for light generation and amplification will become more important with increasing complexity in photonic circuits and networks, IMOS has the potential to address an increasingly important part of the market for silicon based photonics.

Due to the smaller component dimensions and power consumption of membrane devices we expect that membrane technologies with efficient and compact integrated light sources and amplifiers will allow for a complexity an order of magnitude higher than classical InP-photonics, as indicated in Fig. 5 by the curve labeled "membrane".

8. The ultimates in integration

For Photonic integration to move towards LSI (> 10,000) or VLSI (> 1,000,000) integration levels, a change from analogue to digital signal processing will be necessary. This is quite similar to the development path in microelectronic ICs, where analog circuits usually do not contain more than a few hundred transistors per circuit block. The breakthrough to VLSI did not occur in analog electronics but in digital electronics, where signal regeneration inherently occurs after each processing step, so that operations can be concatenated indefinitely.

An all-optical digital information processing system requires: a component or set of components that are boolean complete and can be cascaded to make any digital function, the component(s) must be of microscopic size and able to be densely integrated and interconnected using integrated circuit technology (which also implies that the components have low power requirements), finally the components must operate at very high speed, to be competitive with electronics. Over the past 40 years significant research has gone into trying to make components that fulfill the above requirements. However, the lack of materials with fast, strong, low power optical non-linearities has meant that high speed, complex, integrated digital optical processors have not been achieved.

Lasers have a non-linear optical characteristic suitable for digital operations, and also they are a light source for the optical signals. Micro or nano lasers also have small size, low power, can be integrated in large numbers on a chip, and can potentially have high speed operation [63]. They can also be coupled together to form digital functions [64].

Miniaturization is of key importance for higher speed operation at lower power of the lasers that implement the digital functions. However, the use of dielectric cavities and diffraction limits the size of the optical mode in the cavity and the overall cavity size. Typically, even in the dielectric cavities that have the smallest optical mode size, the overall laser dimensions are several wavelengths. The use of metals to form the laser resonator allows for a further reduction of device dimensions far below the wavelength of light in 2 or 3 dimensions.

For the general implementation of digital functions and in particular for isolation between device inputs and outputs, it is likely that the relaxation oscillation frequency of the laser will limit the device speed. It has been predicted that the smallest of these metal based lasers could reach terahertz modulation or relaxation oscillation frequencies with low power [65]. Such properties could make digital photonics competitive with electronics for high performance applications. Furthermore, such small high speed low power lasers may also satisfy the requirements for on chip optical interconnects.

For a long time it was thought that metal losses in nanocavities would be too high for laser operation. However, just in the last couple of years experimental efforts to use metals to form the nano-laser resonator have allowed both the overall size of the laser to be reduced to smaller than the wavelength of light, and also the optical mode dimensions to be reduced below the diffraction limit. The progress that has been made by many groups in just a few years has been remarkable [66]. Some of these devices are coming close to being useful light sources, and it may only be a few years before we see lasers based on metallic nano structures in applications.

Our particular approach is based on encapsulating etched pillars of double hetero structures in a thin insulator and covering the whole structure with a thick noble metal layer. The first example of this technique was reported in [67] and is shown in Fig. 10. The pillar had an overall diameter of approximately 260 nm and an InGaAs active region height of 300 nm. The presence of the InGaAs heterostructure in the pillar and the metal formed a resonator with an optical mode trapped on the InGaAs gain medium. At cryogenic temperatures it was possible to obtain sufficient gain in the InGaAs to overcome losses in the resonator and achieve lasing at a wavelength of approximately 1400 nm. The device, which was the smallest electrically injected IR-laser ever reported, operated with a threshold current of 6 μA at 77 K, in an intermediate regime between dielectric and plasmonic photon confinement.

A significant advantage of the encapsulated heterostructure approach is that waveguides can be formed by changing the shape of the pillar cross-section, e. g. by etching the same structure in a long thin rectangular pillar. Coating the whole pillar in metal forms a section of so-called metal-insulator-metal (MIM) waveguide [68]. The dielectric/semiconductor pillar core in the middle forms the insulator region where the guided optical mode is tightly confined. Importantly these MIM waveguides are one of the few structures that allow true deep sub-wavelength confinement and guiding of light, propagating light even with an arbitrarily thin insulator region, see Fig. 11. To this end we have demonstrated Fabry-Perot lasers exploiting a MIM waveguide with

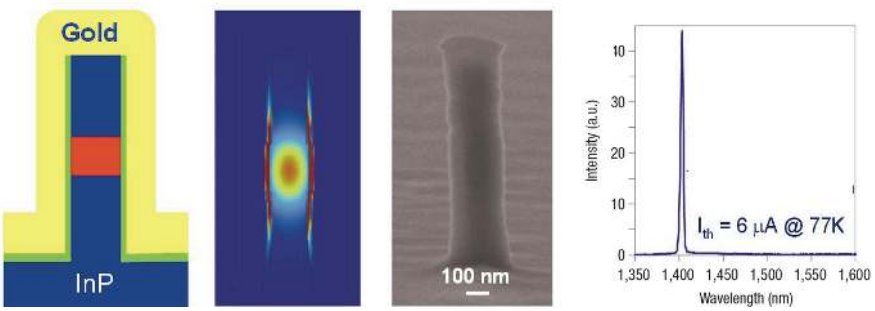

Figure 10 (online color at: www.lpr-journal.org) Metallic nanocavity laser. From left to right: a) Structure: An InP pillar with 250 nm diameter. The laser has a conventional double heterostructure with a 300 nm active region (red area) in the center. It is covered at the sides with a thin dielectric isolation layer and encapsulated with a thick gold layer, which forms a metallic cavity for the laser light. Current is injected from the top of the pillar to the bottom. b) Simulated light distribution in the laser cavity c) Electron-Microscope photograph of a realised device (gold cap removed) d) Measured laser emission spectrum.

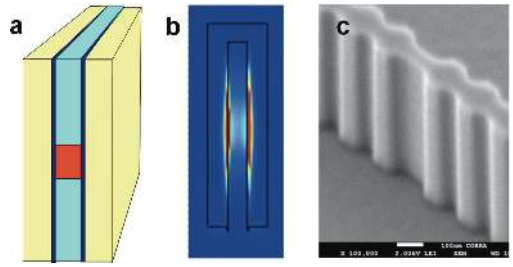

Figure 11 (online color at: www.lpr-journal.org) Metal-Insulator-Metal waveguides via encapsulated heterostructures a) Schematic of the structure. The light blue is InP, while the red in the center is the higher index gain medium InGaAs. The sidewalls are coated with a thin layer of dielectric (SiN, dark blue) before coating in either gold or silver (yellow) to form the MIM waveguide. b) Simulated light distribution in the waveguide, showing light is held in the center of the pillar due to the index loading of the InGaAs, also that a significant amount of light travels in the thin SiN cladding. c) Electron-Microscope photograph of an etched semiconductor core of the MIM waveguide. Via lithography complex core shapes can be made, such as this one which implements a Bragg grating [74].

a center insulator region about half the diffraction limit in size and propagating a gap-plasmon mode [69]. Here the semiconductor core of the laser was just 90nm thick, while lasing at a wavelength of ~ 1400nm.

Using an MIM waveguide approach allows efficient coupling of the laser radiation to either conventional dielectric waveguides [70], or into other passive or active gap-plasmon mode waveguide elements [71]. In theory it has been shown that many of the common waveguide components found in conventional integrated optics can be formed with these MIM waveguides. For example, splitters, bends, and gratings [71, 72]. Another feature is that not only is the confinement of light inside the waveguide sub-wavelength, but additionally there can be very tight packing density of the waveguides [68].

Furthermore the active core region and also the optical mode of the MIM waveguide can be significantly reduced below the diffraction limit in two dimensions. We are working on constructing these deep subwavelength waveguides by using a combination of index loading and sidewall shaping in the pillar, to highly localize the optical mode [73]. Such devices can in theory have small optical modes, only a few tens of nanometers in size, overlapping a similarly small active region. The small size, good modal overlap with the gain region and low quality factor cavities should in theory lead to lasers with terahertz intrinsic modulation bandwidths with pump power levels in the tens of microwatts. Such small, high speed and low power lasers may form the basis for integrated digital photonic processing systems, that could be competitive with electronics for simple high speed processing tasks. In principle, integration of more than 100,000 of these lasers in a single chip seems feasible. This will bring us close to photonic VLSI.

Furthermore plasmonic nanolasers will be an interesting platform to push the minimum limits of laser size. Although the field of metallic and plasmonic nano-lasers is still in its infancy, great progress has been made, and in theory it appears plausible that high speed, efficient coherent (and incoherent) light emitters will appear. These lasers or light emitting diodes will have many applications in integrated optics, lighting and short distance communication systems.

9. Conclusions

It has been argued that Moore's law does not apply to photonics because of the large differences between microelectronic and photonic integration technologies. This is indeed true for today's model in photonic integration. But as these differences are, at the same time, a major reason that photonic integration has not succeeded in initiating a cost reduction similar to that we have seen in microelectronics, the right conclusion should be that we have to remove these differences as far as possible. By applying the methodology of microelectronics to photonics we expect a dramatic reduction of the costs for R&D and manufacturing of photonic ICs and a breakthrough to a wide range of application fields, in telecommunications and datacommunications, but also for application in sensors, medical equipment, metrology and consumer photonics. Such a breakthrough will accelerate the development of more advanced integration technologies that will ultimately bring us VLSI Photonic ICs.

List of abbreviations:

ASICs	Application Specific ICs
AWG	Arrayed Waveguide Grating
BCB	Benzocyclobutene
CMOS	Complementary Metal-Oxide-Semiconductor
DFB	Distributed Feedback Laser
GaAs	Gallium Arsenide
Ge	Germanium
ICs	Integrated Circuits
IMOS	InP Membrane on Silicon
InP	Indium Phosphide
JePPIX	Joint European Platform for Photonic Integration of InP-based Components and Circuits
LSI	Large Scale Integration
MIM	Metal-Insulator-Metal
MMI	Multi-Mode Interference coupler
MPWs	Multi Project Wafer Runs
OCT	Optical Coherence Tomography
PICs	Photonic ICs
PM-DQPSK	Polarisation Multiplexing Differential Quadrature Phase-Shift Keying
R&D	Research & Development
Si	Silicon
SOAs	Semiconductor Optical Amplifiers
SOI	Silicon on Insulator
VLSI	Very Large Scale Integration
WDM	Wavelength Division Multiplexing

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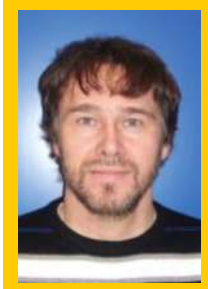

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