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More on the $1/f^2$ Phase Noise Performance of CMOS Differential-Pair LC -Tank Oscillators

Pietro Andreani, *Member, IEEE*, and Ali Fard

Abstract—This paper presents a rigorous phase noise analysis in the $1/f^2$ region for the differential CMOS LC -tank oscillator with both nMOS and pMOS switch pairs. A compact, closed-form phase noise equation is obtained, accounting for the noise contributions from both tank losses and transistors currents, which allows a robust comparison between LC oscillators built with either one or two switch pairs.

The fabricated oscillator prototype is tunable between 2.15 and 2.35 GHz, and shows a phase noise of -144 dBc/Hz at 3 MHz offset from the 2.3 GHz carrier for a 4 mA bias current. The phase noise figure-of-merit is practically constant across the tuning range, with a minimum of 191.5 dBc/Hz. A reference single-switch-pair oscillator has been implemented and tested as well, and the difference between the phase noise levels displayed by the two oscillators is very nearly the one expected from theory.

Index Terms—CMOS, LC , oscillators, phase noise, VCOs.

I. INTRODUCTION

THE theoretical study of phase noise in electrical oscillators is a considerably more difficult task than traditional noise analysis, mainly due to the two following reasons: first, any real oscillator generates large signals, which means that a small-signal circuit with component values linearized around a constant bias point is no longer able to capture the true nature of the oscillator and of the noise sources therein active; the second reason, more subtle and often neglected, is that the conversion of noise into phase noise (“noise-to-phase-noise conversion” in the following) is not constant across the oscillation period.

That a large-signal analysis may yield unexpected results has been known at least since the work by Rael and Abidi [1] (building largely on a previous study of the active mixer by Darabi and Abidi [2]), where the correct equation for the phase noise caused by tank losses and MOS switches in the classical single-switch-pair LC -tank oscillator was presented (a formal derivation of this and other results has been given in [3]). The notable feature in this equation is that the phase noise caused by the MOS switches is independent of the switch transconductances, which may appear at variance with the familiar notion that transistor noise is a linear function (at least ideally) of the transistor transconductance. A direct consequence of this property is that doubling the bias current does not change

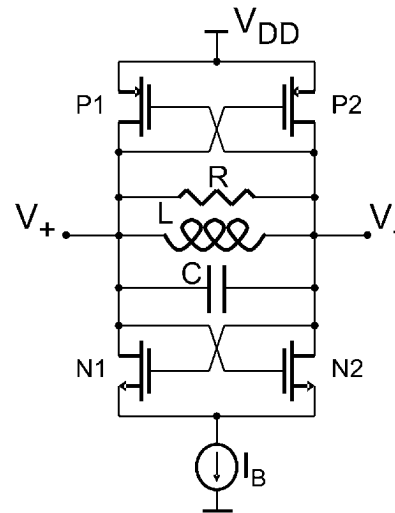


Fig. 1. Simplified schematic view of the DS-VCO.

the noise generated by the oscillator core, while it doubles the oscillation amplitude (provided the oscillator is still working in the current-limited region); thus, phase noise is improved by 6 dB, which is very different from the 3 dB one would predict extrapolating from linear amplifier theory. Recently, we have shown that the same behavior is displayed by Colpitts oscillators as well, both CMOS [3] and bipolar [4].

The nontrivial nature of noise-to-phase-noise conversion has been first explicitly recognized by Hajimiri and Lee, whose Impulse Sensitivity Function (ISF, with symbol Γ) theory of phase noise [5], [6] is based on the acknowledgement that noise-to-phase-noise conversion is a linear, time-variant (LTV) process. Ignoring the real expression of the ISF associated to the most important noise sources generally results in a severely faulty estimate of phase noise (see, e.g., [3] for a worked-out example).

To summarize, we can state that a correct phase noise analysis is twice time-variant, since transistor noise is generated in a cyclo-stationary fashion, and the subsequent noise-to-phase-noise conversion is itself time-variant.

In this paper, a rigorous phase noise analysis of the CMOS LC -tank (voltage-controlled) oscillator with double switch pair [7] (referred to as the DS-VCO, shown in Fig. 1) is presented. A simplified large-signal analysis of the DS-VCO, with the goal of obtaining the expressions of the transistors transconductances, is performed in Section II; Section III recalls basic facts about the ISF theory and its use in phase noise analysis, while Section IV derives the ISFs associated to the MOS channel current noise sources in the DS-VCO. This will enable the calculation of the effective MOS noise contributions to phase

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noise (Section V), eventually leading to the desired DS-VCO phase noise formula (Section VI). The performance comparison between the DS-VCO and the very popular single-switch-pair LC oscillator (SS-VCO) is developed in Section VII, while Section VIII deals with the phase noise figure-of-merit (FoM) of the two oscillators. The impact of parasitic tank capacitances in the DS-VCO is discussed in Section IX, again comparing the two oscillator topologies, and a new tail bias circuit is described in Section X. Finally, measurement results are disclosed in Section XI.

II. LARGE-SIGNAL ANALYSIS OF THE DS-VCO

Fig. 1 shows the simplified schematic view of the DS-VCO, where all losses have been compacted into the equivalent tank resistance R . In the following, we will adopt the ideal square-law expression for MOS transistor current in the active (saturation) region, and neglect all parasitic capacitances. Assuming that the current in the RLC tank is an ideal square wave (which is not far from reality in the low-gigahertz range for the targeted technology), and that the tank- Q is reasonably high, it is well known that the voltage waveform across the tank is almost sinusoidal, i.e.,

$$V_+ - V_- \approx A \sin(\phi) \quad (1)$$

(where $\phi \equiv \omega t$, ω being the angular frequency of oscillation), with amplitude

$$A \approx \frac{4}{\pi} R I_B. \quad (2)$$

Looking at Fig. 1, we can immediately set up the following equations for the currents in the nMOS pair:

$$I_{N1} = \frac{\beta_n}{2} [V_- - (V_s + V_{th,n})]^2 \quad (3)$$

$$I_{N2} = \frac{\beta_n}{2} [V_+ - (V_s + V_{th,n})]^2 \quad (4)$$

$$I_{N1} + I_{N2} = I_B \quad (5)$$

where V_s is the voltage at the common nMOS source, $V_{th,n}$ the nMOS threshold voltage, I_B the tail bias current, and $\beta_n = \mu_n C_{ox} W_n / L_n$ (μ_n being the electron mobility, C_{ox} the unit gate capacitance, and W_n and L_n the nMOS transistors width and length). Using (1), we find easily

$$I_{N1} = \frac{\beta_n}{2} \left[\frac{A}{2} \left(-\sin(\phi) + \sqrt{2 \sin^2(\Phi_n) - \sin^2(\phi)} \right) \right]^2 \quad (6)$$

$$I_{N2} = \frac{\beta_n}{2} \left[\frac{A}{2} \left(\sin(\phi) + \sqrt{2 \sin^2(\Phi_n) - \sin^2(\phi)} \right) \right]^2 \quad (7)$$

where Φ_n is defined by

$$\Phi_n = \arcsin \sqrt{\frac{2I_B}{\beta_n A^2}}. \quad (8)$$

Equations (6)–(7) are valid as long as both currents are larger than zero, i.e., for $-\Phi_n \leq \phi \leq \Phi_n$ as well as for $-\Phi_n + \pi \leq \phi \leq \Phi_n + \pi$.

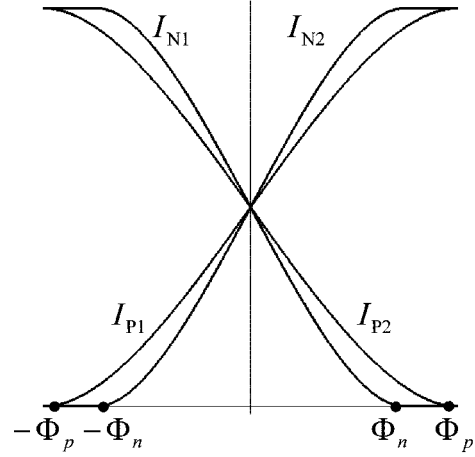


Fig. 2. Example of current commutation in the DS-VCO, when the nMOS pair is slightly faster than the pMOS pair.

Equally simple is to set up the relevant equations for the pMOS currents:

$$I_{P1} = \frac{\beta_p}{2} [(V_{dd} + V_{th,p}) - V_-]^2 \quad (9)$$

$$I_{P2} = \frac{\beta_p}{2} [(V_{dd} + V_{th,p}) - V_+]^2 \quad (10)$$

$$I_{P1} + I_{P2} = I_B \quad (11)$$

where V_{dd} is the power supply voltage, $V_{th,p}$ the pMOS threshold voltage, and $\beta_p = \mu_p C_{ox} W_p / L_p$ (μ_p being the hole mobility, and W_p and L_p the pMOS transistors width and length); solving these equations yields

$$I_{P1} = \frac{\beta_p}{2} \left[\frac{A}{2} \left(\sin(\phi) + \sqrt{2 \sin^2(\Phi_p) - \sin^2(\phi)} \right) \right]^2 \quad (12)$$

$$I_{P2} = \frac{\beta_p}{2} \left[\frac{A}{2} \left(-\sin(\phi) + \sqrt{2 \sin^2(\Phi_p) - \sin^2(\phi)} \right) \right]^2 \quad (13)$$

valid for $-\Phi_p \leq \phi \leq \Phi_p$ as well as for $-\Phi_p + \pi \leq \phi \leq \Phi_p + \pi$, with

$$\Phi_p = \arcsin \sqrt{\frac{2I_B}{\beta_p A^2}}. \quad (14)$$

A plot of the four transistor currents¹ during one current commutation is shown in Fig. 2, where it is arbitrarily assumed that Φ_n is somewhat smaller than Φ_p .

The transconductances of all transistors follow immediately from the respective current equations; with obvious meaning of the symbols, we can write

$$g_{m,N1} = \frac{\beta_n A}{2} \left(-\sin(\phi) + \sqrt{2 \sin^2(\Phi_n) - \sin^2(\phi)} \right) \quad (15)$$

$$g_{m,N2} = \frac{\beta_n A}{2} \left(\sin(\phi) + \sqrt{2 \sin^2(\Phi_n) - \sin^2(\phi)} \right) \quad (16)$$

¹The current equations above assume that both transistors in each pair are working in the active region, when both are on. It is easy to check that this is the case as long as $V_{th,n} \geq V_{od,n}$ ($V_{th,p} \geq V_{od,p}$) where $V_{od,n} = \sqrt{2I_B/\beta_n}$ ($V_{od,p} = \sqrt{2I_B/\beta_p}$) is the overdrive voltage for a single nMOS (pMOS) transistor when conducting the whole I_B . These inequalities are very easily satisfied.

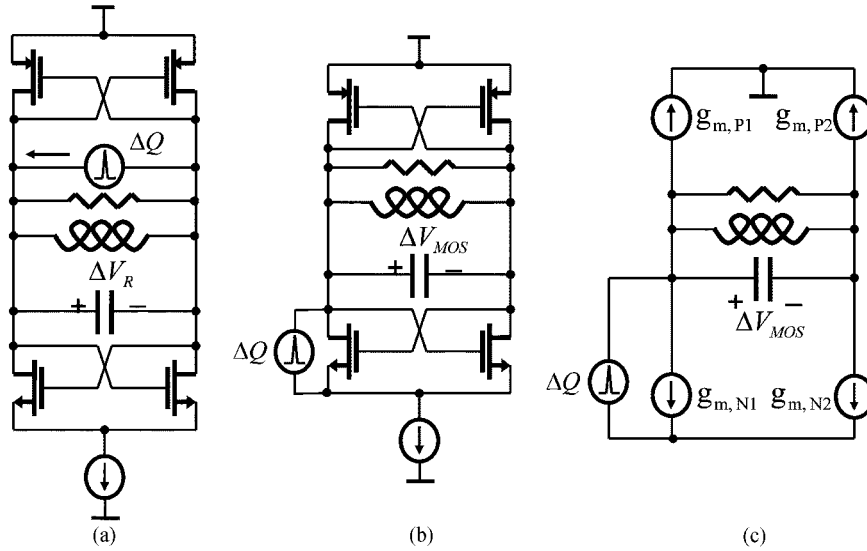


Fig. 3. (a) Setup for the calculation of the ISF associated to the tank resistance; (b) setup for the calculation of the ISF associated to nMOS switch N1; (c) small-signal circuit derived from the circuit in (b).

$$g_{m,P1} = \frac{\beta_p A}{2} \left(\sin(\phi) + \sqrt{2 \sin^2(\Phi_p) - \sin^2(\phi)} \right) \quad (17)$$

$$g_{m,P2} = \frac{\beta_p A}{2} \left(-\sin(\phi) + \sqrt{2 \sin^2(\Phi_p) - \sin^2(\phi)} \right). \quad (18)$$

These transconductances play a fundamental role in the following, as they appear both in the transistor noise formulas and in the associated ISF expressions.

III. ISF AND PHASE NOISE

According to the ISF theory, the phase noise $\mathcal{L}(\Delta\omega)$ caused by a white current noise source $\overline{i_n^2}$ in an LC-tank oscillator is [6]

$$\begin{aligned} \mathcal{L}(\Delta\omega) &= 10 \log \left(\frac{\Gamma_{i_n, \text{rms}}^2 \overline{i_n^2} / \Delta f}{2q_{\text{max}}^2 \Delta\omega^2} \right) \\ &= 10 \log \left(\frac{\Gamma_{i_n, \text{rms}}^2 \overline{i_n^2} / \Delta f}{2A^2 C^2 \Delta\omega^2} \right) \end{aligned} \quad (19)$$

where $\Delta\omega$ is the offset angular frequency from the carrier, q_{max} is the maximum charge swing across the tank capacitance C , and $\Gamma_{i_n, \text{rms}}$ is the root-mean-square of Γ_{i_n} , the ISF associated to $\overline{i_n^2}$. Equally well known [3], [5] is that $\Gamma_R(\phi)$, the ISF associated to R in a single-tank LC differential oscillator, has a very simple form:

$$\Gamma_R(\phi) \approx \cos(\phi) \quad (20)$$

i.e., $\Gamma_R(\phi)$ is sinusoidal, and in quadrature to the tank voltage oscillation. Since the current noise generated by R is

$$\overline{i_R^2} = 4k_B T \frac{1}{R} \quad (21)$$

with k_B Boltzmann's constant and T the absolute temperature, from (19)–(21) we obtain immediately that the phase noise generated by R is

$$\mathcal{L}_R(\Delta\omega) = 10 \log \left(\frac{k_B T}{C^2 A^2 \Delta\omega^2} \cdot \frac{1}{R} \right). \quad (22)$$

While these notions are common knowledge for the oscillator designer, a real challenge lies in the derivation of the phase noise caused by the four switch transistors. Our approach, whose effectiveness has already been demonstrated in earlier works [3], [4], [8], will be the following: using the fact that $\Gamma_R(\phi)$ is known, we will relate all MOS ISFs to $\Gamma_R(\phi)$, which will enable us to find analytic expressions for these ISFs as well. Eventually, these will result in simple closed-form phase-noise formulas for MOS current noise sources, and for the whole DS-VCO as well.

IV. TRANSISTOR ISFS IN THE DS-VCO

Following the original definition [5], the ISF of a current noise source is found by injecting into the oscillator a current impulse (with a well-defined area ΔQ , and a phase sweeping the whole oscillation period) in parallel to the current noise source itself. As an example, Fig. 3(a) shows the setup for the calculation of $\Gamma_R(\phi)$, where the current impulse generates a voltage

$$\Delta V_R(\phi) = \frac{\Delta Q(\phi)}{C} \quad (23)$$

across the tank capacitance. By definition, $\Delta V_R(\phi)$ generates $\Gamma_R(\phi)$:

$$\Delta V_R(\phi) \rightarrow \Gamma_R(\phi). \quad (24)$$

At this point, it is worth noting explicitly that, while $\Delta V_R(\phi)$ is actually constant with ϕ , $\Gamma_R(\phi)$ does vary with ϕ , as expected in a time-variant process. To repeat, $\Gamma_R(\phi)$ is in fact already known, and given by (20).

If we now want to determine $\Gamma_{N1}(\phi)$, the ISF associated to the channel current noise of nMOS transistor N1, we inject the same current impulse in parallel to the channel of N1, and calculate the voltage ΔV_{N1} induced again across the tank capacitance, as displayed in Fig. 3(b). By definition,

$$\Delta V_{N1}(\phi) \rightarrow \Gamma_{N1}(\phi). \quad (25)$$

On the other hand, we can rewrite $\Delta V_{N1}(\phi)$ by multiplying and dividing it by $\Delta V_R(\phi)$:

$$\Delta V_{N1}(\phi) = \Delta V_{N1}(\phi) \frac{\Delta V_R(\phi)}{\Delta V_R(\phi)} = \Delta V_R(\phi) \frac{\Delta V_{N1}(\phi)}{\Delta V_R(\phi)}. \quad (26)$$

This, together with (23) and (25), yields $\Gamma_{N1}(\phi)$ as a function of $\Gamma_R(\phi)$:

$$\Gamma_{N1}(\phi) = \Gamma_R(\phi) \frac{\Delta V_{N1}(\phi)}{\Delta V_R(\phi)}. \quad (27)$$

The somewhat hidden assumption behind the above derivation is that $\Gamma_{N1}(\phi)$ should really be determined solely by the voltage induced across C , i.e., that all other capacitors have a negligible influence on the state of the oscillator. In practice, if all parasitic capacitances are much smaller than C , this condition is satisfied.

A. On the Calculation of ΔV_{N1}

The issue of how ΔV_{N1} is calculated in practice is worth a brief discussion, as it is not uncommon that this causes some misunderstanding. The relevant question here is: since it is obvious that the oscillator generates large signals, are we allowed to substitute the real oscillator circuit in Fig. 3(b) with its small-signal equivalent in Fig. 3(c)? Clearly, all noise sources are exceedingly small, and therefore their impact is completely captured by a first-order (i.e., linear) expansion of all device currents around the instantaneous state of the oscillator. However, the values of the linearized active components is a very strong function of the same instantaneous phase of the oscillation, which means that an LTV analysis is called for. If this is done, the approach is rigorously correct, and yields exact results, not just approximations.

B. ISF Expressions

A straightforward analysis on the circuit in Fig. 3(c), hinging on the property that capacitor C presents an infinitesimal impedance to the current impulse, gives $\Delta V_{N1}(\phi)$ as

$$\Delta V_{N1}(\phi) = \frac{\Delta Q(\phi)}{C} \frac{g_{m,N2}(\phi)}{g_{m,N1}(\phi) + g_{m,N2}(\phi)} \quad (28)$$

which, together with (23)–(27), yields the desired expression for $\Gamma_{N1}(\phi)$:

$$\Gamma_{N1}(\phi) = \Gamma_R(\phi) \frac{g_{m,N2}(\phi)}{g_{m,N1}(\phi) + g_{m,N2}(\phi)}. \quad (29)$$

An identical approach yields the values of the other three ISFs:

$$\Gamma_{N2}(\phi) = \Gamma_R(\phi) \frac{g_{m,N1}(\phi)}{g_{m,N1}(\phi) + g_{m,N2}(\phi)} \quad (30)$$

$$\Gamma_{P1}(\phi) = \Gamma_R(\phi) \frac{g_{m,P2}(\phi)}{g_{m,P1}(\phi) + g_{m,P2}(\phi)} \quad (31)$$

$$\Gamma_{P2}(\phi) = \Gamma_R(\phi) \frac{g_{m,P1}(\phi)}{g_{m,P1}(\phi) + g_{m,P2}(\phi)}. \quad (32)$$

Two remarks can be made on the four ISFs above: they have all the same form, despite the fact that the nMOS pair is source-degenerated, while the pMOS is not; and, more interestingly, the nMOS ISFs are independent of the pMOS pair, and *vice versa*. Eventually, these features have the noteworthy consequence that pMOS and nMOS pairs contribute to phase noise independently of each other, as shown in the next two sections.

We conclude the ISF analysis by presenting the expression of $\Gamma_{N1}(\phi)$ when the finite output parasitic conductance g_{ds} of each transistor channel is taken into account (symmetrical expressions are of course found for the three other transistors):

$$\Gamma'_{N1}(\phi) = \Gamma_R(\phi) \times \frac{g_{m,N2}(\phi) + g_{ds,N2}(\phi)}{g_{m,N1}(\phi) + g_{ds,N1}(\phi) + g_{m,N2}(\phi) + g_{ds,N2}(\phi)}. \quad (33)$$

Clearly, (33) is very well approximated by (29) even in deep-submicron CMOS processes.

V. EFFECTIVE TRANSISTOR NOISE

We will assume in the following that the channel current noise generated by a MOS transistor is proportional to its transconductance according to the equation

$$\overline{i_{\text{MOS}}^2}(\phi) = 4k_B T \gamma g_m(\phi) \quad (34)$$

where $\gamma = \gamma_n$ ($\gamma = \gamma_p$) is the channel noise factor for the nMOS (pMOS) transistor.

Since the noise described by (34) is obviously cyclostationary, its associated ISF must be replaced by an effective ISF $\Gamma_{N1,\text{eff}}$ [5], or, equivalently, the numerator in the general phase noise equation (19) is replaced with the mean-square value of the product of the ISF with the noise current density, i.e., by

$$\Gamma_{N1,\text{eff,rms}}^2 \overline{i_{N1}^2} \equiv \frac{1}{2\pi} \int_0^{2\pi} \Gamma_{N1}^2(\phi) \overline{i_{N1}^2}(\phi) d\phi \quad (35)$$

where neither $\Gamma_{N1,\text{eff,rms}}^2$ nor $\overline{i_{N1}^2}$ are uniquely defined, but their product is. Fig. 4 shows a plot of the integrand function over the current commutation between $-\Phi_n$ and Φ_n ; obviously, noise is generated only during current commutations. Therefore, since there are two symmetrical current commutations during one oscillation period, we can rewrite (35) as

$$\frac{1}{2\pi} \int_0^{2\pi} \Gamma_{N1}^2(\phi) \overline{i_{N1}^2}(\phi) d\phi = \frac{1}{\pi} \int_{-\Phi_n}^{\Phi_n} \Gamma_{N1}^2(\phi) \overline{i_{N1}^2}(\phi) d\phi. \quad (36)$$

A very similar integral has already been evaluated in [3]; following the same approach, and employing (2) and (8), it is easily found that

$$\begin{aligned} \frac{1}{\pi} \int_{-\Phi_n}^{\Phi_n} \Gamma_{N1}^2(\phi) \overline{i_{N1}^2}(\phi) d\phi &= \frac{2}{\pi} k_B T \gamma_n \frac{I_B}{A} \\ &= \frac{\gamma_n}{2} k_B T \frac{1}{R}. \end{aligned} \quad (37)$$

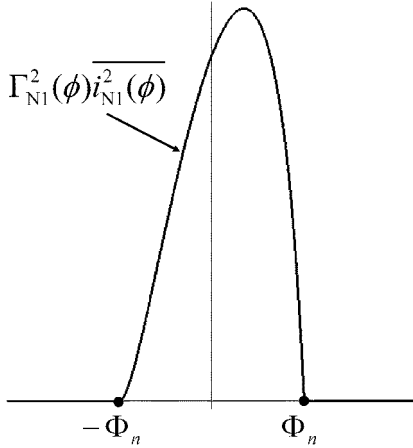


Fig. 4. Effective current noise density for nMOS switch $N1$.

As was already the case in the SS-VCO, almost nothing is left of the individual features of transistor $N1$ in its effective noise contribution to phase noise: apart from γ_n , its width, length, and gain factor do not figure in (37). No matter what $N1$ looks like, its effective noise is always exactly proportional to the tank resistance noise, the only limiting assumption being that of fast current switching (i.e., the MOS pair must have a high enough gain).

Because of symmetry, the effective noise generated by nMOS transistor $N2$ is obviously also given by (37). Moreover, we have already noticed that all pMOS equations are identical in form to the respective nMOS equations, which means that the effective noise contribution of pMOS transistor $P1$ can be written without effort as

$$\begin{aligned} \frac{1}{2\pi} \int_0^{2\pi} \Gamma_{P1}^2(\phi) \overline{i_{P1}^2(\phi)} d\phi &= \frac{1}{\pi} \int_{-\Phi_p}^{\Phi_p} \Gamma_{P1}^2(\phi) \overline{i_{P1}^2(\phi)} d\phi \\ &= \frac{\gamma_p}{2} k_B T \frac{1}{R}. \end{aligned} \quad (38)$$

Since the contribution from $P2$ is again given by (38), all MOS effective noise contributions to phase noise have been found.

VI. PHASE NOISE IN THE DS-VCO

Using (19), (35), and (37)–(38), together with (22), we can at last present the phase noise equation for the DS-VCO accounting for both tank and switch noise (i.e., the minimum phase noise that can be expected from this oscillator, since such noise sources are unavoidable, once the tank- Q has been fixed):

$$\mathcal{L}_{DS}(\Delta\omega) = 10 \log \left[\frac{k_B T}{C^2 A_{DS}^2 R \Delta\omega^2} \left(1 + \frac{\gamma_n + \gamma_p}{2} \right) \right] \quad (39)$$

where we have defined $A_{DS} = A$ for later use. Equation (39), which has been extensively verified through a large number

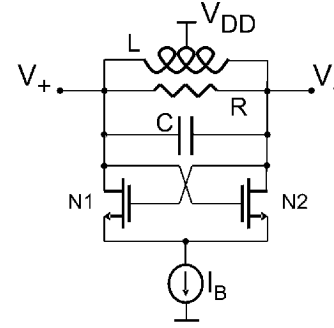


Fig. 5. Simplified schematic view of the SS-VCO.

of numerical spectreRF simulations,² is surprising on two accounts: first, if $\gamma_p = \gamma_n$, the pMOS pair and the nMOS pair contribute equally to phase noise, independently of their respective (peak) transconductances, and of the relative values of Φ_n and Φ_p [i.e., Φ_n and Φ_p do not have to be identical, as long as current switching can be considered square-wave-like, which is the necessary condition for (2)]. Secondly, if we assume that γ_n and γ_p have their ideal long-channel value of $2/3$, as much as 60% of the phase noise is generated by the tank resistance, and only 40% by all switches together. Thus, contrary to what was previously believed (see, e.g., the otherwise excellent treatment in [9]), and as is the case in the SS-VCO as well, tank losses are the major contributors to phase noise in the DS-VCO, at least in the ideal design considered so far. As a matter of fact, values for γ_n or γ_p close to $2/3$ do not have to be wildly optimistic, since no large overdrive is usually needed by the MOS pairs for completing current switching, which means that the transistors are actually behaving rather like “long-channel” devices (or, more appropriately, “low-electric-field” devices [10]), where the ideal MOS transistor equations apply.

VII. DS-VCO VERSUS SS-VCO

It is very interesting, from both a theoretical and a practical point of view, to compare the performance of the DS-VCO with that of the SS-VCO, whose simplified schematic is shown in Fig. 5. The phase noise equation for the SS-VCO has been found in previous works [1], [3], and, with the notation adopted in this paper, is written as³

$$\mathcal{L}_{DS}(\Delta\omega) = 10 \log \left[\frac{k_B T}{C^2 A_{SS}^2 R \Delta\omega^2} (1 + \gamma_n) \right] \quad (40)$$

where A_{SS} is the oscillation amplitude between V_+ and V_- for the SS-VCO. It is well-known that, for a square-wave tank current, A_{SS} is given by

$$A_{SS} = \frac{2}{\pi} R I_B \quad (41)$$

²The reader might wonder why (39) has not been conjectured earlier from simulations results; very likely, the reason is that (39) does not apply if parasitic capacitances play a dominant role, as will be discussed in Section IX.

³The analysis in [3] was based on a two-tank SS-VCO design; the adaptation of those results to a single-tank design with the same component values as for the DS-VCO is, however, devoid of major difficulties.

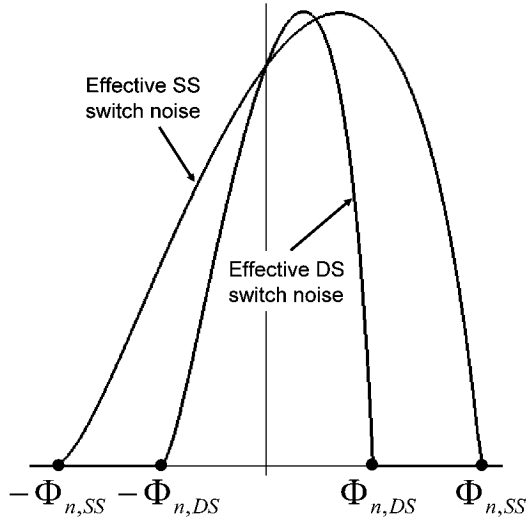


Fig. 6. Effective current noise density for nMOS switch $N1$ in the DS-VCO and SS-VCO, respectively.

that is, A_{SS} is only half as high as A_{DS} for the same LC -tank and bias current. Let us now assume that $\gamma_n = \gamma_p$, that γ_n is the same in (39) and (40), and that DS-VCO and SS-VCO have the same bias current; then, $\gamma_n = (\gamma_n + \gamma_p)/2$, and the only difference between (39) and (40) lies in the different oscillation amplitude in the two oscillators, which immediately results in the DS-VCO having a 6-dB lower phase noise than the SS-VCO:

$$\mathcal{L}_{DS}(\Delta\omega) = \mathcal{L}_{SS}(\Delta\omega) - 6 \text{ dB}. \quad (42)$$

This equation is very remarkable because of the following argument: while we would indeed anticipate a 6-dB signal-level advantage in favor of the DS-VCO, on account of the double oscillation amplitude allowed by the use of a second switch pair, at the same time we would also predict at least some noise deterioration in the DS-VCO core, since there are two (noisy) switch pairs in the DS-VCO, compared to only one in the SS-VCO. Therefore, we would reasonably expect a lower phase noise in the DS-VCO, but not exactly a whole 6 dB lower than in the SS-VCO, as this would be equivalent to demand that there should not be any noise penalty associated to the presence of the second switch pair.

In fact, most surprisingly, this is precisely what happens: it is easy to check that (37) and (38) entail that each switch in the DS-VCO generates only half as much noise as each switch in the SS-VCO [3], so that the total switch noise is the same in both oscillators. This is a very remarkable result, and quite counter-intuitive at first; nevertheless, there is a very intuitive explanation for it. Fig. 6 shows the effective current noise density (i.e., current noise density times the corresponding ISF squared) for two nMOS switches, one belonging to the DS-VCO and one to the SS-VCO, and both having the same peak transconductance value. From Fig. 6 it is immediately clear that having a double oscillation amplitude in the DS-VCO is not just beneficial for the signal level, but it is for the noise level as well. In fact, a double oscillation amplitude halves the value of Φ_n (and of Φ_p ,

of course) in the DS-VCO, as clear from (8), which means that the DS-VCO switch only has half as much time as the SS-VCO switch to generate noise. The area below the DS-VCO switch noise curve is almost exactly half the area below the SS-VCO switch noise curve (exactly half if current commutations are switch-like); since these areas are proportional to the effective noise generated by the switches, as shown by (35), it is clear that each DS-VCO switch generates only half as much noise as each SS-VCO switch. This noteworthy result is yet another compelling proof of the necessity of adopting an LTV analysis in the study of phase noise in oscillators.

VIII. PHASE-NOISE FIGURE-OF-MERIT

It is often interesting to compare not only the phase noise displayed by different oscillators, but also the phase noise normalized to the power consumption, i.e., the phase-noise figure-of-merit (FoM). The commonly used definition of FoM is [11]

$$\text{FoM} = -\mathcal{L}(\Delta\omega) + 20 \log\left(\frac{\omega}{\Delta\omega}\right) - 10 \log(P_{\text{mW}}) \quad (43)$$

where P_{mW} is the power consumption expressed in mW.

If we double the current consumption in the SS-VCO, A_{SS} doubles as well, becoming equal to A_{DS} . This, together with (39) and (40), results in both oscillators displaying the same phase noise. Further, we notice that, even if the SS-VCO has doubled the bias current, it (ideally) requires only half as high minimum power supply voltage V_{dd} , compared to the DS-VCO. This is because the SS-VCO oscillation swings symmetrically above and below V_{dd} , while it swings between V_{dd} and ground in the DS-VCO. If the oscillation amplitude is the same in both oscillators, V_{dd} in the SS-VCO is allowed to drop to half its value in the DS-VCO, assuming for simplicity that no overdrive for the tail bias circuit is needed in either oscillator. This means that not only the phase noise, but also the minimum power consumption is (ideally) the same in the DS-VCO and SS-VCO, which shows that the two oscillators are capable of the same maximum FoM. Compared to the SS-VCO, the DS-VCO needs only half as much bias current, but requires at the same time a double power supply voltage.

It is worth remarking explicitly that, if the DS-VCO (SS-VCO) is working in the current-limited region, doubling the current consumption keeping V_{dd} constant lowers the phase noise by 6 dB, while the current consumption increases by 3 dB only. This should be kept in mind, in order to use (43) in a fair way. In particular, the FoM should be calculated for the minimum V_{dd} allowing current-limited operations; if now the bias current is doubled, V_{dd} must be (approximately) doubled as well, in order to avoid voltage-limited operations. This, in turn, increases power consumption by 6 dB, resulting in a constant FoM, as desired.

It should not, however, be forgotten that the above reasoning neglects second-order effects, such as the presence of bias circuit noise, that may have a relevant impact on the total phase noise performance.⁴

⁴The phase noise caused in the SS-VCO by the white noise from the tail current source has been studied in [3]; the application to the DS-VCO case is straightforward, and is therefore not repeated here.

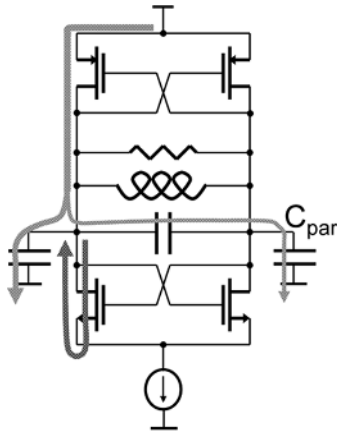


Fig. 7. Different paths for nMOS and pMOS noise in the DS-VCO.

A. Ideal FoM Values in DS-VCO and SS-VCO

Making use of (2) and (39), noticing that the maximum value attainable by A_{DS} is V_{dd} , and employing the usual expression $Q = \omega RC$ for the quality factor Q of the tank, the maximum FoM achievable by a DS-VCO is found as

$$\text{FoM}_{\text{DS,max}} = -10 \log \left[\frac{10^3 \pi k_B T}{4 Q^2} \left(1 + \frac{\gamma_n + \gamma_p}{2} \right) \right] \quad (44)$$

which shows that $\text{FoM}_{\text{DS,max}}$ is dependent solely on the tank- Q of the oscillator (assuming γ_n and γ_p constant). Equation (44) is useful to estimate how close the performance of a real design is to the limits imposed by the technology. It is easy to show that the maximum FoM achievable by an SS-VCO has the same value as $\text{FoM}_{\text{DS,max}}$ if $\gamma_n = \gamma_p$.

IX. IMPACT OF PARASITIC TANK CAPACITANCES

If there are parasitic capacitances C_{par} between tank outputs and ground, as in Fig. 7, the perfect symmetry between pMOS pair and nMOS pair breaks down. This is because the pMOS sources are not floating, which means that pMOS noise can now find a path through the tank to ground, while the nMOS noise is still totally rejected by cascoding from the tail bias, assuming negligible parasitic capacitance at the nMOS sources (of course, pMOS and nMOS swap roles if top biasing is adopted instead of tail biasing). Further, some of the charge on C_{par} can now discharge through the pMOS switch, lowering the effective tank- Q .

If C_{par} is large, the impact of the pMOS switches becomes dominant, while the nMOS noise remains constant. In this respect, the SS-VCO is a more robust choice, since its phase noise is not affected by C_{par} (assuming that the common nMOS source is truly floating). Thus, if the oscillation frequency is high, relative to the technology used, or if it is otherwise unfeasible to implement a (mainly) floating tank capacitor, an SS-VCO is likely to result in a higher FoM than the equivalent DS-VCO.

As an example of the impact of C_{par} in the DS-VCO, Fig. 8 shows a couple of spectreRF phase-noise simulations, one in presence of an ideal floating tank capacitance, the other when C_{par} constitutes 50% of the total tank capacitance. The phase noise deterioration caused by C_{par} is as high as 4.4 dB, with

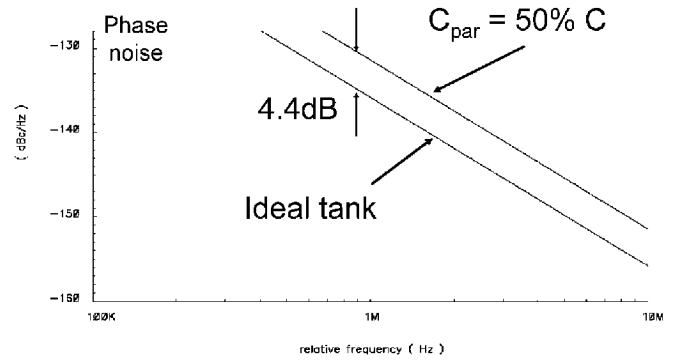


Fig. 8. SpectreRF phase noise simulations for the DS-VCO. When the tank capacitance is largely made of parasitic (grounded) capacitances, the phase noise deterioration may be large.

pMOS switches becoming the main contributors to phase noise (which was found to be the case in previous DS-VCO designs).

In general, it should be mentioned that the amount of phase noise degradation depends on the size of the pMOS transistors as well; however, these simple simulation examples show very clearly how critical it is to minimize the parasitic tank capacitance, if an optimal DS-VCO phase-noise performance is desired.

X. TAIL BIAS CIRCUIT

It is common knowledge that the design of the tail bias transistor is not without problems. In order to minimize its $1/f$ noise contribution to phase noise, its length should be well above the minimum allowed; however, it is also very desirable to keep its drain area (i.e., its width) as small as possible, since a large parasitic capacitance at the common nMOS-pair source has a large negative impact on the overall oscillator performance. However, a long and narrow transistor would need a large drain-source voltage to deliver the required bias current, which would leave a highly reduced voltage headroom for the actual oscillation signal.

One solution to this problem is to accept a large transistor, interposing at the same time an inductor between the common nMOS-pair source and the bias-transistor drain. If the inductor is resonating at double the oscillation frequency with the parasitic capacitance at the common nMOS-pair source, this technique greatly reduces both $1/f$ and white noise from the tail bias transistor [12]. It is, however, associated with two momentous drawbacks: it is narrowband in nature, and the extra inductor approximately doubles the area consumption of the VCO, a fact which is not without importance in today's (and even more tomorrow's) very expensive IC processes.

Following a suggestion by Dr. K. Christensen [13] at Intel in Skovlunde (Copenhagen, Denmark), we have addressed the $1/f$ issue in the tail bias circuit by replacing the single bias transistor with the cascode pair in Fig. 9. Transistor M_{T2} is designed with small width and minimum length, thereby minimizing its parasitic drain capacitance; of course, M_{T2} does generate a large $1/f$ noise, but this is totally rejected by M_{T1} , which presents a very large impedance at low frequencies. M_{T1} itself, on the other hand, is allowed to be very long and wide, and therefore generates a negligible $1/f$ noise while requiring a low drain-source

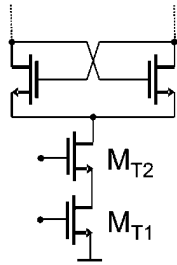


Fig. 9. Cascode tail bias circuit for $1/f$ bias noise minimization.

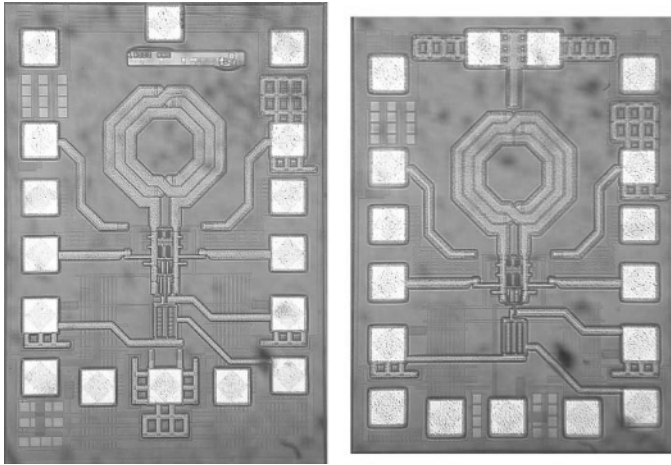


Fig. 10. Die photographs of DS-VCO (left) and SS-VCO.

voltage. In this way, the $1/f$ noise from the tail bias is minimized in a broadband fashion without the need of extra on-chip or off-chip [14] inductors, at the (slight) drawback of a somewhat increased DC bias voltage at the drain of M_{T2} , needed to keep both tail transistors in the active region.

XI. MEASUREMENT RESULTS

The DS-VCO has been realized in a four-metal $0.35\text{-}\mu\text{m}$ CMOS process with thick top metal (Al) layer and MIM capacitors. The inductor has an estimated inductance of 2.6 nH , for a Q of approximately 11 at 2.3 GHz . Coarse tuning is achieved through switchable MIM capacitors, while yet another MIM capacitor sets the center oscillation frequency to 2.3 GHz . The availability of high- Q MIM capacitors has in fact been crucial for the optimal design of the DS-VCO, which requires floating tank capacitors (see Section IX). Fine tuning is implemented with accumulation-MOS varactors.

As can be expected from the discussion in Section IX, all parasitic tank capacitances have been carefully minimized; in particular, no substrate shield has been placed beneath the inductor. The open-drain buffers delivering the differential tank oscillation to the measurement setup do introduce parasitic capacitances in parallel to the tank outputs; these, however, have a negligible impact on phase noise, according to simulations (and to the measurements shown in the following). Thus, the on-chip buffers (or, possibly, the mixer stage) driven by the VCO in real applications are not expected to deteriorate noticeably the phase noise performance of the DS-VCO.

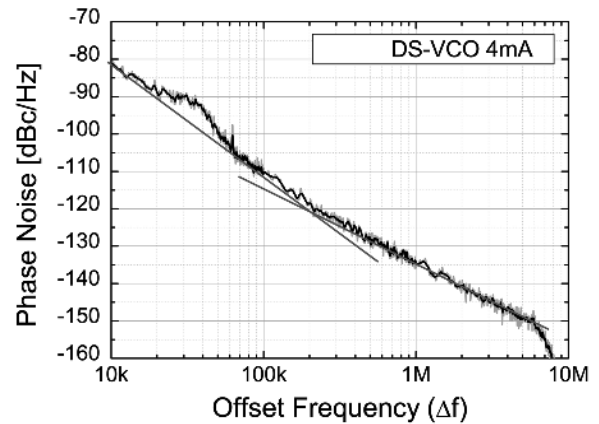


Fig. 11. Measured phase noise for the DS-VCO, with 2.3-GHz carrier frequency, 4-mA bias current, and 2.5-V power supply.

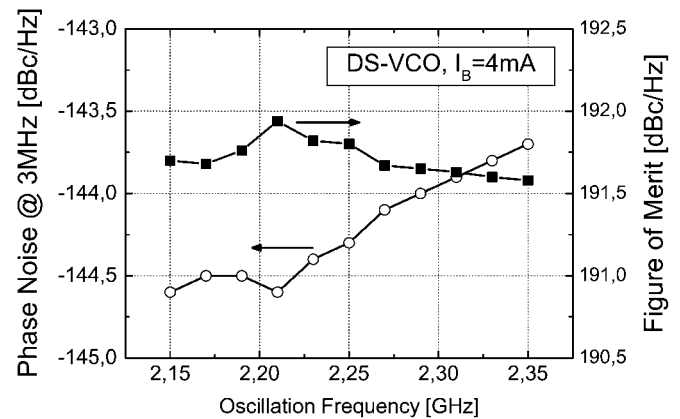


Fig. 12. Measured phase noise and FoM for the DS-VCO across the tuning range, with 4-mA bias current and 2.5-V power supply.

A reference SS-VCO has been implemented as well, using the same tank and tail bias circuit as in the DS-VCO; it can be noted that relative phase noise measurements between DS-VCO and SS-VCO, being independent of the tank- Q , are much more robust than absolute measurements, given the uncertainties on the actual Q value. Fig. 10 shows a die photo of both VCOs.

The two VCOs are tunable between 2.15 and 2.35 GHz in four 75-MHz overlapping bands. A representative phase noise measurement for the DS-VCO is visible in Fig. 11, taken at an oscillation frequency of 2.3 GHz , with 4-mA bias current and 2.5-V power supply. The phase noise at 3-MHz frequency offset is approximately -144 dBc/Hz , while the $1/f$ noise corner is slightly higher than 200 kHz . The roll-off for offset frequencies higher than 5 MHz is an artifact of the open-loop delay-line phase-noise measurement technique here employed.

Phase noise and FoM for the DS-VCO across the tuning range are displayed in Fig. 12. The phase noise varies approximately 1 dB across the tuning range, while the FoM varies less than 0.5 dB , between 191.5 dBc/Hz and 192 dBc/Hz , the highest to date for DS-VCOs to the best of our knowledge. Assuming $Q = 11$, this is at most only 2 dB lower than $\text{FoM}_{\text{DS,max}} = 193.5\text{ dBc/Hz}$ as given by (44), which shows that the phase noise performance of the DS-VCO is indeed (close to) optimal [7].

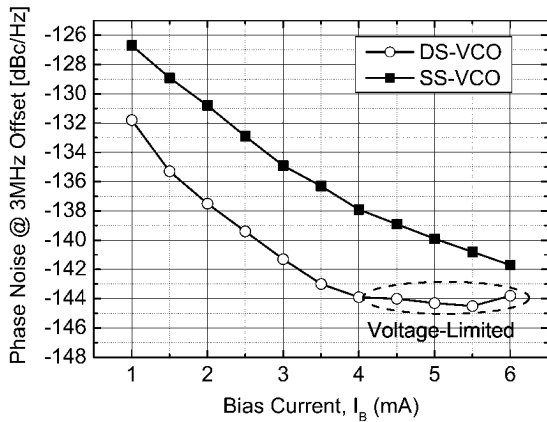


Fig. 13. Measured phase noise difference between DS-VCO and SS-VCO at 3-MHz frequency offset, with 4-mA bias current and 2.5-V power supply.

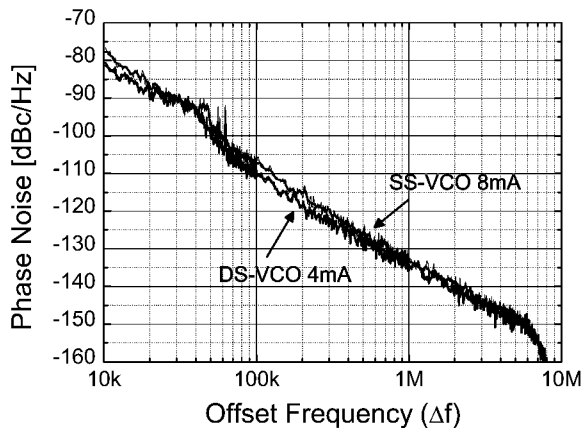


Fig. 14. Phase noise plots for both DS-VCO and SS-VCO, when the SS-VCO bias current is doubled.

It is of course of the highest interest to assess to what extent the theoretical phase noise difference between DS-VCO and SS-VCO is confirmed by measured data. The comparison between the two VCOs working in the current-limited region can be seen in Fig. 13, with the phase noise measured at 3-MHz offset frequency as a function of the bias current. At the low bias current of 1 mA, the difference in favor of the DS-VCO is ~ 5 dB, which increases to 6–6.5 dB for higher bias currents, until the DS-VCO becomes voltage-limited. In average, this is almost exactly the 6-dB phase noise difference expected from theory.

Finally, Fig. 14 shows the overlaid phase noise plots of DS-VCO and SS-VCO, when the SS-VCO bias current is doubled (i.e., set to 8 mA). Ideally, the two VCOs should display the same phase noise, as explained in Section VIII; however, the SS-VCO is 1–2 dB noisier, depending on the offset frequency; on the other hand, it should be considered that a higher bias current results in a higher tail current noise and less switch-like current commutations, i.e., in a larger departure from ideal oscillator operations.

XII. CONCLUSION

The exact phase noise equation for the LC-tank double-switch-pair VCO (DS-VCO), accounting for the noise contri-

butions from tank losses and core transistors current noise, has been derived using the Impulse Sensitivity Function theory of phase noise, together with a linear-time-variant circuit analysis. This has made possible the fair comparison of the DS-VCO with the other very popular LC VCO topology, the single-switch-pair VCO (SS-VCO); surprisingly, the ideal DS-VCO shows a 6-dB lower phase noise for the same current consumption, while the maximum phase-noise figure-of-merit (FoM) is the same in both VCOs. However, if non-negligible parasitic capacitances are found at the tank outputs, the phase-noise performance of the DS-VCO may be seriously degraded, while that of the SS-VCO remains unaffected.

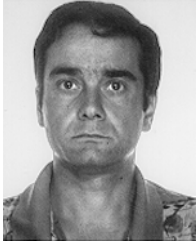
The two VCOs have been implemented in a four-metal (Al) 0.35- μm CMOS process with thick top metal layer and MIM capacitors. A cascode-pair tail current source minimizes the $1/f$ tail noise without any area consumption overhead. The DS-VCO shows a minimum FoM of 191.5 dBc/Hz across the tuning range (2.15–2.35 GHz), and the phase noise difference between the two VCOs is almost exactly the one expected from the theory developed in this work.

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