MOS Transistor Modeling for RF IC Design

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ABSTRACT

The design of radio-frequency (RF) integrated circuits (ICs) in deep-submicron CMOS processes requires accurate and scalable compact models of the MOS transistor that are valid in the GHz frequency range and beyond. Unfortunately, the currently available compact models give inaccurate results if they are not modified adequately. This paper presents the basis of the modeling of the MOS transistor for circuit simulation at RF. A physical and scalable equivalent circuit that can easily be implemented as a Spice subcircuit is described. The small-signal and noise models are discussed and measurements made on a 0.25µm CMOS process are presented that validate the RF MOST model up to 10GHz.

I. INTRODUCTION

Today, deep-submicron CMOS processes typically reach the 50 GHz f_t region and offer low noise figures [1], making them a serious alternative for RF circuits integration for applications in the GHz frequency range. In addition, CMOS offers VLSI capabilities allowing for a high level of integration. The feasibility of RF CMOS circuit integration has clearly been demonstrated. There is no doubt that in the coming years new wireless products will appear with CMOS as the technology used for the integration of the RF portion. Nevertheless, the design of RF circuits for real products remains a challenge due to the strong constraints on power consumption and noise that leave very little margins. It is therefore crucial to be able to accurately predict the performance of RF CMOS circuits. Although good results can be obtained at low frequency (typically below 100 MHz), the simulation of RF circuits in the GHz frequency range with the available compact MOS models such as BSIM3v3 [2], MOS Model 9 [3] or EKV [4] without consideration of all the parasitic components, gives inaccurate or even wrong results. These models have therefore to be enhanced in order to be used for RF CMOS IC design.

This paper describes the basis of MOST modeling for circuit simulation at RF. Section II presents the modeling of the MOS transistor at RF with emphasis on the small-signal operation in strong inversion and in saturation. Section III discusses the noise properties of the MOST at high-frequency (HF).

II. SMALL-SIGNAL MODEL

A cross-section of a single finger MOS transistor is presented in Fig. 1 together with the corresponding simplified equivalent circuit [5]. The latter accounts for the most important physical effects and therefore represents a good trade-off between accuracy and complexity. It has proven to be sufficient for most RF circuit simulations [5]. It can easily be implemented in a Spice simulator as a sub-circuit (SUBCKT), where all the extrinsic components are pulled out of the MOS transistor compact model, so that the MOS transistor symbol only represents the intrinsic part of the device. This allows to have access to internal nodes and model extrinsic components such as series resistances and overlap capacitances in a different way than what is available in the complete compact model. The source and drain series resistors are added outside the MOS model since the series resistances internal to the compact model are only “soft” resistances embedded in the expression used to calculate the drain current to account for the dc voltage drop across the source and drain resistances. They do not add any poles and are therefore invisible for ac simulation. The gate resistance is usually not part of the MOST compact model, but plays a fundamental role in RF circuits and has therefore to be added too.

The substrate resistors R_{dsb}, R_{sb} and R_{db} have been added to account for the signal coupling through the substrate [5]. At HF, the impedances of the junction capacitances become small enough so that the RF signal at the drains couple to the nearby source diffusions and to the bulk through the junction capacitances and the substrate. The doping levels of deep-submicron CMOS processes are sufficiently high so that the substrate can be considered as purely resistive in the GHz frequency range. Resistance R_{dsb} represents all the coupling occurring from drains to sources, whereas R_{sb} and R_{db} correspond to the coupling from source and drain to bulk. R_{dsb} is the result of the parallel connection of all the individual source-to-drain resistances corresponding to each finger. R_{sb} and R_{db} also result from the parallel connection of all individual source-to-bulk and respectively drain-to-bulk resistances. Their scaling strongly depends on the geometry of the bulk contact.

The source-to-bulk and drain-to-bulk diodes are also part of the compact model but their anodes are connected to the same substrate node. The diodes internal to the compact model are therefore also turned off and two external diodes D_{sb} and D_{db} are added in order to account for the substrate resistance R_{dsb} existing between the source and the drain diffusions.

The quasi-static (QS) small-signal circuit corresponding to the equivalent circuit shown in Fig. 1 in saturation is depicted in Fig. 2 together with the definition of the voltage-controlled current sources (VCCS) I_m and I_{ms}. The capacitances C_{gs}, C_{gd} and C_{gb} represent the sum of the intrinsic and overlap capacitances, whereas C_{sb} and C_{db} correspond to the sum of the intrinsic and junction capacitances. The slope factor n used in Fig. 2 is equal to $n = g_{ms}/g_m = g_{mb}/g_m + 1$ and depends on the gate-to-bulk voltage [6][7]. It typically ranges from 1.6 in weak inversion to 1.3 in strong inversion for an n-channel transistor (1.4 to 1.2 for p-channel) [6][7]. The gate transadmittance is given by

$$Y_m = g_m \cdot (1 - j\omega \cdot \tau_{qs}) \quad (1)$$

where the bias-dependent time constant τ_{qs} is related to the transcapacitances and transconductances according to

$$\tau_{qs} = C_m/g_m = C_{ms}/g_{ms}. \quad (2)$$

The subcircuit of Fig. 1 has been used to build a scalable RF MOS model using adequate scaling rules [5][8]. The compact model EKV v2.6 has been chosen for the intrinsic part (Mi in the schematic of Fig. 1). The Y-parameters have been obtained from the measured S-parameters after a two-step de-embedding procedure. DC parameters, including the drain-to-source series resistance parameter R_{dsw}, have been extracted from dc measurements. Most parameters specific to the RF part have been extracted using the methodology presented in [8]. A comparison between measured and simulated Y-parameters versus frequency is presented in Fig. 3. The simulations show a very good match with measurements including the output admittance y_{22}. Note that the discrepancies in $Re\{y_{12}\}$ are not critical since y_{12} is dominated by its imaginary part corresponding approximately to ωC_{gd}. Similar results have been obtained for other operating points and other device geometries using the same scalable model [5].
The performance of RF devices is often evaluated by looking at their transit frequency f_t which is given by

$$f_t \cong g_m/(2\pi \cdot C_{gg}) \quad (3)$$

where $C_{gg} = C_{gs} + C_{gd} + C_{gb}$ is the total gate capacitance. Since g_m is proportional to W_{eff}/L_f and C_{gg} is proportional to $W_{eff} \cdot L_f$, f_t is inversely proportional to L_f^2. Note that this is only true at low lateral electrical field where there is no velocity saturation. If the carriers' velocity is saturated, the f_t then only scales as $1/L_f$.
The transit frequency f_t measured for two n-channel transistors having different gate length are plotted in Fig. 4 versus the inversion factor I_D/I_{spec}, where $I_{spec} = 2n\beta U_T^2$ is the specific current delimiting the regions of weak and strong inversion with $U_T = kT/q$ [7]. The inversion factor is a useful way to characterize the state of inversion of the channel of a MOST in saturation: it is much larger than one in strong inversion, close to unity in the moderate inversion and much smaller than one in weak inversion [7]. Note that I_{spec} depends on the transistor geometry according to $\beta = \mu_{eff} C'_{ox} \; W_{eff}/L_f$ [7]. The measurements are compared to simulations using the subcircuit of Fig. 1 with EKV v2.6 for the compact model. The simulation results agree well with the measured data over a wide bias range. The peaking of f_t is due to the transistor leaving saturation and entering into the triode region. At this point the transconductance starts to saturate or even decrease while the gate-to-drain intrinsic capacitance starts to increase making the f_t reach a maximum and then sharply decrease.

III. NOISE MODEL

The different noise sources in the MOS transistor are shown in Fig. 5 together with their power spectral densities (PSD). They include: the noise at the drain S_{ind}, composed by the channel thermal noise $4kT \cdot G_{nch}$ and the flicker noise $g_m^2 \cdot K_f/(C'_{ox} W_{eff} L_f f^{\alpha})$, the terminal resistances thermal noise S_{vnrg}, S_{inrs}, S_{inrd} and the substrate resistances thermal noise S_{inrsb}, S_{inrdb} and S_{inrdsb}. The flicker noise mainly affects the low-frequency performance of the device and can be ignored at high-frequency. In addition to the channel thermal noise at the drain, at high frequency the local noise sources within the channel are capacitively coupled to the gate and generate an induced gate noise S_{ing} [6][9].
Although all the noise sources contribute to the total noise at high-frequency, the dominant contribution still comes from the channel thermal noise having a PSD given by [6][7]

$$S_{ind} = 4kT \cdot G_{nch} \qquad with \qquad G_{nch} = \gamma \cdot g_{ms} \quad (4)$$

where $k = 1.38 \times 10^{-23} J/K$ is the Boltzman constant and T the absolute temperature in K. G_{nch} is the channel thermal noise conductance, g_{ms} the source transconductance (which reduces to the channel conductance in the linear region). γ is a bias dependent noise excess factor, which for long-channel devices is equal to unity in the linear region. In saturation γ is defined as γ_{sat} and it varies from 0.5 in weak inversion to $2/3$ in strong inversion [6][7]. γ_{sat} is related to another factor defined as [9]

$$\alpha_{sat} \equiv g_m \cdot R_{Nin} = G_{nch}/g_m = g_{ms}/g_m \cdot \gamma_{sat} = n \cdot \gamma_{sat}. \quad (5)$$

α_{sat} is a good figure of merit to compare the thermal noise performance of different transconductors. α_{sat} is proportional to γ_{sat} and is typically equal to unity in strong inversion. For short-channel devices, γ_{sat} (α_{sat}) might become larger than the long-channel value $2/3$ ($n \cdot 2/3$). This is due to velocity saturation and hot electrons [9][11].

At high-frequency, the local channel voltage fluctuations due to thermal noise couple to the gate through the oxide capacitance and cause an induced gate noise current to flow [6][9]. In saturation, this noise current can be modeled by a noisy current source i_{ng} connected in parallel to C_{gs} and having a PSD given by [10]

$$S_{ing} = 4kT \cdot G_{ng}(\omega) \qquad with \qquad G_{ng}(\omega) = \delta \cdot \omega^2 C_{gs}^2/(5g_{ms}) = \beta_{sat} \cdot \omega^2 C_{gs}^2/g_m \tag{6}$$

where δ is a bias dependent factor that is equal to $4/3$ for a long-channel device in saturation and $\beta_{sat} \equiv \delta/(5n)$ [5][10]. Since the physical origin of the induced gate noise is the same as for the channel thermal noise at the drain, the two noise sources i_{nd} and i_{ng} are partially correlated [9][10]. For a long-channel transistor in strong inversion and in saturation, the correlation coefficient is $c = jc_g$ with $c_g \cong 0.4$ [9][10]. For short-channel devices, device noise simulations have shown that the correlation factor c remains mainly imaginary with a value slightly smaller than the long-channel value [12][13]. The induced gate noise is not implemented in compact models yet (except for MOS Model 9 that includes the induced gate noise but without the correlation).

As shown in Fig. 6, a noisy twoport can be represented by the same noiseless twoport and an input noise voltage source v_n having a PSD $S_v = 4kTR_v$ and an input noise current source i_n having a PSD $S_i = 4kTG_i$. S_v and S_i depend on the internal physical noise sources and are therefore generally correlated. This correlation is accounted for by the correlation admittance Y_c defined as

$$Y_c \equiv \overline{i_n v_n^*}/\overline{v_n^2} = G_c + jB_c\,. \tag{7}$$

A complete description of the noise always requires four parameters: R_v, G_i, G_c and B_c. The noise parameters can be evaluated from a simplified small-signal circuit where it is assumed that $R_{dsb} << R_{sb}$ and $R_{dsb} << R_{db}$ leading to a single substrate resistance $R_{sub} = R_{sb} /\!/ R_{db}$. The capacitances C_{bs} and C_{bd} are also neglected resulting in

$$R_v \cong \alpha_{sat}/g_m \cdot D_c \qquad G_i \cong \alpha_{sat}/g_m \cdot (\omega C_{gs})^2 \cdot \psi \qquad G_c \cong \omega^2 R_g C_{gs}^2 \cdot \psi/D_c \qquad B_c \cong \omega C_{gs} \cdot \chi/D_c \tag{8}$$

where $D_c \cong 1 + \alpha_g + \alpha_{sub}$. α_g is the noise PSD of the gate resistance normalized to the input referred channel noise and α_{sub} is the ratio of the output referred substrate resistance noise PSD to the output referred channel noise

$$\alpha_g \equiv g_m R_g/\alpha_{sat} \qquad \alpha_{sub} \equiv g_{mb}^2 R_{sub}/(\alpha_{sat} g_m)\,. \tag{9}$$

Parameters ψ and χ in (8) account for the induced gate noise and its correlation to the drain noise according to

$$\psi \cong 1 + \alpha_{sub} + \beta_{sat}/\alpha_{sat} + 2c_g\sqrt{\beta_{sat}/\alpha_{sat}} \cong 1.83 \qquad \chi \cong 1 + \alpha_{sub} + c_g\sqrt{\beta_{sat}/\alpha_{sat}} \cong 1.4\,. \tag{10}$$

Both variables ψ and χ reduce to unity when the substrate noise and the induced gate noise are ignored. Eqn. (8) shows that the induced gate noise does not affect R_v, but contributes to G_i, G_c and B_c through the factors ψ and χ. On the other hand, substrate noise may typically contribute to 20% of R_v whereas R_g typically contributes to about 5%. The numerical values given in (10) correspond to a long-channel device in strong inversion and in saturation with $\alpha_g \cong 0.06$, $\alpha_{sub} \cong 0.21$ and $D_c \cong 1.27$.

The HF noise is often characterized by a set of four other parameters, namely: the minimum noise factor F_{min} (or minimum noise figure $NF_{min} \equiv 10\log(F_{min})$), the input referred noise resistance R_v and the optimum source admittance $Y_{opt} \equiv G_{opt} + jB_{opt}$ for which the minimum noise figure is obtained. Parameters F_{min}, G_{opt} and B_{opt} can be expressed in terms of the twoport noise parameters R_v, G_i, G_c and B_c

$$F_{min} = 1 + 2R_v \cdot (G_{opt} + G_c) \qquad G_{opt} = \sqrt{G_i/R_v - B_c^2} \qquad B_{opt} = -B_c\,. \tag{11}$$

G_{opt} and B_{opt} can written in terms of device parameters as

$$G_{opt} \cong \omega C_{gs} \cdot \sqrt{D_c\psi - \chi^2}/D_c \cong \omega C_{gs} \cdot 0.47 \qquad B_{opt} \cong \omega C_{gs} \cdot \chi/D_c \cong \omega C_{gs} \cdot 1.1\,. \tag{12}$$

From (12), it is seen that the source susceptance required for noise matching is about 1.1 times larger than that required for power matching. For $\omega R_g C_{gs} << 1$, F_{min} simplifies to

$$F_{min} \cong 1 + 2R_v \cdot G_{opt} \cong 1 + (\omega C_{gs})/g_m \cdot 2\alpha_{sat}\sqrt{D_c\psi - \chi^2} \cong 1 + 1.04 \cdot \omega/\omega_t\,. \tag{13}$$

It can be shown that F_{min} and G_{opt} are both strongly sensitive to R_g and to the induced gate noise, but not to R_{sub} nor to the correlation coefficient c_g. on the other hand, B_{opt} is not sensitive to R_g and R_{sub} nor to the induced gate noise but it is strongly dependent on c_g.

IV. CONCLUSION

A simple scalable RF MOS model that can easily be implemented in a Spice subcircuit has been presented. It includes important effects such as gate resistance, intra-device substrate coupling, thermal noise and induced gate noise. The model has been successfully validated over frequency up to 10 GHz, over geometry and over bias on a 0.25 µm CMOS process for both n- and p-channel devices.

For some RF applications in the GHz range using future deep-submicron processes, it may be advantageous to move the operating point of the RF devices from strong inversion to moderate inversion to take advantage of the higher g_m/I_D ratio and therefore of the higher current efficiency and benefit from the lower electrical fields within the transistor. This avoids velocity saturation and hot carriers effects, resulting in smaller excess noise factor α_{sat}. It also allows to take full advantage of the $1/L_f^2$ scaling of the transit frequency compared to the $1/L_f$ scaling when velocity saturation is present. Finally, moderate inversion also better accommodates the more and more stringent low-voltage constraint.

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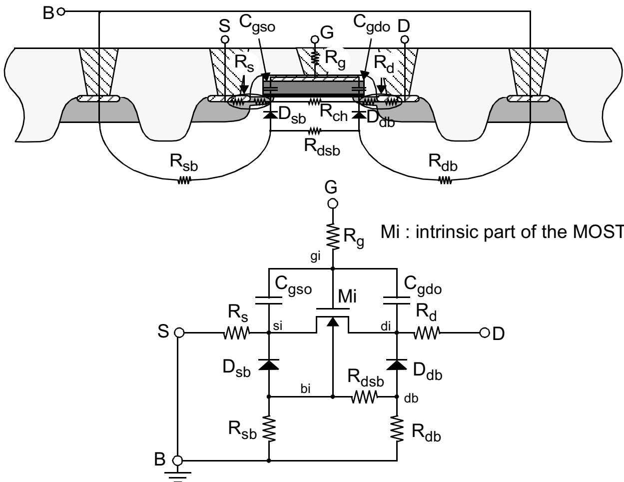
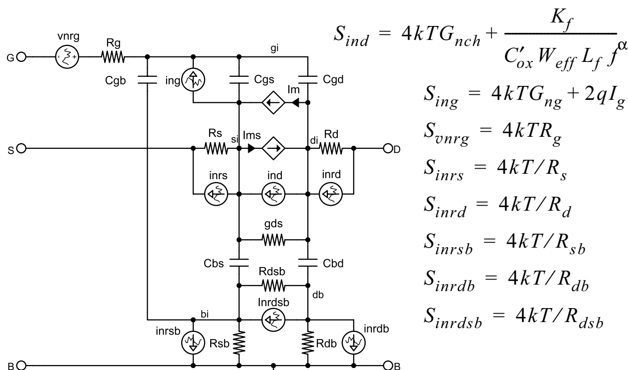
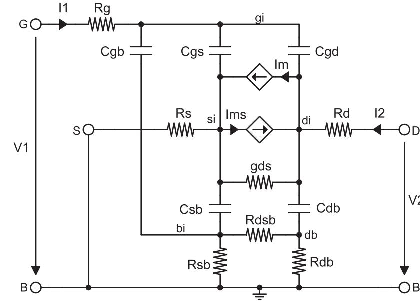


Fig. 1: Single finger RF-MOS transistor cross-section and equivalent circuit.



$$S_{ind} = 4kTG_{nch} + \frac{K_f}{C'_{ox} W_{eff} L_f f^{\alpha}}$$
$$S_{ing} = 4kTG_{ng} + 2qI_g$$
$$S_{vnrg} = 4kTR_g$$
$$S_{inrs} = 4kT/R_s$$
$$S_{inrd} = 4kT/R_d$$
$$S_{inrsb} = 4kT/R_{sb}$$
$$S_{inrdb} = 4kT/R_{db}$$
$$S_{inrdsb} = 4kT/R_{dsb}$$

Fig. 5: Noise sources in the MOS transistor**.**



Bulk referenced models:

$$I_m = Y_m \cdot (V(gi) - V(bi))$$
$$I_{ms} = Y_{ms} \cdot (V(si) - V(bi))$$
$$Y_{ms} = n \cdot Y_m$$

Source referenced models:

$$I_m = Y_m \cdot (V(gi) - V(si))$$
$$I_{ms} = -Y_{mb} \cdot (V(bi) - V(si))$$
$$Y_{mb} = (n-1) \cdot Y_m$$

Fig. 2: Simplified equivalent small-signal circuit (in saturation).

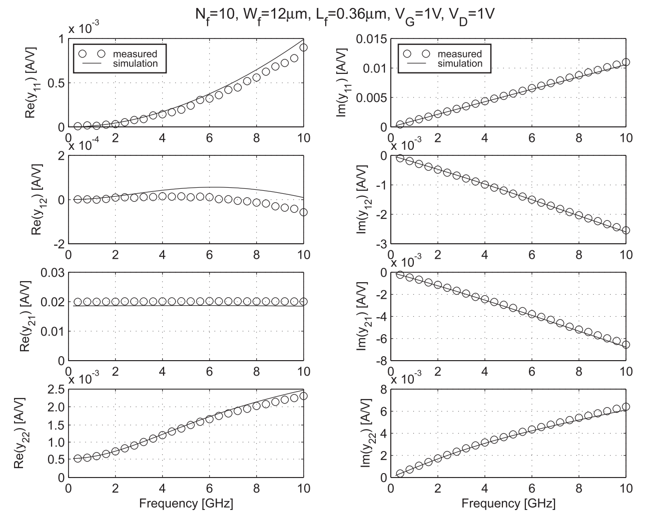


Fig. 3: Comparison between the measured, simulated and analytical Y-parameters (n-channel, $N_f = 10$, $W_f = 12\mu m$, $L_f = 0.36\mu m$ and $V_G = V_D = 1V$).

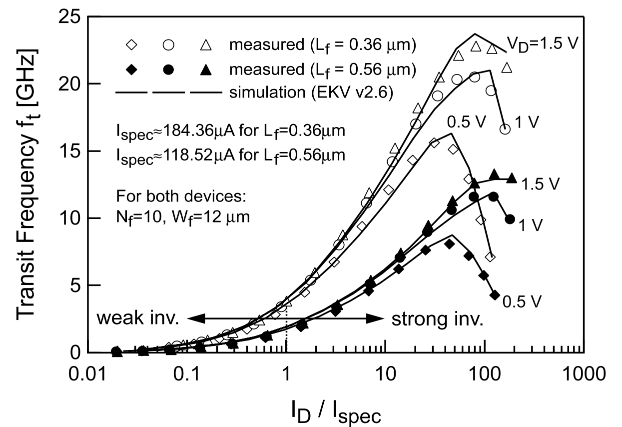


Fig. 4: Transit frequency f_t vs. inversion factor for two different transistors.

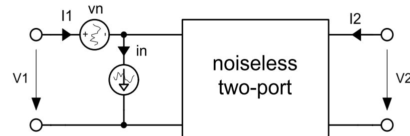


Fig. 6: ABCD-parameter representation of a noisy twoport.