# MOSFET mismatch in weak/moderate inversion: model needs and implications for analog design.

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## Abstract

*Based on mismatch measurements performed on very different CMOS technologies and large operating temperature range, we propose to model more adequately the mismatch in weak and moderate inversion by adding a new term related to the mismatch of the body effect factor dependence on the gate voltage. The model is introduced in a top-down analog design methodology, applied to the current mirror case, revealing some nonobvious design rules as well as typical misconceptions.*

## 1. Introduction

Despite the importance of transistor mismatch for high-performance analog designs, efficient integration of mismatch constraints in top-down analog synthesis is still lacking. Furthermore, existing mismatch models are not adequate in moderate and weak inversion. In this paper, drain current mismatch measurements performed on a 0.35 $\mu m$ CMOS Bulk technology and on a 2 $\mu m$ CMOS Silicon-On-Insulator (SOI) technology from room temperature up to 225 degrees C firstly help to better understand the phenomena, which influence the mismatch in weak and moderate inversion regions. Secondly, we show how analog circuit performance can be increased and design time can be reduced using an efficient top-down design methodology including mismatch data. As an example, we go through the design of a current mirror. This application reveals some nonobvious design rules as well as typical misconceptions.

## 2. Mismatch measurements

The drain current mismatch $((\Delta I_d)/I_d)$ in weak inversion is usually said to be dominated by threshold voltage mismatch $(\Delta V_T)$, as given by [1]

$$\frac{\Delta I_d}{I_d} = -\frac{g_m}{I_d}\Delta V_T \qquad (1)$$

A model assumed to be continuous from weak to strong inversion is presented in [2] relying on (1) and assuming that $\Delta V_T$ is the only parameter which influences the mismatch in weak inversion. The validity of this assumption is tested in [2], revealing that some other phenomena should play a role. In this paper, we also check the validity of this assumption using mismatch measurements performed on different technologies. We generalize the results to better understand the additional phenomena which occur in weak/moderate inversion. Based on this analysis, we propose an additional term related to the mismatch of the n factor $(\Delta n)$ dependence on gate bias $V_g$ to model more adequately the mismatch in weak/moderate inversion.

The test structure [3] for the 0.35 $\mu m$ Bulk CMOS process includes 30 different NMOS and PMOS transistor arrays of different sizes: widths are W = 40, 20, 10, 5, 2 and 0.8 $\mu m$ and lengths L = 10, 5, 2, 0.8 and 0.35 $\mu m$. There are 36 different transistors for each size. In the 2 $\mu m$ CMOS SOI technology [4], the test structure is an array of 20 fully-depleted (FD) NMOSFETs, each 20 $\mu m$ wide and 10 $\mu m$ long.

### 2.1. SOI case

Fig.1 shows the extracted drain current mismatch extracted in saturation for the SOI case from room temperature up to 225 degrees C. Fig.2 shows the measured $g_m/I_d$ vs. the normalised drain current $(I_{norm} = I_d/(W/L))$ for the same devices.

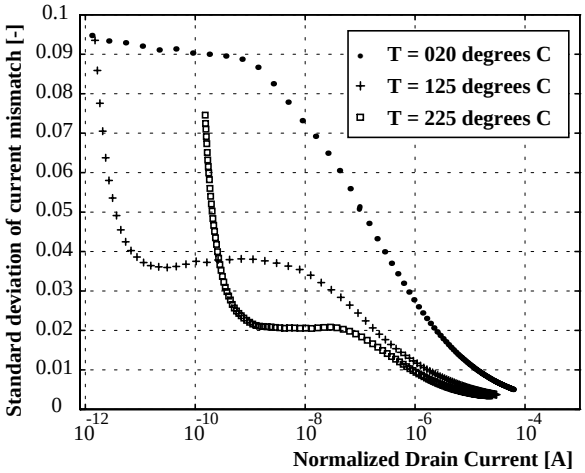


Figure 1. $\sigma((\Delta I_d)/I_d)$ vs. $I_{norm}$ curves for SOI FD nMOS (W/L=20 $\mu m$ /10 $\mu m$ ) at different temperatures T (Drain Voltage (Vd) = 1.5 V)

We clearly observe three different zones (Fig.1) :

•At high $I_{norm}$ (i.e. in strong inversion (SI)) : mismatch improves with the level of inversion and tempera-

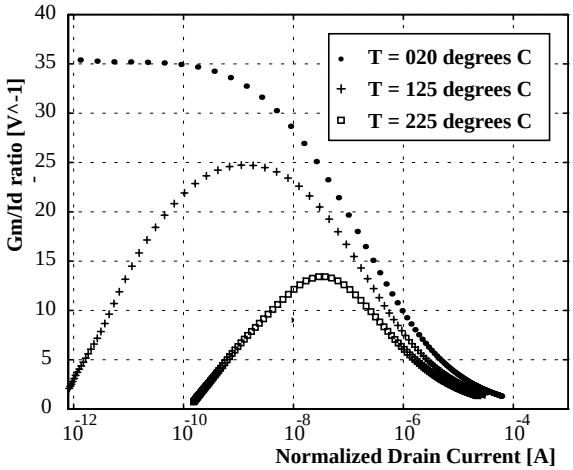


Figure 2. $g_m/I_d$ vs. $I_{norm}$ for SOI FD nMOS (W=20 $\mu m$ L= 10 $\mu m$) in saturation (Vd = 1.5 V) up to T = 225 degrees C

ture (T) thanks to the decrease of the $g_m/I_d$ ratio according to (1).

•At very low $I_{norm}$, the sudden increase of mismatch at elevated T can be linked to the subthreshold junction currents.

•In the central zone, close to the maximum of the $g_m/I_d$ curve (i.e. in weak inversion (WI)), the mismatch shows a plateau value which decreases and shifts to higher $I_{norm}$ values for increasing T according to the $g_m/I_d$ data and (1).

However from (1) and the measured $g_m/I_d$ curves, we clearly do not expect the mismatch to remain almost constant for $I_{norm}$ lower than the value corresponding to the maximum of $g_m/I_d$ since in this region $g_m/I_d$ significantly decreases (Fig.2).

To further stress these experimental discrepancies from the assumption that the threshold voltage mismatch is the only relevant effect in determining the mismatch in weak inversion, as in [2] we rewrite (1) as $(\Delta I_d)/g_m = -\Delta V_T$ and compute the correlation coefficient $(\rho)$ between $\Delta I_d/g_m$ at $V_{gs}= V_T$ and $\Delta I_d/g_m$ at other $V_{gs}$. $\Delta I_d/g_m$ was obtained from the measurement data and $\Delta V_T$ was extracted using a current criterion (i.e. $V_T$ is defined as the gate bias at an a priori defined current level $I_{cc}$). As we are interested in the validity of (1) and not in the exact value of $\Delta V_T$, we choosed, for each size, the value of $I_{cc}$ which best fits the measured mismatch to $-\frac{g_m}{I_d}\Delta V_T$. This ensures that the differences we would see between the two terms of (1) are not related to errors in the extraction procedure, but only the adequacy of (1).

Fig.3a presents $(\rho)$ for the SOI data. In SI, (1) is obviously not valid since the mismatch in the $\beta$ factor is neglected, which discussion is beyond the scope of our analysis. Moving towards moderate inversion (MI), $(\rho)$ increases as the mismatch on the $V_T$ becomes dominant (Fig.3a). Nevertheless, if we move forward in WI, $(\rho)$ starts to decrease and strongly worsens as T is increased (Fig.3a) as discussed above. This clearly indicates that there must be other phenomena occuring in WI and influencing the mismatch.

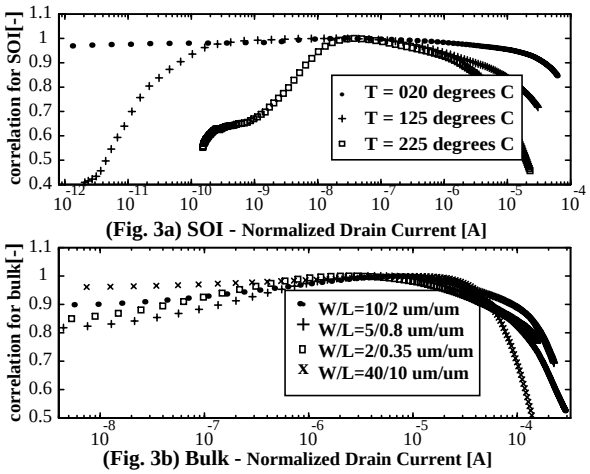


Figure 3. $(\rho)$ vs. $I_{norm}$ curve of SOI nMOS (W/L=20/10; Vd=1.5V) at different T (Fig. 3a) and curves of bulk nMOS of different sizes (Vd = 1.3 V) (Fig.3b)

## 2.2. Bulk case

Fig.3b and Fig.4 present typical $(\rho)$ and $g_m/I_d$ curves measured for the bulk nMOSFETs. Conclusions similar to SOI can be drawn, except that in bulk $(\rho)$ starts to decrease for biases immediately lower to $V_T$, i.e. in MI, whereas in SOI, $(\rho)$ shows a constant value on a wide bias range (MI) and only decreases for currents lower than the maximum or plateau value of $g_m/I_d$, i.e. in WI. This observation is key to the generalized understanding and modelling of the phenomenon.

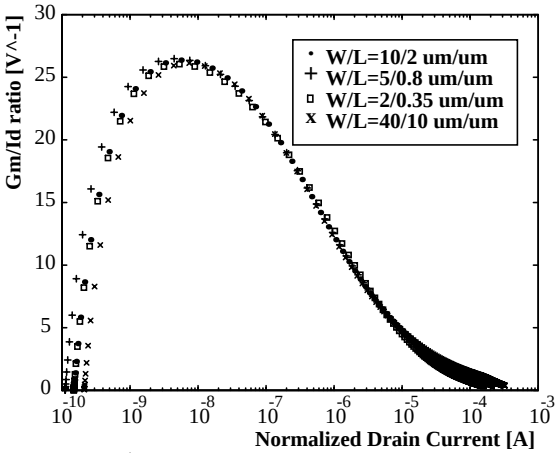


Figure 4. $g_m/I_d$ vs. $I_{norm}$ for nMOS bulk of different sizes in saturation (Vd = 1.3 V).

## 2.3. Generalization

For FD SOI MOSFETs, it is well known that the n body factor remains constant even in MI as the width of the depletion region is equal to the silicon film thickness [4]. Only in very weak inversion or as T is increased, does n start to increase. Whereas in bulk, for gate biases immediately below $V_T$ the depletion width shrinks as the

surface potential drops below $2\Phi_F$, the n factor in turn increases and strongly depends on the gate bias. To better fit the measured drain mismatch, we then propose to add a term to the right member of (1) such that:

$$\frac{\Delta I_d}{I_d} = -\frac{g_m}{I_d}\Delta V_T + f(V_g)\Delta n \qquad (2)$$

From the formula proposed in [5] to model the n dependence on $V_g$, we empirically propose a function $f(V_g)$, which adequately models the mismatch in WI to be like $f(V_g)= \frac{1}{\left[\alpha_1 + \left(\frac{v_g}{\alpha_2}\right)^{\alpha_3}\right]}$, where $\alpha_1,\alpha_2,\alpha_3$ are fitting parameters. Extracting n and $\Delta n$ by equating the measured maximum $g_m/I_d$ to $1/(nU_T)$, where $U_T$ is the thermal voltage and by fitting $f(V_g)$ to the measured mismatch of the bulk transistors, an excellent agreement is obtained in WI (Fig.5). Table I also shows that the values of the parameters of $f(V_g)$ for different MOS sizes stay rather similar, with $\alpha_2$ fairly close to $V_T$, which suggests a certain physical adequacy of our empirical formula

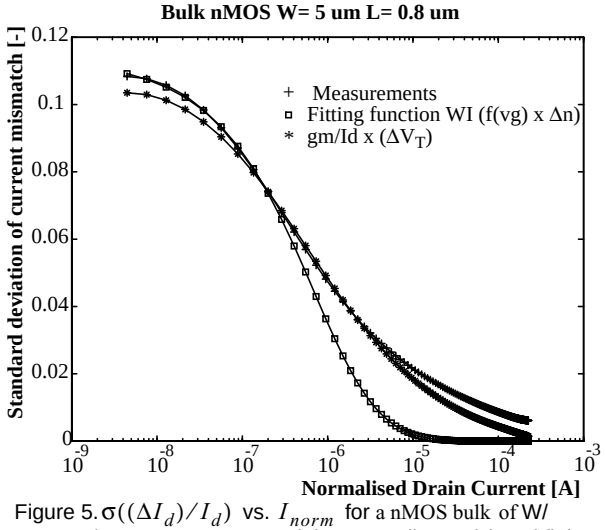


Figure 5. $\sigma((\Delta I_d)/I_d)$ vs. $I_{norm}$ for a nMOS bulk of W/L=5µm /0.8µm (Vd = 1.3V). Fitting according to (1) and fitting with $f(V_g)\Delta n$.

Table I: Parameters of the fitting function for the different W/L ratios

| | W/L=5/0.8 | W/L=20/5 | W/L=40/2 |
|---|---|---|---|
| $\alpha_1$ | 0.0372 | 0.0287 | 0.0205 |
| $\alpha_2$ | 0.9314 | 0.9087 | 1.0354 |
| $\alpha_3$ | 8.9192 | 8.4778 | 8.2048 |

Even if the difference between the measured mismatch and the approximate model (1) is not that big, it seems worth to add our new term since mismatch in moderate inversion is important to design high-performance analog circuits as we will show here below. Moreover, as temperature is considered, the importance of the additional term strongly rises.

## 3. Mismatch for the analog designer

Nevertheless, efficient modelling is useless if the models do not provide the analog designer with the adequate information on how to size and how to bias transistors in order to optimize mismatch along with other analog performance such as e.g. the gain-bandwidth product GBW. Recently, [6] proposed a model aiming to be designer focused. But the use of this model remains based on complicated Monte-Carlo or sensitivity analysis and when applying the methodology to the design of a current mirror only mismatch is optimized, whereas e.g. the position of the pole-zero doublet associated to the mirror is not guaranteed to lie beyond the transition frequency of the circuit he is part of.

Here below, we show that incorporating basic mismatch data into our $g_m/I_d$ design methodology [7], we are able to efficiently guide the analog designer when dealing with mismatch constraints among others. In a second design step, experimental or more accurate models from the foundry can be used to fine tune the devices bias and sizes. This results in design time savings and in more performant circuits.

As an example, we will go through the design of a nMOS current mirror. We suppose the current mirror is part of a one-stage differential-input amplifier, e.g. the first stage of a Miller type two-stage amplifier. If the amplifier is intended to be part of a high-precision circuit, we expect the first stage to be low-noise, low-offset and possibly low-voltage.

The following example uses the $0.35\mu m$ Bulk CMOS data and targets a GBW of $2MHz$ on a load capacitance $(C_L)$ equal to $2pF$. The MOS behaviour is described by the $g_m/I_d$ ratio vs. $I_{norm}$ characteristic directly coming from measurements.

To minimize the added 1/f noise of the current mirror, nMOS $(M_3,M_4)$ their length $(L_3)$ must be such that [8]: $L_3 \geq 5\ldots6 \times L_1$, where $L_1$ is the length of the input differential pair pMOS $(M_1,M_2)$. We can suppose that $L_1$ is minimum (i.e. 0.35 $\mu m$, here) to best comply with the specifications. But too long mirror devices may cause the apparition of a pole-zero doublet, linked to the capacitance existing at the mirror node $(C_1)$, which is given by

$$C_1 = C_{db1} + C_{db3} + C_{gg3} + C_{gso3} + C_{gg4} + C_{gso4} \qquad (3)$$

where $C_{db1}(C_{db3})$ is the drain-to-substrate capacitance of the negative input transitor $M_1$ (of the diode-connected $M_3$), $C_{gg3}(C_{gg4})$ is the total gate capacitance of $M_3$ ( $M_4$) and $C_{gso3}(C_{gso4})$ is the gate-source overlap capacitance of $M_3$ ( $M_4$). A continuous expression from weak to strong inversion for $C_{gg}$ can be obtained through the EKV model [5] or estimated from measurements. All other capacitances are given by the technology.

The frequency of the mirror pole is given by

$$F_{mir} = g_{m,3}/(2\pi C_1) \quad (4)$$

where $g_{m,3}$ is the transconductance of $M_3$ and $M_4$. The mirror zero is at twice $F_{mirr}$. As a design criterion to minimize the related phase losses, we decide that

$$F_{mir} \geq 4 f_T \quad (5)$$

Let us now consider that the total unprecision of the mirror is related to the random mismatch. The impact of the finite output resistance of $M_3$ and $M_4$ could be easily introduced but is beyond the scope of this paper. The current mismatch of long devices occupying a relatively small area can be described as [9] (2)

$$\sigma\left(\frac{\Delta I_d}{I_d}\right) = \frac{g_m}{I_d}\sigma(\Delta V_T) + f(v_g)\sigma(\Delta n) + \sigma\left(\frac{\Delta\beta}{\beta}\right)$$
$$\sigma^2(\Delta V_T) = \frac{A_{VTo}^2}{WL};\sigma^2\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta^2}{WL} \quad (6)$$

For short lengths, the mismatch model of (6) might not be 100% corect but would still yield a correct qualitative trend in order to select the more appropriate length range in a first step. Once this is known, the analog designer could use more accurate mismatch models to fine tune his design. Parameters for (6) were extracted from bulk measurements ; as we do not know yet the exact dependence of $f(V_g)$ on device dimensions, we did not include this term in the design example without loosing generality.

Fig.6 demonstrates that, when designing our current mirror to satisfy (5), for a fixed bias current defined by the choices made on the input differential pair to respect the GBW specifications, the mismatch for a given mirror length decreases, contrarily to the classical belief, when biasing the device towards the WI region i.e. high $g_m/I_d$ ratios.

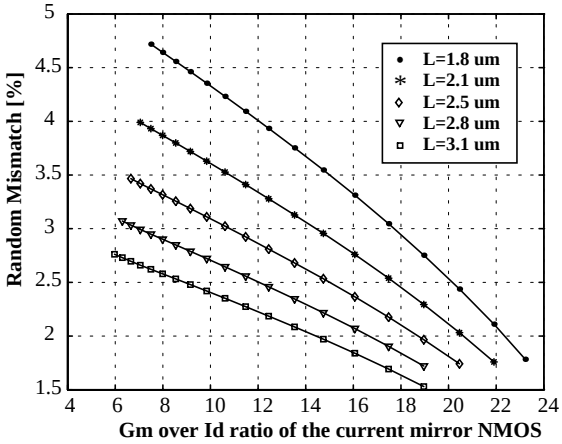


Figure 6.Random mismatch of the mirror vs. nMOS $g_m/I_d$ for different lengths (drain current of 1.676 µA and $g_m/I_d$ of the pMOS : 15)

This is due to the fact that as we move from strong to weak inversion and from a design perspective (i.e. constant current), two balancing phenomena occur : the mismatch increases for a given transistor size but decreases with increasing transistor surface (6), the last phenomenon being far dominant. The possible use of high $g_m/I_d$ is obviously of high interest for low-voltage low-power applications.

## 4. Conclusions

We presented drain current mismatch measurements performed on a 0.35 $\mu m$ CMOS Bulk technology and on a 2 $\mu m$ CMOS SOI technology and, for the first time to our knowledge, up to 225 degrees C. Based on these measurements, we confirmed and explained the non validity of the classical assumptions regarding mismatch in weak and moderate inversion. We also proposed to add a term related to the mismatch of the body factor dependence on gate bias. We showed that this term adequately fits the mismatch in the weak and moderate inversion region. We finally included drain current mismatch data in a top-down design methodology showing how we can design more performant analog circuits in shorter time.

## 5. References


[1] E.A. Vittoz. “The design of high-performance analog circuits on digital CMOS chips” *IEEE J. of Solid-State Circuits*, Vol. SC-20, Mar. 1985.

[2] J.A. Croon et al. “An Easy-to-Use Mismatch Model for the MOS Transistor” *IEEE J. of Solid-State Circuits*, Vol. 37, No 8, Aug. 2002.

[3] Teresa Serrano-Gotarredona et al. “Systematic Width-and-Length Dependent CMOS Transistor Mismatch Characterization and Simulation" *Analog Integrated Circuits and Signal Processing,* Dec. 1999.

[4] D. Flandre et al. “Fully-depleted SOI CMOS technology for low-voltage low-power mixed digital/analog/ microwave circuits” *Analog Integrated Circuits and Signal Processing*, Dec. 1999.

[5] C. Enz et al. “An analytical MOS transistor model valid in all regions of Operation and dedicated to low-voltage and low-current applications” *Analog Integrated Circuits and Signal Processsing*, July 1995

[6] P.G. Drennan et al. “Understanding MOSFET Mismatch for Analog Design” *IEEE J. of Solid-State Circuits,* Vol. 38, No 3, Mar. 2003.

[7] J.-P. Eggermont et al. “Design of SOI CMOS Operational Amplifiers for Applications up to 300C” *IEEE J. of Solid-State Circuits,* Vol. 38, No 3, Mar. 2003.

[8] K. R Laker, W. Sansen. *Design of Analog Integrated Circuits and Systems*. New York: McGraw-Hill, 1984.

[9] M. Pelgrom, A. Duinmaijer, A. Welbers. “Matching properties of MOS Transistors” *IEEE J. of Solid-State Circuits,* Vol. 24, No 5, Oct. 1989.