MOSFET Mismatch Modeling: A New Approach

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Editor's note:
Handling component mismatch represents a great challenge in analog and even digital design for current and future submicron technologies. This article, a special selection from the Symposium on Integrated Circuits and Systems Design (SBCCI), presents a matching model to help designers account for real effects while maintaining simplicity and easing the design effort.
—Luigi Carro, Federal University of Rio Grande do Sul

Digital and analog ICs generally rely on the concept of matched behavior between identically designed devices.[1-3] Time-independent variations between identically designed transistors, called mismatch, affect the performance of most analog and even digital MOS circuits. In analog circuits, the spread in the DC characteristics of supposedly matched transistors produces inaccurate or even anomalous circuit behavior.[2] In digital circuits, transistor mismatch leads to propagation delays whose spread can amount to several gate delays for deep-submicron technologies.[2,3] As Meindl predicted, "Variations will set the ultimate limits on scaling of MOSFETs."[4] Shrinking MOSFET dimensions and a reduced supply voltage make matching limitations even more important.

Mismatch results from either systematic or stochastic (random) effects. Systematic effects originate from either poor layout or uncontrollable variation during an IC's fabrication. Systematic mismatch can originate from equipment-induced nonuniformities such as temperature gradients and photomask size differences across the wafer. Systematic effects are important for large distances, but appropriate layout techniques can minimize them.

Random mismatch refers to local variation in parameters such as doping concentration, mobility, oxide thickness, and polysilicon granularity. Random mismatch dominates systematic mismatch for short distances (that is, distances of the same order as the transistor size as opposed to the die size) and is generally assumed to display a Gaussian distribution characterized by the random mismatch's standard deviation. Stochastic mismatch requires a model to guide the IC designer's sizing and biasing strategies.

This article focuses on the analysis of mismatch in MOS transistors resulting from random fluctuations of the dopant concentration, first studied by Keyes.[5] Today, we recognize these fluctuations as the main cause of mismatch in bulk CMOS transistors.

Impurity fluctuation effects

Veendrick offers an example of how the dopant concentration in advanced technologies affects a transistor's electrical performance.[2] A minimum-size transistor in a 0.25-micron CMOS process contains about 1,100 dopant atoms in the depletion layer beneath the channel. A 0.10-micron process contains only 200 dopant atoms. Assuming a Poisson distribution of impurities in both the 0.25- and 0.10-micron technologies, the spreads in the number of dopant atoms beneath the channel are about 33 and 14, respectively. In both cases, the spread in the number of dopant atoms causes a spread in an electrical parameter of the MOSFET, the threshold voltage (V_T), of about 30 mV. This effect increases with each new process generation. As an example, for gate voltages below V_T (weak inversion, a bias condition commonly used in low-power circuits), a 30-mV deviation in V_T causes deviation in the transistor current by a factor of about 2.5, which can be catastrophic for many

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applications. Although undoped double-gate MOSFETs (FinFETs) avoid dopants and, consequently, dopant number fluctuation effects, single-gate doped MOSFETs will still prevail in coming years. Therefore, predicting the effects of random dopant numbers on MOSFET mismatch is of prime importance.

Figure 1, from an article that investigates the influence of random dopant fluctuation on threshold voltage deviation,[6] illustrates both the atomistic distribution of impurities and the potential distribution. In this figure, the gate is flipped open like the cover of a book to give an impression of the random distribution of its dopants (dots) at its interface with the gate oxide, which is removed. The actual number of dopants in each atomistic region randomly follows a Poisson distribution with a mean equal to the corresponding average dopant numbers. The article concludes that the effects of random distribution of dopants in both the channel region and the gate are important factors contributing to component mismatch in deep-submicron devices.

In general, the applicability of DC models for characterizing mismatch hasn't been questioned. Researchers widely accept that they can model matching by the random variations in geometric, process, or device parameters, and using the transistor DC model lets them quantify the effect of these random parameters on the drain current. As Lan and Geiger,[7] and more recently Yang et al.,[8] point out, there is a fundamental flaw in the current DC models for mismatch, and this flaw results in inconsistent formulas. The main reason for this inconsistency arises from the assumption that mismatch can be calculated by using lumped parameters rather than by accounting for the MOS transistor channel's distributed nature. According to Lan and Geiger, using lumped parameters for the series or parallel association of transistors leads to an inconsistent model of mismatch, owing to the nonlinear nature of MOSFETs.[7] The conventional approach to modeling mismatch, described by Pelgrom et al., accounts for the dopant fluctuations over the entire channel,[3] but in this article we consider explicitly the effects of local fluctuations. We integrate the contribution of the local fluctuations along the channel, keeping in mind the main MOSFET nonlinearities. Fortunately, the formalism needed to include local fluctuations—namely, carrier number fluctuation theory—is already available in flicker, or 1/*f*, noise modeling.[9]

Our work deals mainly with the effects of having a random number of carriers resulting from impurity fluctuations, acknowledged as the dominant source of mismatch in MOS transistors. The result is a compact expression for transistor mismatch, which we obtain through the advanced compact MOSFET (ACM) model.[10]

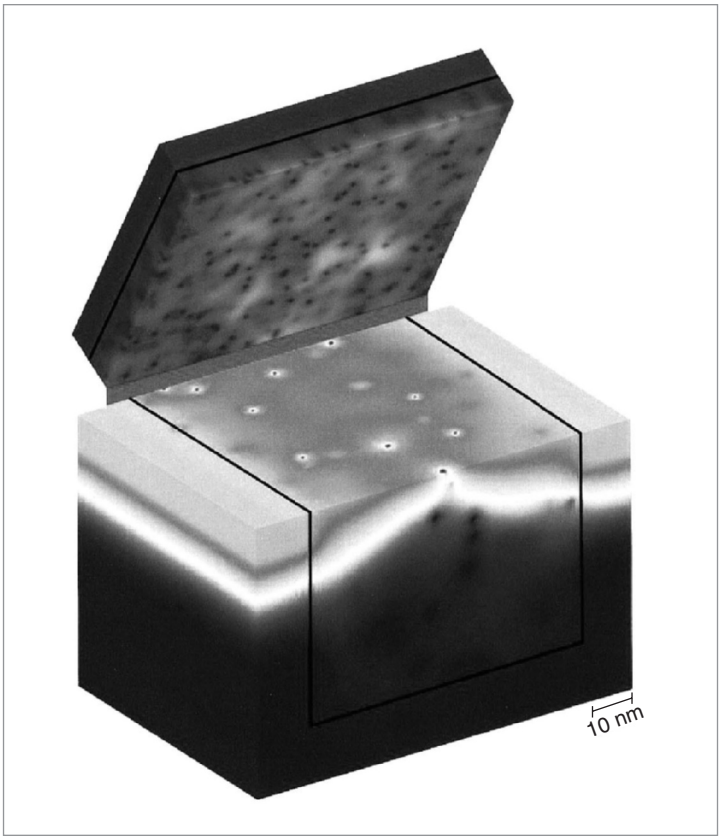
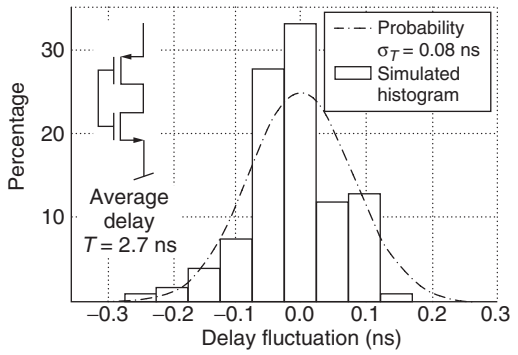


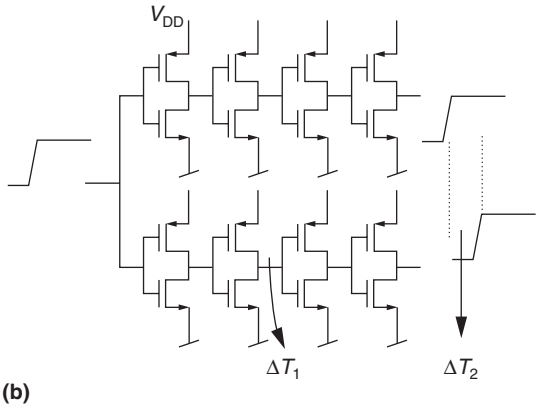
Figure 1. Typical atomistic simulation domain for a MOSFET with a single crystal silicon gate, channel doping concentration $N_A = 5 \times 10^{18}$ cm^{-3}, gate doping concentration $N_D = 5 \times 10^{19}$ cm^{-3}, $L_{eff} = W_{eff}$ (effective channel length and width) = 50 nm, x_j (drain and source junction depth) = 7 nm, and t_{ox} (oxide thickness)= 3 nm. The potential distribution corresponds to $V_G = V_T = 0.723$ V.

Conventional bulk CMOS technology still prevails (and will for several years) in the microelectronics industry. According to the latest update of the *International Technology Roadmap for Semiconductors* (http://public.itrs.net), bulk MOS transistors will be used for the 45-nm technology node (gate length around 18 nm), expected in 2010. In fact, the feasibility of 15-nm conventional MOS transistors in a bulk CMOS technology has already been demonstrated.[11] Also, as many recent articles have shown, dopant fluctuation in the depletion region will be the dominant factor for the random variations of bulk CMOS processes of coming generations.

By focusing mainly on the prevailing cause of parameter fluctuations, we intend to provide circuit designers with a novel mismatch model that is easy to use and



(a)



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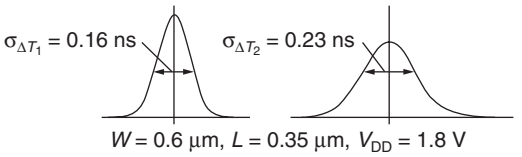


(c)

V_{DD} (V)	T (ns)	σ_T/T
3.3	1.3	1.8%
1.8	2.7	2.9%
1.2	8.2	7.5%
1.0	19	13%
0.8	119	38%

W = 0.6 µm, L = 0.35 µm

W (µm)	T (ns)	σ_T/T
9.6	4.9	0.7%
2.4	5.0	2.8%
0.6	8.2	7.5%

V_{DD} = 1.2 V, L = 0.35 µm

(d)

Figure 2. Chain of buffers illustrating the clock skew between two branches of a clock tree caused by MOS transistor mismatch. The histogram is the simulated distribution of the time delay over 200 trials for a single minimum-size inverter in a 0.35-micron technology with V_{DD} = 1.8 V (a). Delay fluctuations accumulate in the two four-inverter chains (b). As the pulses advance, their time difference (ΔT) is more likely to increase, as noted in the expected distribution plots for ΔT_1 (two inverters) and ΔT_2 (four inverters) (c). The tables show the delay dispersion normalized to the average delay of a unit inverter (σ_T/T) for different transistor sizes and supply voltages (d).

requires only simple calculations. Also, our mismatch model is intrinsically consistent for series/parallel association. Although we used the ACM model to derive our mismatch model, our results are fully compatible with most transistor DC models and therefore can be readily included in circuit simulators, offering direct mismatch estimations without the need of time-consuming iterative Monte Carlo analysis.

Implications for electronic circuits

The two identical inverter chains in Figure 2b are an example of a deleterious effect of mismatch in digital circuits.[2,3] The mismatch in the inverter chains, caused by transistor mismatch, permits the arrival times at the end of each path to differ by several gate delays, depending on the inverter chain's depth. Delay fluctuations increase when lowering the supply voltage or reducing the transistor size, two major trends in modern technology. For high-speed circuits, where timing is critical, modeling of transistor mismatch is essential for a robust design.

A familiar effect of component mismatch is the offset voltage of operational amplifiers. This is the differential voltage required at the input to set the output to 0. The offset voltage comprises random and systematic components. Good engineering can set the systematic component to some tens of microvolts; the random component depends on matching between transistors. Figure 3 is a histogram of the simulated distribution of the offset voltage of a CMOS operational amplifier over 1,000 trials, using parameters from a standard 0.35-micron technology. The simulation results led to a standard deviation of 2.1 mV.

For simulation of the operational amplifier and the inverters, we assume that the transistors' threshold voltages follow a normal distribution, according to the model described by Pelgrom et al.[3] Because operational amplifiers (or comparators) usually serve as parts of more complex circuits, their offset uncertainty appears as specific circuit limitations. For example, the operational amplifier offset can directly impact the yield of an A/D converter by limiting the maximum achievable converter resolution.[3] Such circuit deviations demonstrate how important it is for designers to predict the impact of transistor mismatch on circuit performance or how to use the mismatch information to alter the design to achieve the required accuracy. Existing mismatch models, howev-

er, are not really appropriate: They use either simple drain current models limited to a specific operating region,[1,3] or complex expressions.[12]

The current-based ACM model

The charge-based ACM model was derived on the basis of an approximation of the depletion capacitance—one of a MOSFET's fundamental capacitances.[10] Rather than reproducing the derivation of the ACM model here, we simply present the expression that is most useful to designers. In the ACM model, drain current I_D is expressed as the difference between the forward (I_F) and reverse (I_R) components.[10]

$$I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D) = I_S(i_f - i_r) \quad (1)$$

where $I_S = (1/2)\mu C'_{ox} n \phi_t^2 (W/L)$ is the normalization current, which is proportional to the transistor's aspect ratio W/L. V_G, V_S, and V_D are the gate, source, and drain voltages, with reference to the substrate. Here, C'_{ox} is the gate oxide capacitance per unit area; n is the slope factor, slightly greater than unity and weakly dependent on the gate voltage; μ is the effective mobility; and ϕ_t is the thermal voltage. Parameters i_f and i_r are the normalized forward and reverse currents, or inversion levels, at the source and the drain, respectively. In the saturation region, the drain current is almost independent of V_D; therefore, $i_f >> i_r$ and $I_D \cong I_F$. On the other hand, if V_D is low (linear region), then $i_f \cong i_r$. Figure 4 illustrates the decomposition of the drain current.

The inversion level i_f (i_r) represents the normalized carrier charge density at the MOSFET source (drain). As a rule of thumb, values of i_f greater than 100 characterize strong inversion, and those less than 1 are associated with weak inversion. Intermediate values of i_f, from 1 to 100, indicate moderate inversion.

This model is bulk referenced and fully drain-source reversible.

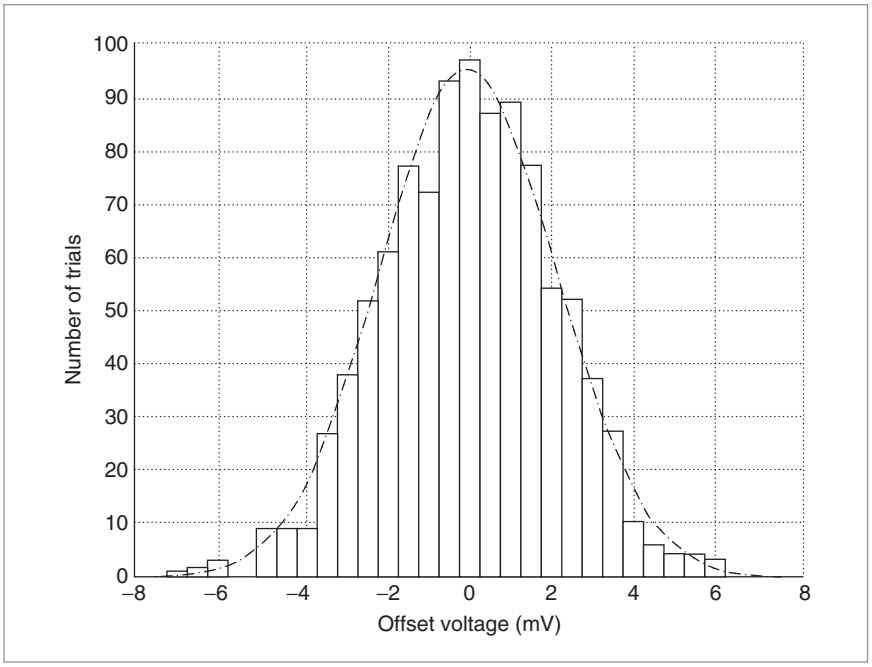


Figure 3. Monte Carlo simulation of the offset voltage of a CMOS Miller operational amplifier. The histogram shows the distribution of the offset voltage over 1,000 trials in 0.5-mV intervals. The dot-dashed curve is the related Gaussian approximation.

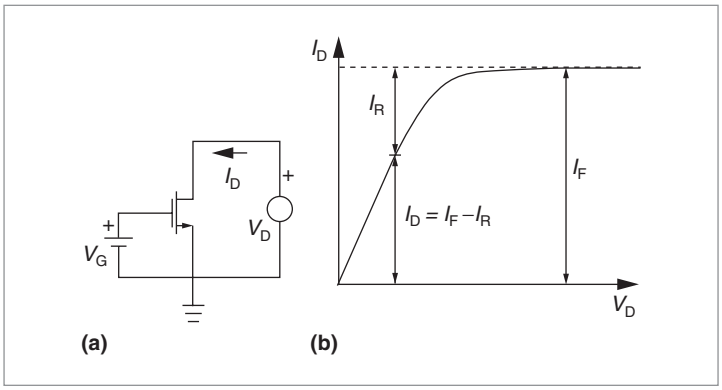


Figure 4. DC characteristics of a MOS transistor in the common-source configuration: the common-source circuit (a) and the decomposition of the drain current into its forward and reverse components (b).

Mismatch model for drain current

For simplicity, in the derivations that follow, we give some equations that provide the essential parameters needed to understand the principles of our mismatch model. Detailed derivations of the drain current mismatch model are available in the literature.[13]

In the following derivation of the mismatch model, we calculated the fluctuations of the drain current

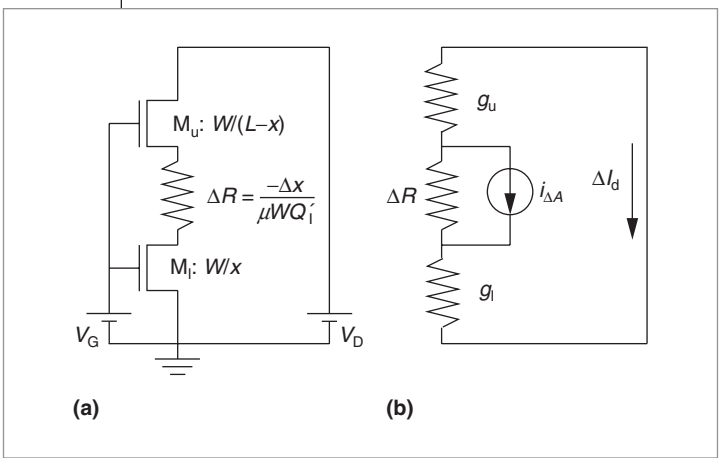


Figure 5. Splitting a transistor into three series elements: transistor equivalent circuit (a) and small-signal equivalent circuit (b), where ΔR is the resistance of the small channel element between the upper and lower transistors of the model, g_u and g_l are the small-signal conductance of the upper and lower MOS transistor, $i_{\Delta A}$ is the local current fluctuation related to the small channel element of area ΔA, and ΔI_d is the effect of $i_{\Delta A}$ on the drain terminal of the device.

around its nominal value resulting from the sum of all the tiny contributions from local fluctuations along the channel, whatever their origin. To calculate the effect of these fluctuations, we split the transistor into three series elements, as shown in Figure 5a: an upper transistor (M_u), a lower transistor (M_l), and a small channel element of length Δx and area $\Delta A = W\Delta x$. In Figure 5a, x is the distance from the channel element to the source.

We assume the local current fluctuation ($i_{\Delta A}$) to be a 0-mean stationary random process dependent on the variable x. Small-signal analysis lets us calculate the effect of $i_{\Delta A}$ on the drain current deviation (ΔI_d), as Figure 5b shows.

The current division between the channel element and the equivalent small-signal resistance of the rest of the channel[13] gives

$$\Delta I_d = [(\Delta x)/L]\, i_{\Delta A} \tag{2}$$

Thus, the square of the total drain current fluctuation is

$$\overline{\Delta I_D{}^2} = \sum_{\text{channel length}} (\Delta I_d)^2 = \lim_{\Delta x \to 0} \sum \left(\frac{\Delta x}{L} i_{\Delta A} \right)^2 = \frac{1}{L^2} \int_0^L \Delta x \left(i_{\Delta A} \right)^2 dx \tag{3}$$

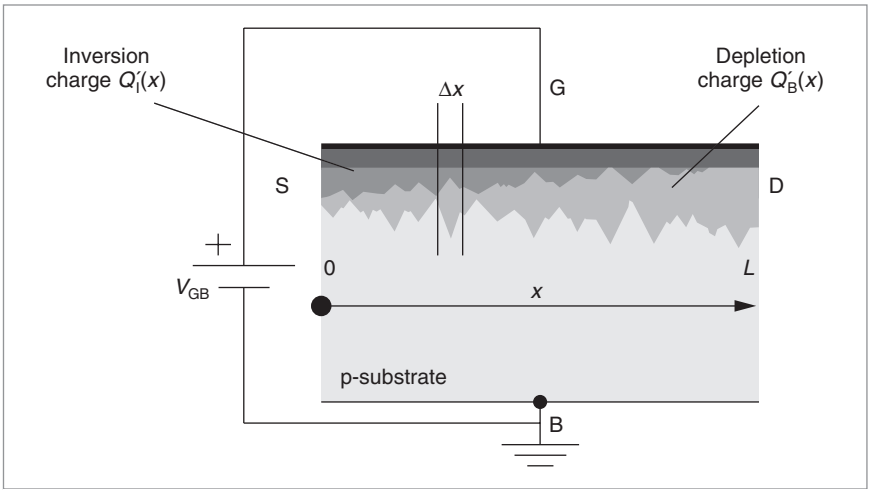


Figure 6. Cross section of a MOS transistor showing the (greatly exaggerated) fluctuations in both inversion and depletion charge densities resulting from local dopant fluctuations. V_{GB} is the gate-bulk voltage, S is the source region, D is the drain region, G is the gate terminal, and B is the bulk terminal.

In Equation 3, we assumed that the local current fluctuations along the channel are uncorrelated. Local current fluctuations arise from three independent physical origins, namely fluctuations of both channel and polysilicon gate doping, surface state density, and gate oxide thickness.[3] Because $i_{\Delta A}$ is related to local fluctuation calculated in the area $W\Delta x$, its variance is proportional to $1/(W\Delta x)$. Like Pelgrom et al.,[3] we assumed that channel doping fluctuation is the main factor that determines local current fluctuations. Figure 6 shows the fluctuations in the inversion charge density Q'_I resulting from local dopant fluctuations. Note that both the depletion charge Q'_B and the inversion charge Q'_I change as a result of the variation in the number of impurity atoms along the x-axis. Like Pelgrom et al.,[3] we have assumed that fluctuations in the number of impurities are solely responsible for fluctuations $\Delta Q'_I$ in the inversion charge density.

To derive the mismatch model, we adopted the following principles and approximations:[13]

- charge conservation in the MOS transistor;

- the capacitive model of the MOS transistor, assuming the depletion capacitance to depend on the gate-bulk voltage only;
- the current division principle, as shown in Equation 2;
- fluctuation of the impurity concentration in the depletion layer as the main source of mismatch;
- the assumption of a Poisson distribution of impurity atoms;
- the assumption of uncorrelated local impurity fluctuations;
- expression of the channel current in terms of the inversion charge and the channel potential; and
- the ACM model.

Applying these eight principles and approximations yields

$$\frac{\sigma^2_{I_D}}{I^2_D} = \left(\frac{N_{oi}}{WLN^{*2}}\right)\left(\frac{1}{i_f - i_r}\right)\ln\left(\frac{1+i_f}{1+i_r}\right) \quad (4a)$$

with

$$N^* = (nC'_{ox}\phi_t)/q \quad (4b)$$

and

$$N_{oi} = \int_0^{y_d} N\left(1-\frac{y}{y_d}\right)^2 dy \quad (4c)$$

In Equation 4a, $\sigma^2_{I_D}$ is the square of the standard deviation of the drain current. In Equation 4b, N^* represents the ratio of the channel charge density at pinch-off to the electron charge. In Equation 4c, y is the depth from the oxide-semiconductor interface, and y_d is the depletion region depth.

We define N_{oi} as the effective number of impurities per unit area in depletion depth y_d. $N = N_a + N_d$, the local impurity concentration, in cm^{-3}, where N represents the sum of the acceptor and the donor concentration of impurities, or the total local impurity concentration. Stated simply, N_{oi} is a technological parameter that translates a Poisson distribution's random number of impurities into a continuous mismatch model. Equation 4a presents mismatch dependencies on geometry (W and L), bias (i_f and i_r), and technology (N^* and N_{oi}), which are the three degrees of freedom that circuit designers use.

The result in Equation 4a is essentially the same as that derived for flicker noise in MOS transistors by Arnaud and Galup-Montoro.[9] This similarity results from the physical origin of both matching and 1/*f* noise. The former is related to spatial fluctuations in fixed charges; the latter results from temporal fluctuations in localized states along the channel.

Equation 4a indicates that the ratio of mismatch power to DC power is inversely proportional to gate area WL. Moreover, this ratio is proportional to t_{ox}^2 and to $N^{1/2}$ for a constant doping level. It's possible to simplify Equation 4a under specific conditions. In the following section, we consider particular cases of Equation 4a to provide insight into its meaning and to interpret the experimental results from its use.

Our model uses a continuous approach, evaluating the impact of doping fluctuation only, but it disregards the impurity position placement, a factor that significantly impacts mismatch for very short channel technologies (below 100 nm). A compact model like ours gives a first-order approximation of mismatch in advanced bulk CMOS technologies, or it can give accurate results if N_{oi} is modified to include short-channel effects.

Interpreting the mismatch model for particular operating regions

In weak inversion, $i_f, i_r \ll 1$; thus, the first-order series expansion of Equation 4a leads to

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{N_{oi}}{WLN^{*2}} \quad (5a)$$

Therefore, in weak inversion, the normalized mismatch is not sensitive to the current level, for either the saturation ($i_f \gg i_r$) region or the linear ($i_f \cong i_r$) region.

From weak to strong inversion in the linear region, $i_f \cong i_r$, and Equation 4a reduces to

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{N_{oi}}{WLN^{*2}}\frac{1}{1+i_f} \quad (5b)$$

Equation 5b indicates once again that the normalized mismatch is not sensitive to the inversion level in weak inversion ($i_f \ll 1$) and is inversely proportional to i_f in strong inversion ($i_f \gg 1$).

Finally, in saturation ($i_r \to 0$), Equation 4a can be written as

$$\frac{\sigma^2_{I_D}}{I^2_D} = \frac{N_{oi}}{WLN^{*2}}\frac{\ln(1+i_f)}{i_f} \quad (5c)$$

As IC designers are generally aware, Equations 5b and 5c indicate that under strong inversion, current mis-

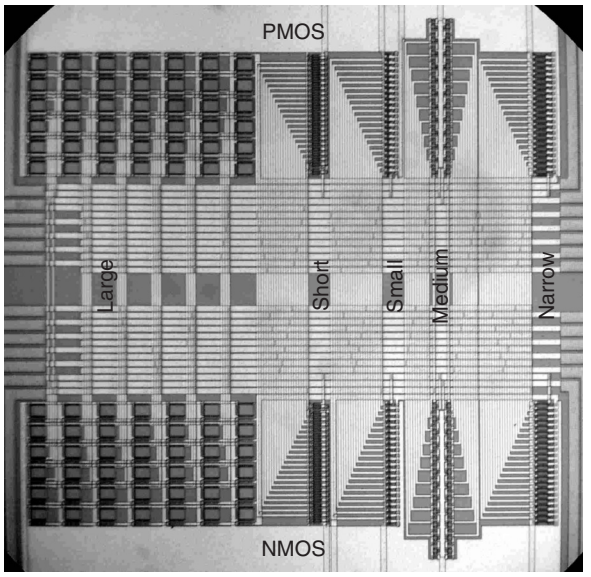


Figure 7. Test chip microphotograph showing PMOS and NMOS transistor arrays fabricated in a 0.35-micron technology. Transistor dimensions ($W \times L$) in the different arrays are 12 μm × 8 μm (large), 3 μm × 2 μm (medium), 0.75 μm × 8 μm (narrow-minimum width), 12 μm × 0.5 μm (short-minimum length), and 0.75 μm × 0.5 μm (small-minimum size).

match decreases when the inversion level increases. This behavior is more prominent in the linear than in the saturation region.

Measurements

We measured intradie current mismatch in a set of NMOS and PMOS transistors on a test circuit fabricated with the Taiwan Semiconductor Manufacturing Co. (TSMC) 0.35-micron 3.3-V CMOS n-well process, through the Mosis Educational Program (http://www.mosis.org). To ensure the same surroundings for all the transistors, those in the test circuit are in arrays of 20 identical devices terminated by dummy transistors. Matched transistors have the same orientation. Wide metal connections and multiple contact windows in the layout assure lower ohmic drops. All of the 10 packaged dies that were characterized showed similar mismatch behavior.[14] Figure 7 is a microphotograph of the test chip.

Figure 8 shows the mismatch power normalized to the DC power for drain-to-source voltage ranging from 10 mV (linear region) to 2 V (saturation) for the medium-size NMOS devices. We measured mismatch for six different inversion levels (0.01, 0.10, 1.00, 10, 100, and 1,000), keeping the bulk terminal at 0 V. We determined simulated (model) curves from Equation 4a, with i_r calculated through the ACM model.[10]

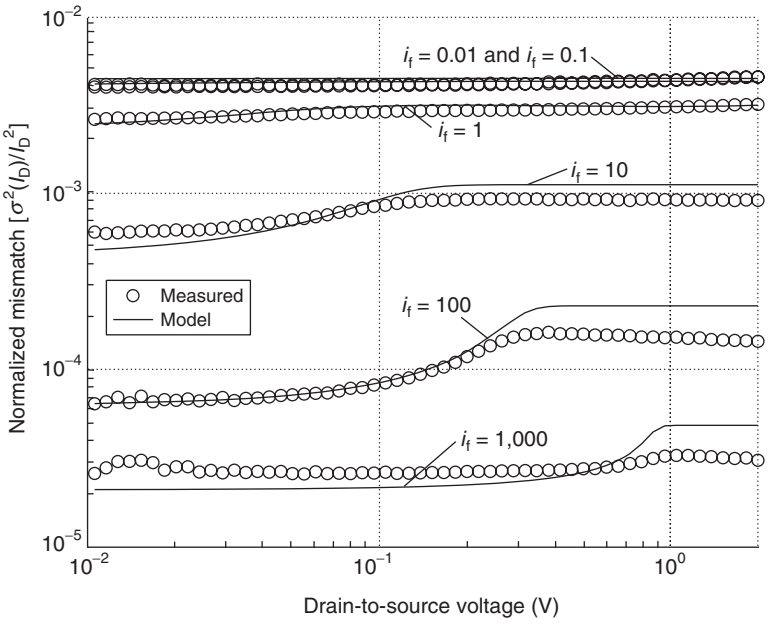


Figure 8. Normalized current mismatch power for the medium-size (W = 3 μm, L = 2 μm) NMOS transistor array.

In weak inversion (i_f = 0.01 and 0.10), mismatch is almost constant from the linear to the saturation region and independent of the inversion level, as predicted by Equation 5a. The measured and simulated curves for weak inversion are almost coincident. From moderate (i_f = 1 and 10) to strong (i_f = 100) inversion, both the simulated and measured curves show similar behavior, increasing from the linear to the saturation region, where they form a plateau. Differences between measured and simulated curves at saturation can be associated with statistical spatial-nonuniformity concentration of dopant atoms.

We estimated parameter N_{oi} from measurements in weak inversion, using Equation 5a, with effective transistor width and length, and we calculated N^* on the basis of parameters provided by Mosis. We obtained the same value of N_{oi} (1.8×10^{12} cm^{-2} for the NMOS devices and 7×10^{12} cm^{-2} for the PMOS devices) for both

the large and medium-size transistors.

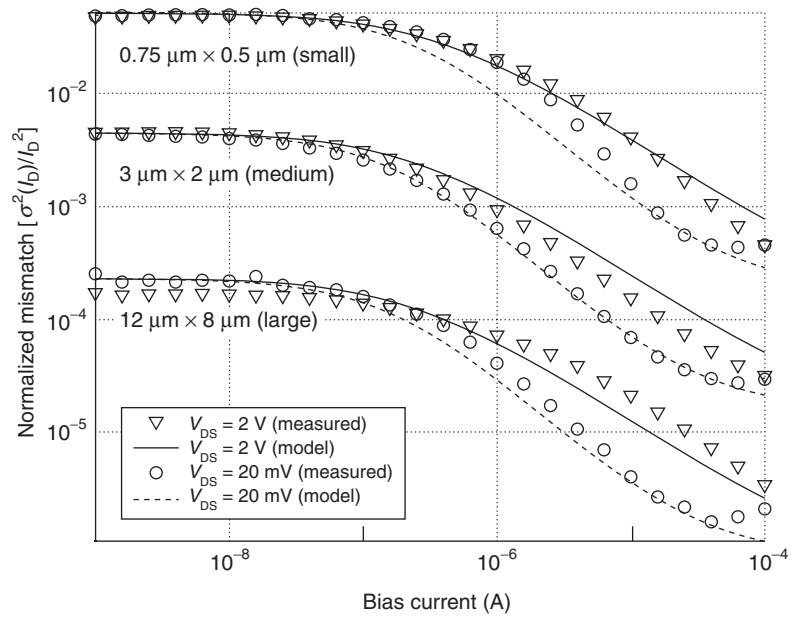
At inversion level $i_f = 1{,}000$, the mismatch given by Equation 4a deviates considerably from the experimental results. This is due to the rather simplified model we've used thus far. Indeed, when the inversion level is high, the inversion charge layer (channel) provides a shield for the gate bulk electric field. This reduces the influence of random dopant placement on mismatch, making the effects of other mismatch components—variation in gate oxide thickness, in mobility, and in slope factor—play a more important role. To account for mismatch factors other than doping fluctuations, we can include the random errors resulting from the normalization sheet current, $I_{SQ} = (1/2)\mu C'_{ox} n\phi_t^2$, as described by Shyu et al.,[1] which results in a modification of Equation 4a, yielding

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{1}{WL}\left[\frac{N_{oi}}{N^{*2}}\frac{1}{i_f - i_r}\ln\left(\frac{1+i_f}{1+i_r}\right) + B^2_{I_{SQ}}\right] \quad (6)$$

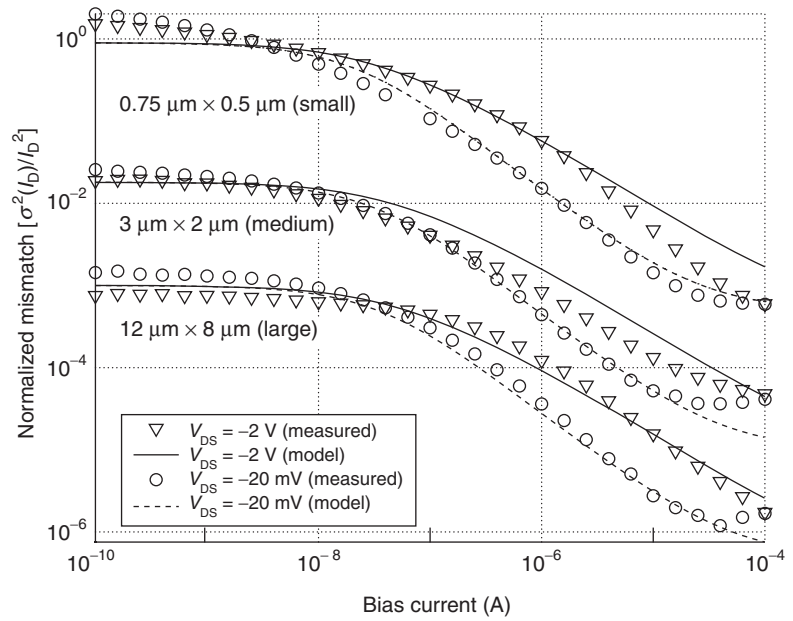
where $B_{I_{SQ}}$ is a mismatch factor that accounts for variations in the normalization current.

Therefore, for high inversion levels, mismatch flattens out at a minimum value determined by $B_{I_{SQ}}$, a result corroborated by the experimental data.

We estimated parameter $B_{I_{SQ}}$ from measurements in strong inversion in the linear region, using Equation 6. $B_{I_{SQ}}$ on the order of 0.89 %-µm and 0.71 %-µm (a relative variation of drain current, related to the length and width of the MOSFET) resulted for NMOS and PMOS devices, respectively, for both large and medium-size devices. The simulated curves shown in Figures 8 and 9 are based on the values extracted for both N_{oi} and $B_{I_{SQ}}$, for either NMOS or PMOS transistors.



(a)



(b)

Figure 9. Dependence of current matching on inversion level (bias current I_B) in linear and saturation regions ($|V_{DS}|$ = 20 mV and $|V_{DS}|$ = 2 V, respectively, where V_{DS} is the drain-to-source voltage) for the large, medium-size, and small NMOS transistor arrays (a) and PMOS transistor arrays (b).

Figure 9 shows the measured and simulated dependence of current matching on inversion level (or bias current I_B) for the linear and saturation regions for three sizes of NMOS and PMOS transistors.

From Figure 9, we see that larger transistors follow the area rule, as our model shows. We also used the same $B_{I_{SQ}}$ value for modeling the matching of both the large and medium-size devices. Small transistors don't follow

this rule, resulting in a mismatch 55% lower (NMOS) and 80% higher (PMOS) than the model estimates using the same N_{oi} that we used for the large and medium-size transistors. However, to obtain better fitting of the curves, we chose different N_{oi} values for the small transistors than those measured for the large transistors. For the dies we characterized, small transistors presented an unpredictable N_{oi}. In fact, electrical characteristics of short-channel devices are very sensitive to fluctuations because of a greater dependence on edge effects. This high sensitivity of short-channel devices is one of the main difficulties in modeling mismatch, particularly in today's complex submicron technologies. Also, for minimum-length devices, drain and source doped regions are very close to one another, strongly affecting the shape of the depletion layer below the channel.

The behavior of the curves in Figure 9 resembles that seen in 1/*f* noise characterization.[9] This indicates that mismatch and 1/*f* noise both arise from the same mechanism, although the first is related to random doping density fluctuation and the second to random trapping/detrapping of carriers in the channel oxide-substrate interface.

Our measurements span a wide range of six decades of current, going from very weak to very strong inversion, and they fit the mismatch over this entire current range. Also, we've demonstrated the accuracy of our mismatch model for both the linear and the saturation regions. We could attain greater accuracy using better-fitting parameters, but we prefer to keep our mismatch model simple, making it a useful, uncomplicated design tool that requires only two parameters (N_{oi} and $B_{I_{SQ}}$) to interface technology with designers.

Our new compact model surpasses traditional mismatch models and is valid for any operating condition, from weak to strong inversion and from the linear to the saturation region, and it also retains consistency for series association of devices. Its simplicity, resulting from the use of only two technological parameters, makes this model a powerful hand-design tool. We are working on a version of the model adequate for deep-submicron technologies for use in circuit simulators. ■

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