MOSFET MODELING FOR RF CIRCUIT DESIGN

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ABSTRACT

In this paper, we discuss some important issues in MOSFET modeling for radio-frequency (RF) integrated-circuit (IC) design. We start with the introduction of the basics of RF modeling. A simple sub-circuit model is presented with comparisons of the data for both y parameter and f_T characteristics. Good model accuracy is achieved against the measurements for a 0.25μm RF CMOS technology. The high frequency (HF) noise modeling issues are also discussed. A methodology to extract the channel thermal noise of MOSFETs from the HF noise measurements is presented and the concept of induced-gate noise is discussed briefly. The results of different noise modeling approaches are also given with the comparison of the measured data, with which the prediction capability of the HF noise behavior of any modeling approach can be examined.

I. INTRODUCTION

With the fast growth of the radio frequency (RF) wireless communications market, RF designers have begun to explore the use of CMOS in RF circuits. Accurate and efficient RF MOSFET models are required. It has been known that a device model emphasizing on the low frequency applications cannot be used directly in RF [1]. Compared with the MOSFET modeling at low frequency, compact RF models are more difficult to develop and do not exist in present commercial circuit simulators. Many microwave circuit designers' use a table-look-up approach based on measurements. However, this approach requires a large database obtained from numerous device measurements, and becomes prohibitively complex when used to simulate highly integrated CMOS RF circuits.

Recently, work has been reported to model the RF performance of submicron MOS devices [1-5]. Basically, they are all developed with the subcircuit approach by adding parasitic components to a core intrinsic MOSFET model. They have demonstrated good accuracy up to 10GHz. However, there are still a lot of issues to be studied, and some examples are now listed. (1) The added parasitic components should be physics-based and linked to process and geometry information to ensure the scalability and prediction capability of the model. (2) Simple sub-circuits are preferred to reduce the simulation time. (3) Clear and efficient parameter extraction methodologies should be developed. (4) HF behavior related to the thermal noise should be investigated. (5) Efficient models for NQS effects are required.

In this paper, we discuss some issues that must be properly accounted for in modeling a MOSFET at RF, and present a simple sub-circuit MOSFET model. The model is accurate in y-parameters (up to the $\frac{1}{2}f_T$ frequency range) and f_T characteristics in the device geometry range interested in RF IC. Further, we present a methodology to extract the channel thermal noise that is important in HF noise modeling. The simulation results of different noise modeling approaches are demonstrated with the measured data.

II. MOSFET MODELING AT RF

1. Modeling of Parasitics

As shown in Fig. 1, a four terminal MOSFET contains many parasitic components, such as the gate resistance R_g, gate/source overlap capacitance C_{gso}, gate/drain overlap capacitance C_{gdo}, gate/bulk overlap capacitance C_{gbo}, source series resistance R_s, drain series resistance R_d, source/bulk junction diode D_{sb}, drain/bulk junction diode D_{db}, and substrate resistances R_{sb}, R_{db} and R_{dsb}. They will influence significantly the device performance at high frequency.

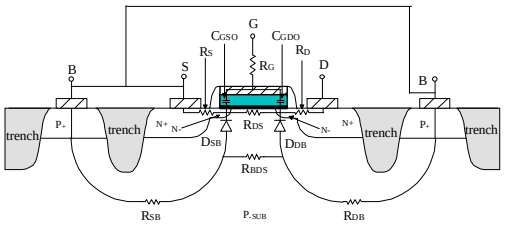

Fig. 1 A MOSFET schematic cross-section with the parasitic components.

(a) Gate Resistance: The gate resistance consists mainly of the poly-silicon sheet resistance. The typical sheet resistance for a polysilicon gate ranges between 20-40 Ω/square, and can be reduced by a factor of 10 with a silicide process, and even more with a metal stack process.

Signal delay at the gate due to the distributed transmission line effect at high frequency has been studied. A factor of 1/3 or 1/12 is introduced, depending on the layout structures of the gate connection, to account for the distributed RC effects when calculating the gate resistance at RF. This effect will become more severe as the gate width becomes wider and the operation frequency becomes higher. So multi-finger devices are used in the

circuit design with narrow gate widths for each finger to reduce the influence of this effect. Complex numerical models for the gate delay have been proposed. However, a simple gate resistance model with the factor of 1/3 or 1/12 for the distributed effect has been found accurate up to $\frac{1}{4}f_T$ [11], even though additional bias dependence of the gate resistance may need to be included to account for the non-quasi-static effect (NQS) effect.

The NQS effect or the distributed RC effect of the channel is another effect that should be accounted for in modeling the HF behavior of a MOSFET. It has been proposed that an additional component is added to the gate resistance to represent the channel distributed RC effect as shown in Fig. 2 [7]. When a MOSFET operates at high frequency, the contribution to the effective gate resistance is not only from the physical gate electrode resistance but also from the distributed channel resistance, which can be "seen" by the signal applied to the gate. Thus, the effective gate resistance R_g consists of two parts: the distributed gate electrode resistance (R_{geltd}) and the distributed channel resistance seen from the gate (R_{gch}), which is a function of biases [7]. This bias dependent R_g model is one of the approaches to account for the NQS effect, as we will discuss again later.

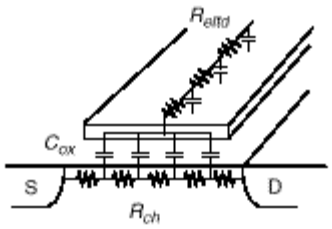

Fig. 2 Illustration of gate electrode resistance R_{geltd}, channel resistance R_{ch} , and gate capacitance C_{ox} [7].

(b) Source and Drain Resistances: The source and drain resistances consist of several parts in an IC MOSFET, such as the via resistance, the salicide resistance, the salicide-to-salicide contact resistance, and the sheet resistance in LDD region, etc. However, the total resistance is usually dominated by the contact and LDD sheet resistances. The typical value of the sheet resistance is around 1kΩ/square in LDD region for a typical 0.25μm CMOS technology.

It has been known that the source/drain resistances are bias dependent. In some compact models such as BSIM3v3 [8], these bias dependencies are included. However, these parasitic resistances are treated only as virtual components in the *I-V* expressions of BSIM3 to account for the DC voltage drop across these resistances and therefore they are invisible by the signal in the ac simulation. External components for these series resistances need to be added outside the intrinsic model to accurately describe the noise characteristics and the input AC impedance of the device [9].

(c) Substrate Resistance: The influence of the substrate resistance can be ignored in the compact model for digital and analog circuit simulation at low frequency. However, at high frequencies, the signal at the drain couples to the source and bulk terminals through the source/drain junction capacitance and the substrate resistance. The substrate resistance influences mainly the output characteristics, and can contribute as much as 20% or more of the total output admittance [9]. Recently, work on the modeling of substrate components are reported. Several different substrate networks have been proposed to account for the influence of substrate resistance at RF [1-5, 9, 10].

An equivalent circuit (EC) for the substrate network is proposed to describe the HF substrate-coupling-effect (SCE), as shown in Fig. 3 (a). With a further approximation, a single resistor substrate network, as shown in Fig. 3 (b), can be obtained based on the y-parameter analysis of the substrate network in Fig. 3 (a) [11], which has been used in RF modeling with good accuracy up to 10GHz [10].

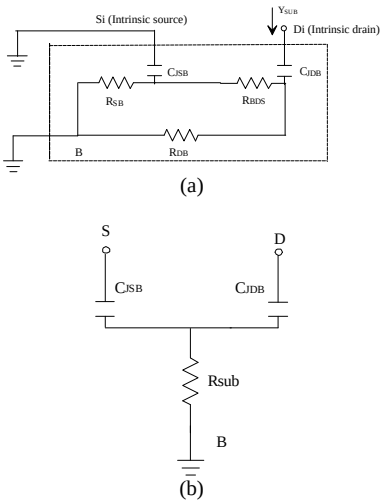

Fig. 3 Proposed equivalent circuit for substrate network. C_{jsb} and C_{jdb} are capacitances of source/bulk and drain/bulk junctions.

Analytical model equations can be found for the substrate resistance components R_{sb}, R_{dsb}, and R_{db} respectively, which are functions of process and layout parameters such as substrate doping concentration, the space and depth of field (or trench) isolation, etc. The substrate resistance R_{sub} in Fig. 3(b) is an equivalent resistance to R_{db}, R_{sb}, and R_{dsb}.

(d) Parasitic Capacitances: The parasitic capacitances in a MOSFET can be divided into five components: 1) the outer fringing capacitance between the polysilicon gate and the source/ drain, C_{FO}; 2) the inner fringing

capacitance between the polysilicon gate and the source/drain, C_{FI}; 3) the overlap capacitances between the gate and the heavily doped S/D regions (and the bulk region), C_{GSO} & C_{GDO} (C_{GBO}), which are relatively insensitive to terminal voltages; 4) the overlap capacitances between the gate and lightly doped S/D region, C_{GSOL} & C_{GDOL}, which changes with biases; and 5) the source/drain junction capacitances, C_{JD} & C_{JS}. Most of them have been modeled for digital/analog circuit simulation. It would be preferred that these capacitance models are still applicable to RF simulation. For that purpose, an efficient and correct parameter extraction methodology considering the cases for both low frequency and RF is needed. However, additional parasitic capacitance models may have to be developed if the present models can not meet the requirements at RF [9].

2. Modeling of NQS Effects

Most MOSFET models available in circuit simulators use the quasi-static (QS) approximation. In a QS model, the channel charge is assumed to be a unique function of the instantaneous biases: i.e. the charge has to respond a change in voltages with infinite speed. Thus, the finite charging time of the carriers in the inversion layer is ignored. In reality, the carriers in the channel do not respond to the signal immediately, and thus, the channel charge is not a unique function of the instantaneous terminal voltages (quasi-static) but a function of the history of the voltages (non-quasi-static). This problem may become pronounced in RF applications, where the input signals may have rise or fall times comparable to, or even smaller than, the channel transit time. For long channel devices, the channel transit time is roughly inversely proportional to (V_{gs}-V_{th}) and proportional to L^2. Because the carriers in these devices cannot follow the changes of the applied signal, the QS models may give inaccurate or anomalous simulation results that cannot be used to guide circuit design.

The NQS effect can be modeled with different approaches for RF applications: (a) R_g approach in which a bias-dependent gate resistance is introduced to account for the distributed effects from the channel resistance as discussed earlier [7], (b) R_i approach in which a resistance R_i (well-used in modeling a MESFET) is introduced to account for the NQS effect [12], (c) transadmittance approach in which a voltage-control-current-source (VCCS) is connected in parallel to the intrinsic capacitances and transconductances to model the NQS effect at the 1st-order [9], and (d) core model approach in which the NQS effect can be modeled in the core intrinsic model [8]. It should be pointed out that all of these approaches will have to deal with a complex implementation.

Both R_g and R_i approaches will introduce additional resistance besides the existing physical gate and channel resistance, so the noise characteristics of the model using either R_g or R_i approach need to be examined. We will further discuss this issue in the HF noise modeling section. Ideally, the NQS effect should be included in the core intrinsic model if it can predict both NQS and noise characteristics without a large penalty in the model implementation and simulation efficiency.

In Fig. 4, simulation results of a RF model, to be discussed next section, with and without NQS effects are shown with a comparison to the measured data. In this example, the NQS effect is modeled by the intrinsic model of BSIM3v3 with the NQSMOD=1 [8]. Without considering the NQS effect, the model cannot predict the measured Y_{21} at higher frequency range. The inclusion of the NQS effect would be a desirable feature for a RF model even though it remains a question whether the devices in RF circuits for small-signal applications will operate in the frequency region at which the devices show significant NQS effects.

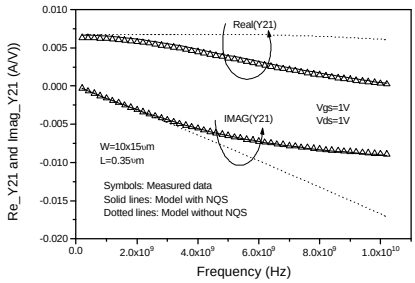

Fig. 4 Comparison of models with and without NQS effect and measured data.

3. Subcircuit RF Model

Based on the above analysis, a complete subcircuit model for RF MOSFETs is given in Fig. 5 (a). This is a simple four-external-resistor model. The core intrinsic model can be any MOSFET model that is used for analog applications, and here it is BSIM3v3, which has included a bias-dependent overlap capacitance. The EC for the RF MOSFET model is given in Fig. 5 (b).

The model has been examined at different bias conditions, and shows satisfactory agreement to experiments. As an example, Fig. 6 shows the comparison of the y-parameter characteristics between measurements and the model for a three finger device with W_f/L_f=12/0.36 at V_g=V_d=1.5V. Good match between the model and data shows the simple EC model can work up to 10GHz, which is about half of f_T for the given device. Fig.7 gives the comparison of f_T-I_D characteristics

between the model and measurements for different devices.

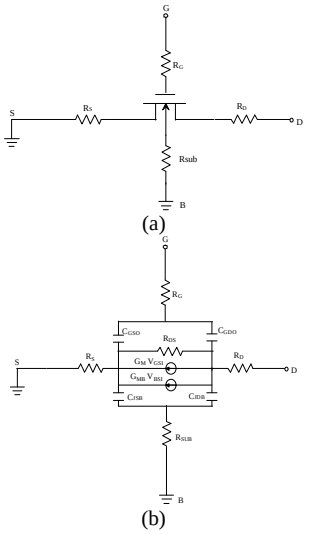

Fig.5 (a) A simple four external resistor RF model; (b) Equivalent circuit for the RF model.

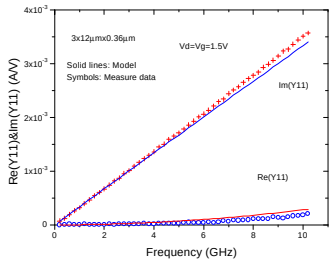

Fig. 6 (a) Comparison of the Y_{11} characteristics between the model and measured data for a three finger device with W/L=12/0.36 at Vg=Vd=1.5V.

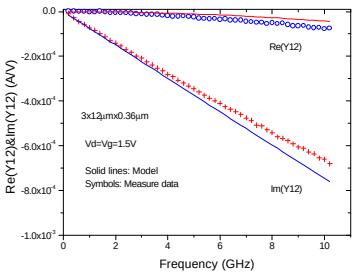

Fig. 6 (b) Comparison of the Y_{12} characteristics for the three finger device with W/L=12/0.36 at V_g=V_d=1.5V

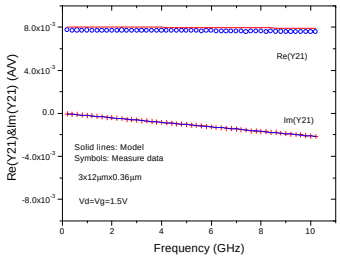

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Fig. 6 (c) Comparison of the Y_{21} characteristics for the three finger device with W/L=12/0.36 at V_g=V_d=1.5V.

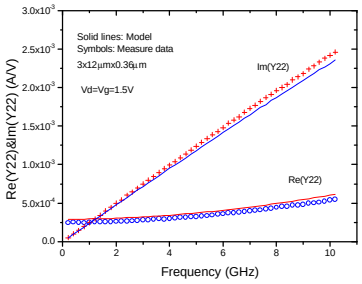

Fig. 6 (d) Comparison of the Y_{22} characteristics for the three finger device with W/L=12/0.36 at V_g=V_d=1.5V.

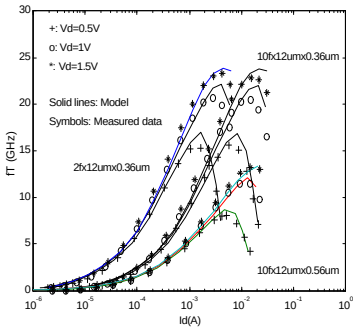

Fig. 7 Comparison of f_T-I_D characteristics between the model and measurements for different devices.

III. HF NOISE MODELING

Different noise sources associated with terminal resistances, channel resistance exist in a MOSFET. In this paper, we introduce a methodology to extract the channel thermal noise of MOSFETs from the HF noise measurements. Also, we discuss the issue of induced-gate noise that has been discussed recently.

1. Channel Thermal Noise

(a) The Extraction of Channel Thermal Noise

A noisy two-port may be represented by a noise-free two-port and two current noise sources as shown in Fig. 8 (a), and these two noise sources are usually correlated with each other. From the *y*-parameters of the two-port and the noise source information (i_1, i_2 and the their correlation term), we may evaluate the noise parameters of the two-port by transforming the noisy two-port to a noise-free two-port with a noise current and a noise voltage source at the input side of the two-port (Fig. 8(b)). The HF noise sources in a MOS transistor include the contributions from the terminal resistances at the gate, source and drain, the channel resistance, and the substrate resistances. Fig. 9 shows the complete equivalent noise circuit model for a MOSFET operated at RF. However, at low frequency, the equivalent noise circuit model can be simplified (shown in Fig. 10) and the power spectral

density of the noise current source i_2 defined in Fig. 8 (a) can be obtained from

$$\frac{\overline{|i_2|^2}}{\Delta f} = \overline{|u|^2} \cdot |y_{21}|^2 = 4kTR_n|y_{21}|^2 \qquad (1)$$
$$= \frac{\overline{|i_{Gout}|^2}}{\Delta f} + \frac{|i_{Sout}|^2}{\Delta f} + \frac{|i_{Dout}|^2}{\Delta f} + \frac{|i_{dout}|^2}{\Delta f}$$

where i_{Gout}, i_{Sout}, i_{Dout} and i_{dout} are the noise currents contributed at the output port by gate resistance (R_{G}), source and drain resistances (R_{S} and R_{D}), and the channel thermal noise (i_{d}), respectively. The noise contribution from the substrate resistance R_{sub} is ignored in eqn. (1) because of the "open" junction capacitances at DC or low frequency, which is the assumption in this derivation. By calculating the noise contribution from each noise source analytically and substituting i_{Gout}, i_{Sout}, i_{Dout} and i_{dout} in eqn. (1), the power spectral density of the channel thermal noise in MOSFETs can be extracted according to the following equation

$$\overline{|i_d|^2} = 4kT\left[(R_{n0} - R_G - R_S)g_m{}^2 - \frac{2g_mR_S}{R_{DS}} - \frac{R_D + R_S}{R_{DS}{}^2}\right] \quad (2)$$

where R_{no} is the equivalent noise resistance extrapolated at DC or measured at low frequencies.

In order to obtain the model element values in eqn. (2), values of parameters R_{G}, R_{S}, R_{D}, g_m and R_{DS} are extracted with the measured S-parameters. The methodology of directly extracting these parameters has been reported [9]. Based on these extracted parameters and eqn. (2), the channel thermal noise can be calculated from the measured HF noise characteristics [13]. The extracted HF noise parameters can be used to verify the noise predictive capability of models available in circuit simulation [14].

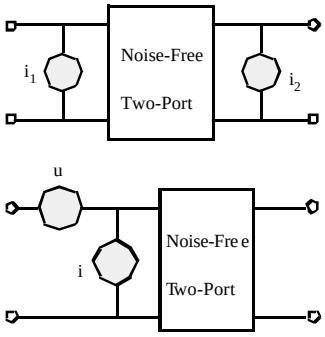

Fig. 8 Different representations of noisy two-port networks.

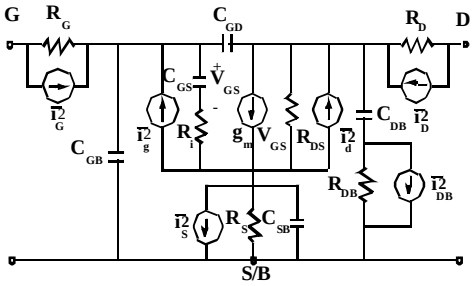

Fig. 9 Equivalent noise circuit model for an intrinsic MOSFET.

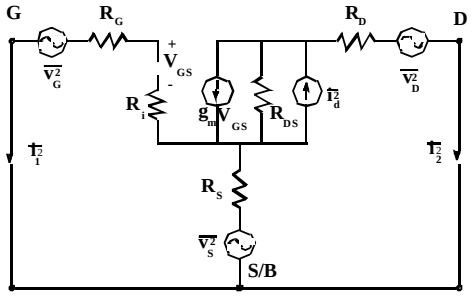

Fig. 10 Simplified equivalent noise model at DC or lower frequency.

(b) Comparison of Different Noise Models

With the extracted parameters from the measured data for a 0.25μm RF CMOS technology, we compared the calculated results of the noise characteristics for the equivalent circuit given Fig. 9 at different configuration cases. One is called R_g approach, that is, we set R_i in Fig. 9 to zero and extract the R_g with the measured s-parameters for the noise calculation. One is called R_i approach, that is, we extract both R_g and R_i with the measured s-parameter data for the noise calculation. The calculated results of both R_g and R_i approaches for four noise parameters are given in Fig. 11 against the measured data for a 0.36um device at V_g=1.2V and V_d=1V. It shows that the R_g approach gives better noise prediction with the R_g value extracted from the measured $Re\{Y_{11}\}$.

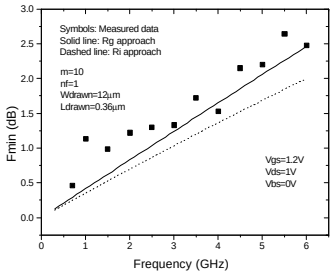

Fig. 11 (a) Comparisons of measured data for minimum noise figure, F_{min}, with simulations from both R_g and R_i approaches with extracted $|i_d|^2$.from eqn. (2). The m in the figure is the numbers of the devices connected in parallel. The nf is the finger number of each device. Each device (single finger here) is with the channel width of 12μm and channel length of 0.36um.

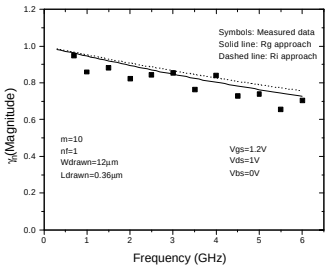

Fig. 11 (b) Comparisons of measured data for the magnitude of the optimized source reflection coefficient, γ_n, with simulations from both R_g and R_i approaches.

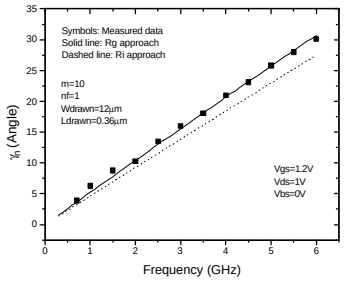

Fig. 11 (c) Comparisons of measured data for the phase of the optimized source reflection coefficient, γ_n, with simulations from both R_g and R_i approaches.

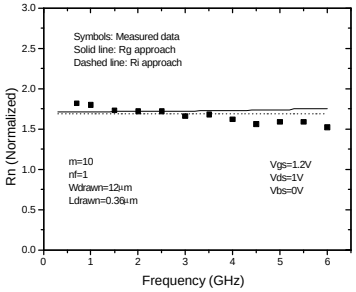

Fig. 11 (d) Comparisons of measured data for the noise resistance normalized to 50Ω, R_n, with simulations from both R_g and R_i approaches.

2. Induced-Gate Noise

The concept of the induced-gate noise has been introduced for three decades [13]. But it is still an issue that many researchers are debating the existence of this noise source. At high-frequencies, it is believed that the local channel voltage fluctuations due to thermal noise couple to the gate through the oxide capacitance and cause an induced gate noise current to flow [13, 15]. This noise current can be modeled by a noisy current source connected in parallel to the intrinsic gate-to-source capacitance C_{gsi}. Since the physical origin of the induced gate noise is the same as for the channel thermal noise at the drain, the two noise sources are partially correlated with a correlation factor [16].

Currently, the induced gate noise and moreover its correlation to the thermal noise at the drain are not implemented completely in compact models yet. One reason is due to the difficulty of modeling the induced-gate noise, and another reason is that it is probably not very critical at frequencies much smaller than the device f_T, since besides the thermal noise at the drain, the other most important contributors to the total noise are the substrate and the gate resistances. Recently, some people even claim that the induced-gate noise does not exist by some derivation theoretically. Currently, a further detailed investigation is needed to understand the induced-gate noise issue and model it correctly if it does exist.

IV. CONCLUSIONS

In this paper, we have discussed some important issues in RF MOSFET modeling. The modeling of parasitic components in MOSFETs is necessary to describe the HF behavior of MOS devices at GHz frequency. An accurate RF MOSFET model with a simple substrate network is presented. The model has been verified by high frequency (HF) measurements. Good model accuracy at different bias conditions has been found for devices with different channel length (L), width (W) and fingers. The developed RF MOSFET model can be the basis of a predictive and statistical modeling approach for RF applications.

The modeling approaches of NQS effects have been analyzed. A RF model including the NQS effect is desirable without introducing complex implementation and simulation time penalty.

The HF noise modeling is also discussed. A methodology of extracting the channel thermal noise parameters is introduced, with which the correctness of the noise sources introduced in a RF model can be examined. The results of noise models with different equivalent circuits are shown with the comparisons of the measured data. The equivalent circuit with the R_g value extracted from $Re\{Y_{11}\}$ gives better noise prediction. The concept of the induced-gate noise is briefly introduced without further theoretical analysis and experimental investigation. It is still an issue to be studied for its existence, the correlation with channel thermal noise and its influence to the circuits at RF.

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