

# **MOSFET MODELS FOR SPICE SIMULATION, INCLUDING BSIM3v3 AND BSIM4**

---

**WILLIAM LIU**

Texas Instruments



A Wiley-Interscience Publication

**John Wiley & Sons, Inc.**

New York • Chichester • Weinheim • Brisbane • Singapore • Toronto

# CONTENTS

<b>Preface</b>	<b>xi</b>
<b>1 Modeling Jargons</b>	<b>1</b>
1.1 SPICE Simulator and SPICE Model,	1
1.2 Numerical Iteration and Convergence,	8
1.3 Digital vs. Analog Models,	11
1.4 Smoothing Function and Single Equation,	27
1.5 Chain Rule,	36
1.6 Quasi-Static Approximation,	38
1.7 Terminal Charges and Charge Partition,	44
1.8 Charge Conservation,	50
1.9 Non-Quasi-Static and Quasi-Static $y$ -Parameters,	62
1.10 Source-Referencing and Inverse Modeling,	70
1.11 Physical Model and Table-Lookup Model,	77
1.12 Scalable Model and Device Binning,	86
References and Notes,	98

<b>2 Basic Facts About BSIM3</b>	<b>101</b>
2.1 What Is and What's Not Implemented in BSIM3, 101	
2.2 DC Equivalent Circuit Model, 104	
2.3 BSIM3's $y$ -Parameters, 116	
2.4 Large-Signal Equivalent Circuit, 122	
2.5 Small-Signal Model, 133	
2.6 Noise Equivalent Circuit, 140	
2.7 Special Operating Conditions: $V_{DS} < 0$ , $V_{BS} > 0$ , $V_{GS} < 0$ , or $V_{BD} > 0$ , 149	
References and Notes, 156	
<b>3 BSIM3 Parameters</b>	<b>158</b>
3.1 List of Parameters According to Function, 158	
3.2 Alphabetical Glossary of BSIM3 Parameters, 162	
3.3 Flow Diagram of SPICE Simulation, 275	
References and Notes, 283	
<b>4 Improvable Areas of BSIM3</b>	<b>284</b>
4.1 Lack of Robust Non-Quasi-Static Models: Transient Analysis, 285	
4.2 Problem with the 40/60 Partition: The “Killer NOR Gate”, 299	
4.3 Lack of Channel Resistance (NQS Effect; Small-Signal Analysis), 303	
4.4 Incorrect Transconductance Dependency on Frequency, 313	
4.5 Lack of Gate Resistance (and Associated Noise), 316	
4.6 Lack of Substrate Distributed Resistance (and Associated Noise), 323	
4.7 Incorrect Source/Drain Asymmetry at $V_{DS} = 0$ , 329	
4.8 Incorrect $C_{gb}$ Behaviors, 333	
4.9 Capacitances with Wrong Signs, 339	
4.10 $C_{gg}$ Fit and Other Capacitance Issues, 341	
4.11 Insufficient Noise Modeling (No Excess Short-Channel Thermal Noise), 356	
4.12 Insufficient Noise Modeling (No Channel-Induced Gate Noise), 362	
4.13 Incorrect Noise Figure Behavior, 366	

4.14	Inconsistent Input-Referred Noise Behavior,	375
4.15	Possible Negative Transconductances,	376
4.16	Lack of GIDL (Gate-Induced Drain Leakage) Current,	382
4.17	Incorrect Subthreshold Behaviors,	387
4.18	Threshold Voltage Rollup,	390
4.19	Problems Associated with a Nonzero RDSW,	391
4.20	Other Nuisances,	392
	References and Notes,	396
<b>5.</b>	<b>Improvements in BSIM4</b>	<b>399</b>
5.1	Introduction,	399
5.2	Physical and Electrical Oxide Thicknesses,	400
5.3	Strong Inversion Potential for Vertical Nonuniform Doping Profile,	402
5.4	Threshold Voltage Modifications,	403
5.5	$V_{GST,\text{eff}}$ in Moderate Inversion,	408
5.6	Drain Conductance Model,	409
5.7	Mobility Model,	412
5.8	Diode Capacitance,	414
5.9	Diode Breakdown,	417
5.10	GIDL (Gate-Induced Drain Leakage) Current,	425
5.11	Bias-Dependent Drain-Source Resistance,	427
5.12	Gate Resistance,	431
5.13	Substrate Resistance,	434
5.14	Overlap Capacitance,	435
5.15	Thermal Noise Models,	436
5.16	Flicker Noise Model,	450
5.17	Non-Quasi-Static AC Model,	451
5.18	Gate Tunneling Currents,	459
5.19	Layout-Dependent Parasitics,	465
	References and Notes,	472

<b>Appendices</b>	<b>473</b>
A BSIM3 Equations,	473
B Capacitances and Charges for All Bias Conditions,	507
C Non-Quasi-Static $y$ -Parameters,	510
D Fringing Capacitance,	515
E BSIM3 Non-Quasi-Static Modeling,	519
F Noise Figure,	522
G BSIM4 Equations,	528
<b>Index</b>	<b>583</b>