Multi-carrier single-DAC transmitter approach applied to digital cable television

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List of abbreviations

ACLR	Adjacent Channel Leakage Ratio
BER	Bit Error Rate
CATV	Cable Television
CIC	Cascaded Integrator Comb
CM	Cable Modem
CML	Current Mode Logic
CMTS	Cable Modem Termination System
CORDIC	COordinate Rotation DIgital Computer
CSD	Canonical signed digit
CSO	composite second order
CTB	composite triple beat
DDS	Direct digital synthesizer
DNL	Differential nonlinearity
DOCSIS	Data Over Cable Service Interface Specification
DSP	Digital Signal Processor
EMI	Electromagnetic interference
EVM	Error Vector Magnitude
FEC	Forward Error Correction
FoM	Figure of Merit
HFC	Hybrid Fibre-Coaxial
IMD	Intermodulation Distortion
INL	Integral nonlinearity
ISI	Intersymbol Interference
ITRS	International Technology Roadmap for Semiconductors
LUT	Lookup Table
MER	Modulation Error Rate
MSE	mean square error
NCO	Numeric Controlled Oscillator
NORA	No Race Logic
NTSC	National Television System Committee
OFDM	Orthogonal frequency-division multiplexing
OSI	Open Systems Interconnect
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PLL	Phase Lock Loop
PSRR	Power Supply Rejection Ratio
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature phase-shift keying
RRC	Root Raised Cosine
RS	Read-Solomon
RTZ	Return-to-Zero

SDR	Signal-to-distortion ratio
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-noise and distortion ratio
SOI	Silicon on Insulator
SPI	Serial Peripheral Interface
SSB	Single Sideband
TCP	Transmission Control Protocol
THD	Total Harmonic Distortion
TSPC	True Single Phase Clock Logic
VCO	Voltage Controlled Oscillator
VHDL	Hardware Description Language

Contents

1

Introduction

Cable television began its life with antennas and coaxial cables that distributed the TV signal inside buildings and remote rural areas in the U.S., on places where reception with consumer antennas was difficult, in the late 1940's. In the Netherlands shortly after the introduction of television in 1951, inhabitants in high rise buildings began to distribute the signal from a central antenna, to reduce the number of antennas needed and to improve the quality of reception. Since the distribution of television signals was monopolized to the PTT, distribution of these signals by other companies or individuals was not allowed. Only central antenna systems inside buildings were tolerated. From the 1970's municipalities were allowed to issue a licence to create a cable network that could cover a small group of homes i.e. less than 100, or the complete town. Since every municipality could issue a single licence, the municipalities themselves often created these cable networks. Later the regulations became more relaxed and municipalities began connecting their networks and more television signals were distributed on them.

In the 90's the distribution of television signals became exempt from licensing, because of European rules. The networks where connected together through optical fibers in a short amount of time. Most of these municipality owned networks where bought by private cable companies that transformed the aged coaxial networks into hybrid-fiber-coaxial (HFC) networks.

Due to the wide spread use of the Cable Television (CATV) networks and the

large amount of unused frequencies the cable industry searched for methods to expand their network utilization. In 1994 the IEEE802.14 working group began the cable standardization work which enabled digital data transport over the traditional analog cable and made two way communication possible. Traditionally the cable network was designed for one-way, broadcast only, traffic. To enable two-way communication, physical modifications, such as bi-directional amplifiers are required. Since the cable network is a broadcast network in which all connected customers receive the same signal, protocols are required to allow point-to-point communication. The Multimedia Cable Network System (MCNS) also began cable standardization in 1995 and produced the first version of the Data Over Cable Service Interface Specification (DOCSIS) [1], which was approved in 1998. Later other versions, DOCSIS 1.1 in 1999 and DOCSIS 2.0 in 2001, where approved that mainly focused on improving the upstream, from customer location to the head-end.

Because of the rapid growth in bandwidth requirements for services such as digital television, internet services and video-on-demand, it became apparent that the bandwidth of a single channel, which is about $42 Mbit/s$ for the U.S. DOCSIS channel, would become insufficient. Therefore, with the introduction of DOCSIS 3.0 in 2007 the ability was added to combine multiple channels as if it were a single channel, thereby allowing bandwidths for customers of 100's of Mbit/s.

1.1 Motivation

The available bandwidth for data traffic downstream and upstream for each customer is inversely proportional to the number of households that are connected, since the cable network is shared with all users that are supplied with the same signal. For a broadcast signal downstream this is no limitation, since the data is equal for all subscribers. For narrowcast data (upstream/downstream), such as internet services or video-on-demand, this can pose a problem. A method to increase the effective network speed is to reduce the number of households that are supplied with the same signal. However, the available equipment nowadays that is required to generate and modulate the signals for the channels that are

broadcasted on the cable network can draw several kW's of power [2], which limits the the number of neighborhood hubs. Therefore, efficient techniques to broadcast vast amounts of data over the cable infrastructure are desired.

1.2 Aim

In the traditional DOCSIS cable transmitter each channel is converted with a digital-to-analog converter to the analog domain and then with a dual conversion transmitter upconverted to the desired RF frequency. In this approach many analog components are required that all require tuning and calibration to ensure correct operation and they have a relative high power consumption to ensure a high signal-to-noise level. In order to transmit multiple channels, a multiple of these upconverters is placed in parallel and their outputs are combined by adding their output signals.

In the proposed method the channels are first upconverted and combined in the digital domain, followed by a single digital-to-analog converter that generates the RF signal without further analog upconversion. The new approach has the advantage that the complexity of the multi-carrier transmitter is reduced because less analog components are required. In addition since this approach uses a lot of digital circuits it allows to take advantage of the scaling of these circuits according to Moore's law, resulting in a significant reduction of the power consumption when many carriers are being broadcasted.

A theoretical study will be made of the consequences of this combining in the digital domain on the properties of the signal that is converted with the DAC. Using these changed properties, requirements will be set on the specifications of the DAC and of the digital signal processing.

Furthermore, the work will study the traditional DAC/mixer combination and the requirements for the individual components that are needed, and from these specifications will be derived. The power consumption of such a transmitter is estimated and is used to compare against the proposed method. The new approach of combining the carriers in the digital signal processing will be analyzed and requirements for the digital signal processing functions will be

defined. Using these requirements the power consumption of the digital circuits will be estimated. A comparison of the power consumption of the two approaches will be made to compare the power efficiency when multi-carriers are being broadcasted.

1.3 Scope

The thesis will use the U.S. version of the DOCSIS standard as a reference. In this version the channels have a bandwidth of $6MHz$, while the European version has channels that are $8MHz$ wide. Also the data rate of the versions is different. For the U.S. version the data rate is about $5.36Mb/s$ when 256-QAM signals are being broadcasted, while the EuroDOCSIS has a data rate of $6.952Mb/s$. Although in this thesis the U.S. version is analyzed, the results will be similar for the EuroDOCSIS version with minor changes.

While in the case that all channels are independently upconverted to their desired RF frequency the channels can be placed anywhere in the band, this is not necessarily the case when carriers are first grouped and then as a group upconverted to the desired RF frequency. For the analysis it is assumed that the channels that are being broadcasted by the transmitter form a continuous block of channels, unless it is stated otherwise.

The analysis of the DOCSIS transmitter will only focus on the circuits that are needed for the IF/RF subsystem, which could be either in the analog domain or in the digital domain. The baseband processing that is required to add error correction, to shape the signal, and to modulate the signals, are outside the scope of this thesis.

1.4 Original contributions

Several original contributions are described and discussed in this thesis. The most important of these are:

- The non-orthogonal combining of the channels as used in the DOCSIS standard is compared to the orthogonal combining of carriers such as used in OFDM modulation systems.

- Analysis of the traditional DOCSIS transmitter architecture and specifications for the individual components that are needed to achieve the required performance.

- Estimation of the minimum power consumption required for the traditional single carrier DOCSIS transmitter.

- Analysis of the changing signal properties when the DAC is placed closer to the output of the transmitter.

- An efficient architecture for the proposed transmitter that combines the carriers in the digital domain and converts this digital RF signal with a single digital-to-analog converter to the analog domain.

- A derivation of the required sample rate for the digital-to-analog converter in the proposed transmitter given the symbol rate and the complexity of the Nyquist filter that follows the DAC.

- Derivation of the requirements for the individual building blocks that are needed for the proposed transmitter architecture.

- Investigation to achieve an efficient method to upsample the digital RF signal at high sample rates.

- Derivation of the Adjacent Channel Leakage Ratio (ACLR) performance of the DAC when it is impaired by limited output impedance and amplitude mismatch of the current sources for wideband signals.

- The impact of the technology scaling of digital circuits made in current mode logic.

- Design of an optimized decoder topology to achieve the high sample rates needed in the system.

1.5 Outline

Chapter 2 will introduce the communication system and the challenges when many channels are combined. The optimal level for amplitude clipping in the case of a limited number of carriers and in the case of many carriers is given. In Chapter 3 the DOCSIS system architecture is introduced and the spectral requirements of a single transmitter that is capable to transmit multiple carriers is calculated. The traditional transmitter for a DOCSIS broadcast system is analyzed in Chapter 4. In addition the minimum power consumption of such a transmitter is derived. In Chapter 5 the advantages of increasing the digitization and of advanced CMOS technologies are explained. These are used to propose the architecture for the 'All-digital' transmitter in Chapter 6. Of this architecture the requirements for the building blocks are studied and the power consumption of these digital circuits is estimated. In Chapter 7 the digital-to-analog converter used in this 'All-digital' transmitter is analyzed and several models are derived to estimate the performance of the DAC in case of imperfections. Using these models an architecture for the DAC is selected and the measurement results of the realized DAC are shown. In Chapter 8 the IC implementations are being discussed and the proposed multi-carrier transmitter architecture is compared against the traditional multi-carrier transmitter. Conclusions are presented in Chapter 9.

2

Multi-carrier broadcast system overview

Nowadays the data rate of communication standards, such as digital television broadcast and internet-through-cable, becomes higher and higher. This increased amount of information has to be transmitted over the available bandwidth as efficiently as possible. This places ever more stringent demands for the components involved for the generation and reception of these signals.

An example of such a standard is DOCSIS (Data Over Cable Service Interface Specification)[3]. This standard is developed to broadcast large amounts of information in a metropolitan area. The DOCSIS standard specifies a frequency range of 54 - $1000MHz$ for the downstream path. This bandwidth is split into many channels, each 6 - $8MHz$ wide, depending on the geographical location.

This chapter describes in the first section the generic communication channel between a transmitter and a receiver for a multi-carrier broadcast system. The second section shows methods to evaluate the quality of the channel between transmitter and receiver. The third section introduces the multi-carrier QAM transceiver. The fourth section describes the signal properties of this multi-carrier signal with its large peak-to-average ratio (Crest factor).

2.1 The communication channel

A generic communication system is shown in Fig. 2.1. All communication systems involve three main components: the transmitter, the channel and the receiver. A message that the transmitter wants to send is encoded and transported through the channel to the receiver which decodes the message again. In the channel various noise sources are present that can corrupt the message. The capacity, C, that a channel has in the presence of noise uncorrelated to the signal, was calculated by Shannon and is given by

$$C = BW \log_2 (1 + SNR), \tag{2.1}$$

where BW is the bandwidth and SNR is the signal to noise ratio, expressed as a power ratio. This equation gives the theoretical limit of the amount of information the channel can transport without errors. However, it does not give information about how this limit can be achieved.

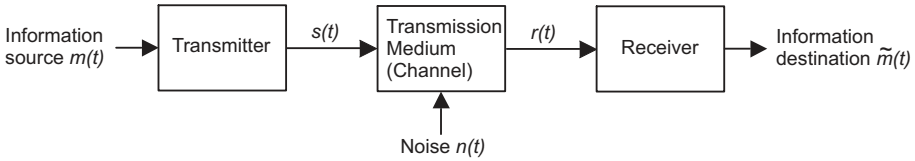


Figure 2.1: Generic communication system, with an generic transmitter and receiver

Signal modulation

The signal can be modulated to transmit as much information as possible in the available bandwidth as is given by equation 2.1. Modulation and demodulation are important functions of the transmitter and receiver.

The modulation of the information can be divided into two categories: analog modulation and digital modulation. Examples of analog modulation are AM, FM and PM; these are mainly used in radio and analog TV broadcast systems and simple local voice communication (walkie-talkies). The main advantage of

analog modulation is the low complexity of the transmitter and the receiver. However, this often comes at the cost of lower spectral efficiency [4].

The processing power of digital circuits follows Moore's Law. Digital modulation benefits from the strive for having more computational power in CMOS technology. With every generation of technology, the possibility to perform complex operations faster and more efficiently, increases. Nowadays, operations, such as filtering, mixing, that where traditionally performed in the analog domain can be performed in digital. It is calculated that the dynamic power consumption per logic transition reduces by a factor 1000 each decade [5].

The power / performance balance of analog circuits develops much slower. According to the International Technology Roadmap for Semiconductors (ITRS), the lines for constant power versus the resolution and signal bandwidth have shifted up by a factor of 10 every decade [6] in the past.

From this gap in improvement it becomes clear that it will be more and more attractive to perform an increasing amount of signal processing in the digital domain. In addition analog signal processing suffers from the following drawbacks

- Aging
- Sensitivity to the environment
- Uncertain performance in production units
- Variation in performance of units
- Sensitivity of analog traces for noise and interference
- Effort to migrate and reuse existing solutions

The digital signal processing does not suffer as much from the above mentioned drawbacks and it can reduce the time needed to realize a product.

QAM modulation

There are many applications in which a vast amount of data has to be transferred from point A to point B. If we restrict ourself to the case that point A and B are connected by a cable, many different methods to transmit the data are possible, depending on the requirements w.r.t. cost, distance, number of users, flexibility, etc.

If the bandwidth efficiency is not that important but low cost has a high priority, as for example is the case in local computer networks, simple forms of baseband modulation are used.

In baseband modulation the complete bandwidth from zero up to the maximum frequency of the medium is used. In the case of 100BASE-T, MLT-3 encoding, which is a kind of 3 level modulation, is used. In the case of 1000BASE-T, 5-level Pulse-Amplitude-Modulation (PAM-5) is used.

As bandwidth efficiency becomes more important, higher levels of modulation can be used. An efficient form of digital modulation is Quadrature Amplitude Modulation (QAM). In QAM both the amplitude and phase of the carrier are modulated. QAM can be seen as two orthogonal signals with PAM modulation, along the I and Q axes respectively, see Fig. 2.2. Because the amplitude and the phase are modulated orthogonal to each other they can be modulated independently, what makes this type of modulation bandwidth efficient.

In general a QAM signal can be expressed as

$$S_m(t) = S_I(t)\cos(2\pi f_c t) + S_Q(t)\sin(2\pi f_c t), \tag{2.2}$$

where $S_m(t)$ is the modulated signal, $S_I(t)$ and $S_Q(t)$ are the I and Q signals to be modulated and f_c is the carrier frequency.

The number of bits transmitted into one symbol is variable. The simplest form of QAM modulation encodes two bits into every symbol, as is shown in Fig 2.2a. More bits can be encoded into one symbol, as is shown in Fig 2.2b, where 4 bits are encoded.

The generic name for this modulation is M-ary QAM, where $M = 2^b$ and b is

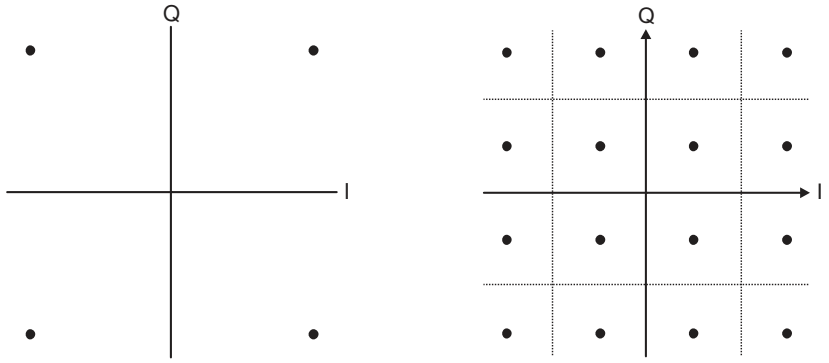


Figure 2.2: Quadrature Amplitude Modulation Constellation for b = 2 (left), 4 (right)

the number of bits that is encoded in one symbol. To keep the Crest factor of the QAM signal small a (near) square constellation is optimal [7]. For every bit more encoded into a symbol the required SNR increases, for equal bit error rate performance, by about $3dB$ [4].

Often the type of QAM modulation where only two bits are encoded into one symbol is called QPSK. In this thesis we will call it 4-QAM to have a more consistent naming when comparing it to higher order QAM.

The symbols inside the constellation, Fig. 2.2, are usually defined by a Gray coding of the input binary data. The advantage of the Gray code mapping is that the Bit Error Rate (BER) is lower with Gray coding than without the Gray code mapping of the symbols. This can be explained as follows. When the signal plus noise exceeds the decision boundary between two symbols at the receiver, as shown with dotted lines in Fig. 2.2, a symbol error occurs. The most likely error is the crossing of one symbol barrier. The receiver decodes this symbol then as a neighbor symbol of the symbol that was sent by the transmitter. With Gray code mapping all symbols that are next to each other differer only in one bit. This is called the Hamming distance and is in this case equal to one. Without Gray code mapping the Hamming distance between two neighboring symbols can be larger than one, and as a result more than one bit error can occur when one symbol is received incorrectly. The probability that the noise and distortion gets larger than two symbol decision boundaries

is much smaller, so therefore it is less probable that more than one bit will be decoded incorrectly.

For odd values of b there is a problem, since the constellation does not allow a fractional number of bits in either dimension. To overcome this, the constellation is chosen to fit the nearest larger available square, with the extreme values removed, as for example is shown in figure 2.3. The non-square constellation diagrams has the disadvantage that full Gray code mapping of the symbols is not possible, while this is possible for the square constellations. The Hamming distance between two neighboring symbols is not always equal to one. The BER for these non-square constellations is therefore relatively larger than for the square constellations. Therefore they are used less often in practice.

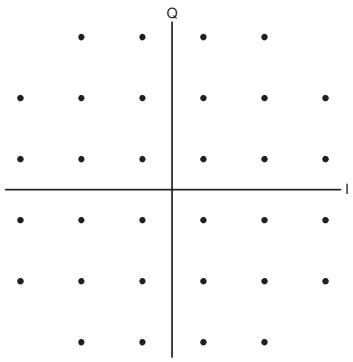


Figure 2.3: Quadrature Amplitude Modulation Constellation for $b = 5$

Wire line communication channels

Wire line communication channels are channels that run between a fixed transmitter and a fixed receiver connected by a cable. These wire line channels can be formed by, for example twisted pairs, wave-guides, optical fibres, and coaxial cables. Whatever the type of channel, its output signal differs from the input signal. The difference can be deterministic or random, but usually it is initially unknown to the receiver. A few examples of channel impairments are dispersion, non-linear distortion and random noise.

In the literature [4], the nature of communication channels is examined in more detail. For example, the dispersive nature of the channel gives rise to Inter Symbol Interference (ISI) leading to imperfect reception at the receiver and mixing of different symbols. This dispersive nature of the channel can be attributed to the non-linear phase shift characteristics of the channel. The effect of ISI can be reduced by dividing the allocated spectrum into a number of carriers. This is known as multi-tone or multi-carrier modulation. For each carrier the narrower spectrum allocated has a more linear group delay.

The always present additive Gaussian noise (AWGN) is a fundamental limiting factor in communications through linear time invariant (LTI) channels. Fixed channels can often be modeled by a linear transfer function that describes the channel dispersion [7]. Although the channel characteristics might change, for example due to aging, temperature changes, etc., these variations will not be apparent in the time span of a typical communication. This inherent time invariance characterizes the fixed channel.

The ideal distortion-free channel would have a flat amplitude response over the used frequency range and a linear phase response over the bandwidth of the signal that is being transmitted. However, the practical channel will always have some non-flat amplitude response and non-linear phase response.

Coaxial cables are suitable for applications that require a large bandwidth. A coaxial cable consists of at least two conductors that are centered around each other (coaxial). The inner conductor is usually a straight wire and the outer conductor is a shield that can be a foil or braided.

Coaxial cables are characterized by their impedance and the loss of the cable. In the normal operation frequency range of a coax cable, usually from 100kHz and up, the impedance is independent of the length of the cable [8]. The characteristic impedance is determined by the size and spacing of the conductors and the dielectric used in between them.

In television applications the characteristic impedance of the coaxial cable is usually 75Ω. An impedance of about 77Ω gives the lowest loss in the cable for any cable with $\varepsilon_r = 1$ (air dielectric) [8]. Commercial CATV cables are filled with PTFE foam, which has a dielectric constant around 1.43. The minimum

Cable type	RG-59 B/U (consumer cable)	RG-11 (professional cable)
Impedance (ohms)	75	75
Conductor material	Copper planted	Copper
Core conductor strand(mm2)	0.58	1.63
Resistance (ohm/km)	159	21
Insulation material	Foam PTFE	Foam PTFE
Insulation diameter (mm)	3.7	7.24
Outer conductor	copper wire braid	Aluminium foil and copper braid
Coverage (%)	95	foil: 100, braid: 61
Resistance (ohm/km)	8.5	4
Outside diameter (mm)	6.15	10.3
Capacitance per meter (pF)	67	57
Attenuation dB/100m		
@ 50 MHz	8	3.3
@ 100 MHz	12	4.9
@ 200 MHz	18	7.2
@ 400 MHz	24	10.5
@ 500 MHz	27.5	12.1
@ 900 MHz	39.5	17.1

Table 2.1: Characteristics of a RG59 B/U and RG-11 coaxial cable

loss impedance is in that case around 64 Ohms. When solid PTFE ($\varepsilon_r = 2.2$) is used the minimum loss occurs near 52 Ohms. A theory why we use 75Ω is given in [9]. Often the center conductor of cheap cables is made of a steel core, with some copper plating. For high frequency signals the resistance per unit length of the coax cable is determined by the circumferential area of the conductor surface due to skin depth effect, not the cross-sectional area. The lower the impedance, the bigger the diameter of the center core. An impedance of 75 Ohms probably was a compromise between low loss and cable flexibility.

Some characteristic properties of two often used coaxial cables, the RG-59 B/U and RG-11, are given in Table 2.1. As can be seen from the table, the attenuation increases with increasing frequency. The attenuation, expressed in dB, increases approximately with the square root of the frequency. Hence for wide band, long distance operation, such as is used in the cable infrastructure

for digital television, channel equalization is required to compensate for the frequency dependent loss.

The QAM transmitter

Commonly used transmitter architectures are the direct conversion transmitter (Homodyne) [10, 11, 12] and the two-step transmitter (Heterodyne) [11, 13, 14, 15, 16, 17].

In Fig 2.4 the principle of a direct conversion transmitter is presented. In a direct conversion transmitter, the baseband signal is directly converted up to the desired RF frequency. This transmitter structure has the advantage that it is relatively simple, as only few components are required.

The data to be transmitted is first split into two streams, the in-phase (I) and quadrature-phase (Q) component. This mapping of the input stream to the two streams is done according to the Gray coding. Then the digital signals are converted into analog signals and the two streams are filtered. This filter shapes the signal to limit the amount of bandwidth needed to transmit the data, as will be shown later this filter is nowadays often implemented in the digital domain to reduce the analog complexity. The filter that is most often used for this shaping is the Root Raised Cosine (RRC) filter. After the signals are filtered, the I and Q data stream signals are modulated on a carriers, the LO, with a 90° phase shift. The I and Q signals then become orthogonal to each other and are summed together. A filter is used to remove the harmonics created by the mixing and finally the signal is amplified. This amplified signal is then sent over the channel, to be received at the other end of the channel by the receiver.

However, the simple direct conversion transmitter suffers from several drawbacks. The practical realization of this architecture is sensitive to imbalance between the mixers amplitude and phase errors of the LO signals and the accuracy of the 90° phase difference between them. This imbalance will lead to LO leakage and reduced suppression of the image frequencies [11]. Additionally, since the frequency of the output signal is equal to the oscillator frequency any coupling between them will influence the local oscillator, which is usually a

VCO (Voltage Controlled Oscillator). This phenomenon is known as injection pulling [11] and will cause the frequency of the local oscillator to differ from its desired frequency.

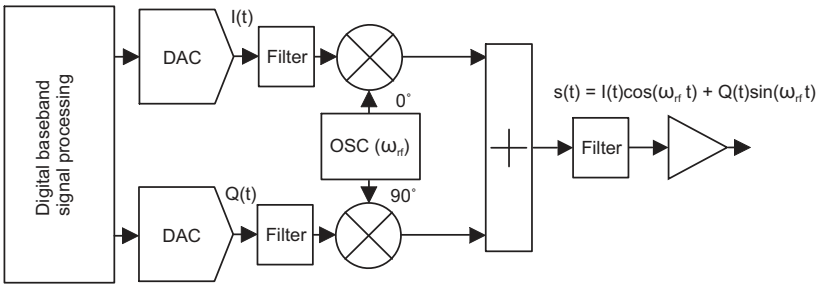


Figure 2.4: Direct conversion transmitter architecture.

One way of reducing the injection pulling is to offset the LO frequency from the output frequency. A frequency offset can for example be generated by doubling/halving the LO frequency and the use of a harmonic mixer. Another method that avoids this problem is the two-step transmitter.

The transmitter architecture, as is shown in Fig. 2.5, is called a two-step transmitter. In this transmitter structure the signal is first upconverted to an intermediate frequency and then upconverted to the desired frequency.

This has several advantages compared to the direct conversion transmitter. First, the frequency at which the I and Q signals are added is lower, which makes it easier to reduce the I/Q imbalance. Second, by using a bandpass filter at the IF stage additional attenuation of the adjacent channel spurs and noise is possible. A disadvantage of this structure is the requirement of steeper analog filters, because the mirror of the signal component is at the $\omega_{rf} - 2\omega_{if}$, which has the same power as the wanted signal at ω_{rf}. To relax the filtering a high ω_{if} is preferred.

The QAM receiver

In figure 2.6 the structure of a QAM receiver is shown. The first stage filters the input RF data stream to attenuate the image frequencies, which would

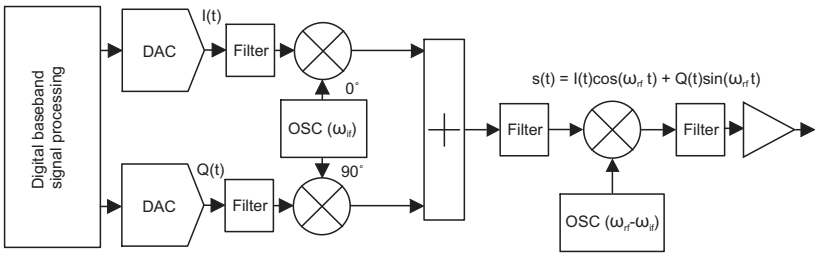


Figure 2.5: Two-step transmitter architecture.

interfere with the wanted signal after the mixer. Then the data stream is down converted to the IF frequency by a mixer, and filtered again to remove the mirror signals. The data is then demodulated by two carriers with a 90° phase shift to recover the I and Q signals. The frequency and phase offset for the generator are extracted from the received signal by the Carrier Recovery loop. After the mixing, filtering is performed to recover the data symbols from the data streams. The used filter is matched to the data symbols to achieve the lowest possible BER, when no interferer is present. The most common filter used for the reception of QAM is the Root Raised Cosine (RRC) filter, which is the same type of filter as is used in the transmitter. After the filtering the levels of the I and Q signals are converted back into bits with a filter and detector and combined into one symbol.

More blocks can be present in the receiver, which are not drawn in this figure. For example, the Variable Gain Amplifier (VGA) with gain control loop and equalizer. The VGA amplifies or attenuates the signal so that the level is optimal for the symbol recovery. An equalizer is also often used to compensate for the impairments present in the channel; this becomes especially important for carriers with a large bandwidth. In addition, some of the blocks drawn in Fig. 2.6 could be implemented in the digital domain, within an Digital Signal Processor (DSP), for example the filter/detector and the carrier recovery, for which the signal must first be converted into a digital signal with an Analog-to-Digital converter.

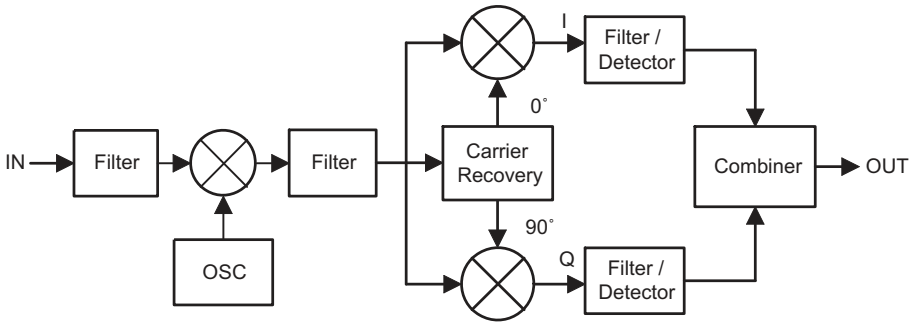


Figure 2.6: Quadrature Amplitude Modulator Receiver

2.2 Signal quality evaluation of QAM signals

The synthesis of communication signals in the digital domain allows the characteristics of these signals to be controlled precisely. Filters that are implemented in the digital domain allow for precise control of their properties, while analog filters always have some inaccuracies due to effects such as mismatch, unwanted coupling, aging, etc. However, non-idealities are generated by the transmitter, the receiver and the channel when this signal is sent. Those imperfections may lead to unpredicted results if they are not well understood and characterized. Analysis of the generation of non-idealities in the DAC and their effect on the resulting signal is important to reduce the risk of not meeting the required system performance.

The quality of the system can be specified in the percentage of communication errors during the transmission of the data. The Bit Error Rate (BER), see Fig. 2.7, is defined as the number of bits that are different between the input and output divided by the total number of bits sent:

$$BER = \frac{n(N)}{N}, \tag{2.3}$$

where $n(N)$ is the number of bits that are different between input and output and N is the total number of bits sent.

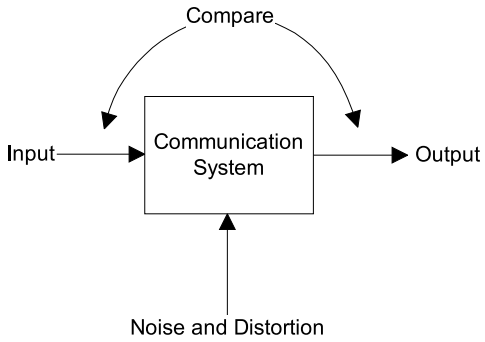


Figure 2.7: Determining the bit-error-rate of a communication system.

Ideally, at the receiver an infinitesimally small sample point will be found in the center of the symbol boundary area in the constellation diagram, see Fig. 2.8. Unfortunately this never occurs in practise, because there is always noise and distortion present. The noise and distortion can become so severe that the received constellation point crosses a decision boundary, see Fig. 2.8. In that case, the output signal does no longer match with the signal at the input of the system.

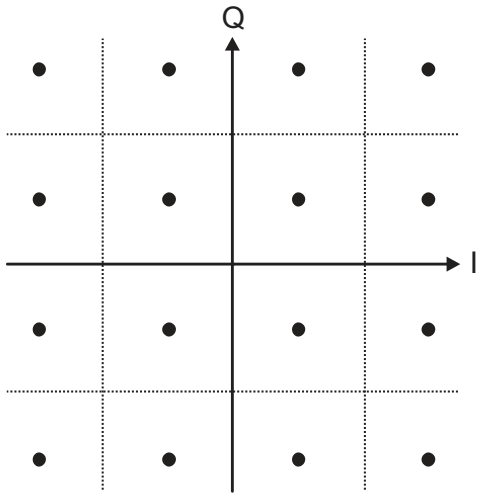


Figure 2.8: A 16-QAM signal with the decision boundaries.

In order to characterize those imperfections, simulations are required. These

simulations must be done with models that contain enough detail to model the limitations correctly. However, especially when the desired accuracy is high or when the likelihood that some events happen is low, these simulations can take a long time to evaluate. In this section several methods are discussed on how this evaluation can be done in a faster way.

One possible way to estimate the Bit Error Rate of a system is to make use of an analytical method. Such a method requires mathematical equations of the non-ideal effects, but these are often too difficult to derive from the system. Therefore, simplifications in the models of these effects are required. Closed form equations only exist for certain types of communication systems. For noise sources this method usually assumes that the most dominant source of bit errors can be modeled as Added White Gaussian Noise (AWGN). Other distributions are hardly used because of the difficulties of the calculations. However, already for a Gray coded M-QAM signal with AWGN it is not easy to obtain an exact closed form result for the average bit error probability for arbitrary M [18]. A quite accurate approximation for the bit error probability of QAM with arbitrary M is given in [19] as

$$P_b(E) \simeq 4\left(\frac{\sqrt{M}-1}{\sqrt{M}}\right)\left(\frac{1}{\log_2 M}\right)\sum_{i=1}^{\sqrt{M}/2} Q\left((2i-1)\sqrt{\frac{3E_b \log_2 M}{N_0(M-1)}}\right), \quad (2.4)$$

where M is the number of bits per symbol, E_b/N_0 is the signal to noise ratio per bit. The $Q(\cdot)$ function is defined as

$$Q(z) \doteq \frac{1}{2} erfc\left(\frac{z}{\sqrt{2}}\right), \quad (2.5)$$

where the cumulative error function is defined as

$$erfc(z) = \frac{2}{\sqrt{\pi}} \int_z^{\infty} e^{-x^2} dx, \quad (2.6)$$

For large SNR the first term of the summation is dominant in which case the

equation simplifies to

$$P_b(E) \simeq 4\left(\frac{\sqrt{M}-1}{\sqrt{M}}\right)\left(\frac{1}{\log_2 M}\right) Q\left(\sqrt{\frac{3E_b \log_2 M}{N_0(M-1)}}\right), \tag{2.7}$$

In addition, it is often assumed that the system is linear, at least from the input of the Gaussian noise till the output. This has two important implications: firstly, linearly filtered Gaussian noise remains Gaussian; and secondly, the superposition theorem holds. With this assumption all the Gaussian noise sources can be recalculated and added to one noise source at the input of the decision device. Although this might give some important information about the expected system performance, effects such as non-linearity in the system are not taken into account. The theoretical BER data is useful for comparison with the simulation results. However, for many problems the analytical method is it too complex to create an equation which has enough detail to describe the real limitations of the system that impact the performance.

The $Q(\cdot)$ function and the $erfc(\cdot)$ function that are used in the equations given before have an integration range that extends until infinity. For numerical integration algorithms this can cause difficulties. Instead of having integration boundaries that reach until infinity, the following approximate expression, that is introduced in [20], is given for the $Q(\cdot)$ function

$$Q(z) \approx \frac{1}{\pi}\int_0^{\pi/2} \exp\left(\frac{-z^2}{2\sin^2(\Phi)}\right) d\Phi, \tag{2.8}$$

for which the integration range is finite.

2.2.1 Monte Carlo analysis to estimate the BER

The most general method to estimate the Bit Error Rate is through Monte Carlo analysis. The Monte Carlo method makes no a priori assumptions, or as little as possible.

The BER of the system is subject to statistical processes, such as the noise injected into various points in the system, non-idealities and the input signal. Because of these statistical processes of both the signal and the non-idealities, a Monte Carlo analysis is often a more viable solution compared to the analytical approach.

The main idea in a Monte Carlo simulation is that each trial takes a random sample from the random processes, signals and noises, that evolve in time bearing whatever statistical properties are ascribed to them [21].

The aim of the Monte Carlo simulation is to determine the chance, p, that a bit will have an error. Since we can not observe p directly, many trials are executed. In these trials the failures and successes, i.e. a bit error or not, are counted. This is called a Bernoulli experiment. The probability distribution of such an experiment is the Binomial distribution. The chance that of these N bits k bits are received incorrectly is given by

$$P_r\{k\} = \binom{N}{k} p^k (1-p)^{N-k}, \tag{2.9}$$

When N is large this equation becomes unpractical to work with. When $N \cdot p > 5$ this discrete distribution can be approximated by the continuous Gaussian distribution. This Gaussian distribution has the expected value $\mu = Np$ and a variance $\sigma^2 = Np(1-p)$. This can be approximated by $\sigma^2 = Np$, because in typical systems the expected p is small, i.e. a low BER.

The method requires no assumptions about the system properties. It only needs to know the relative delay between the input and the output. The system itself is further considered as a blackbox. Comparing the two sequences provides the information of how many bits are received incorrectly.

In the experiment the value of N is known, but the value of p is unknown. By carrying out an experiment with a large enough number of bits N and counting the number of errors, k, an estimate for p results:

$$\hat{p} = \frac{k}{N}. \tag{2.10}$$

The number of symbols, N, that need to be observed in a Monte Carlo simulation for a certain confidence level, can be phrased as k_{req}/p, where p is the true error probability and k_{req} is a constant. The constant k_{req} defines the reliability of the estimate. To estimate p, N bits are being transmitted through the system and compared with their expected values, counting the number of bits that have an error. The simulation can be ended when k_{req} errors are counted.

The higher the value of k_{req} the higher the confidence on the true BER when more symbols are transmitted. When the number of transmitted symbols is $k_{req} = 10$ then the 95% confidence interval is between $0.55\hat{p}$ and $1.8\hat{p}$. Increasing the number to $k_{req} = 100$ improves the 95% confidence interval between $0.8\hat{p}$ and $1.25\hat{p}$, which is a relative minor improvement for 10 times more simulation or measurement time and yet an unacceptable large confidence interval. Increasing the number further gives even less improvement, because the confidence interval improves with $\sqrt{N}$, see Fig. 2.9. Therefore a tradeoff between simulation and measurement time and the confidence of the result is important.

In systems, such as DOCSIS, the BER before error correction should be better than 10^{-8}. To have a Monte-Carlo simulation with a 95% confidence interval of a factor 2, about 10^9 symbols have to be simulated. However in simulation this is not feasible anymore. Therefore other methods to estimate the BER in simulations are required. In measurements achieving the similar accuracy requires for DOCSIS, where the symbol rate is $5.36 MSym/s$, about 180 seconds or 3 minutes, which is easily feasible.

2.2.2 Semi-analytical method to estimate the BER

A method that reduces the drawback of the analytical analysis and the Monte-Carlo method is the semi-analytical method. This approach uses a combination of simulation and analysis to evaluate the performance of the communication system. A similar method was introduced by Matworks in recent versions of the program Matlab in the communication toolbox [22].

The previously described Monte-Carlo method of simulating the performance of the communication system combines the distortion and noise into one sim-

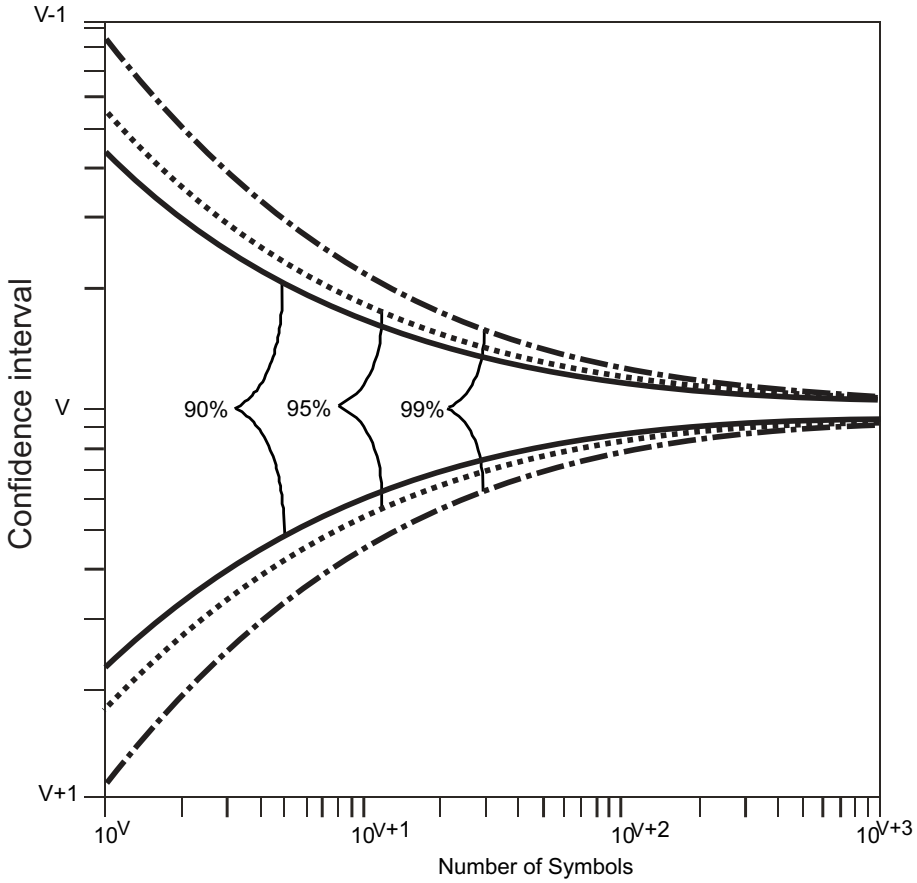


Figure 2.9: Confidence interval on Bit Error Rate when observed BER value is 10^{-v} *for the Monte Carlo technique*

ulation. The main disadvantage of this approach is the long simulation time required, as was shown.

The method described in this section splits the simulation into two steps. In the first step a simulation is performed to assess the distortion of the signal in the communication system without any added noise. The constellation points will no longer coincide with the ideal constellation points due to this distortion, see Fig. 2.10.

As a second step Added White Gaussian Noise (AWGN) is added analytically

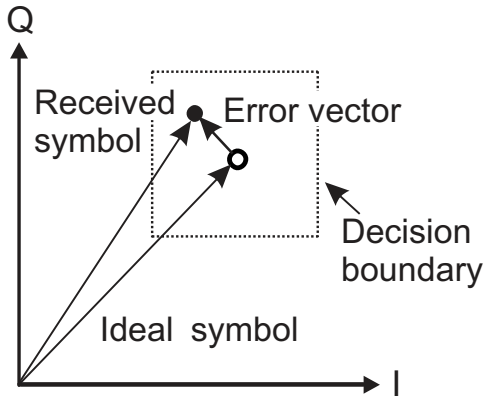


Figure 2.10: Step 1: Distortion in the system causes the received constellation point to move from its ideal location.

around the distorted constellation points. As a consequence of the distortion the received points are closer to the decision boundaries (except for the outer constellation points when they move further away from the origin). Therefore, less noise is required to cross the decision boundary to have a bit error and the BER has increased for a certain SNR, compared to the case where no distortion is present, see Fig. 2.11. The chance that the decision boundary is crossed can be calculated easily.

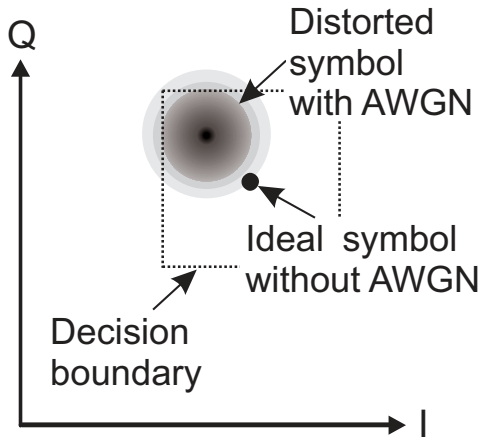


Figure 2.11: Step 2: AWGN added to the distorted constellation point.

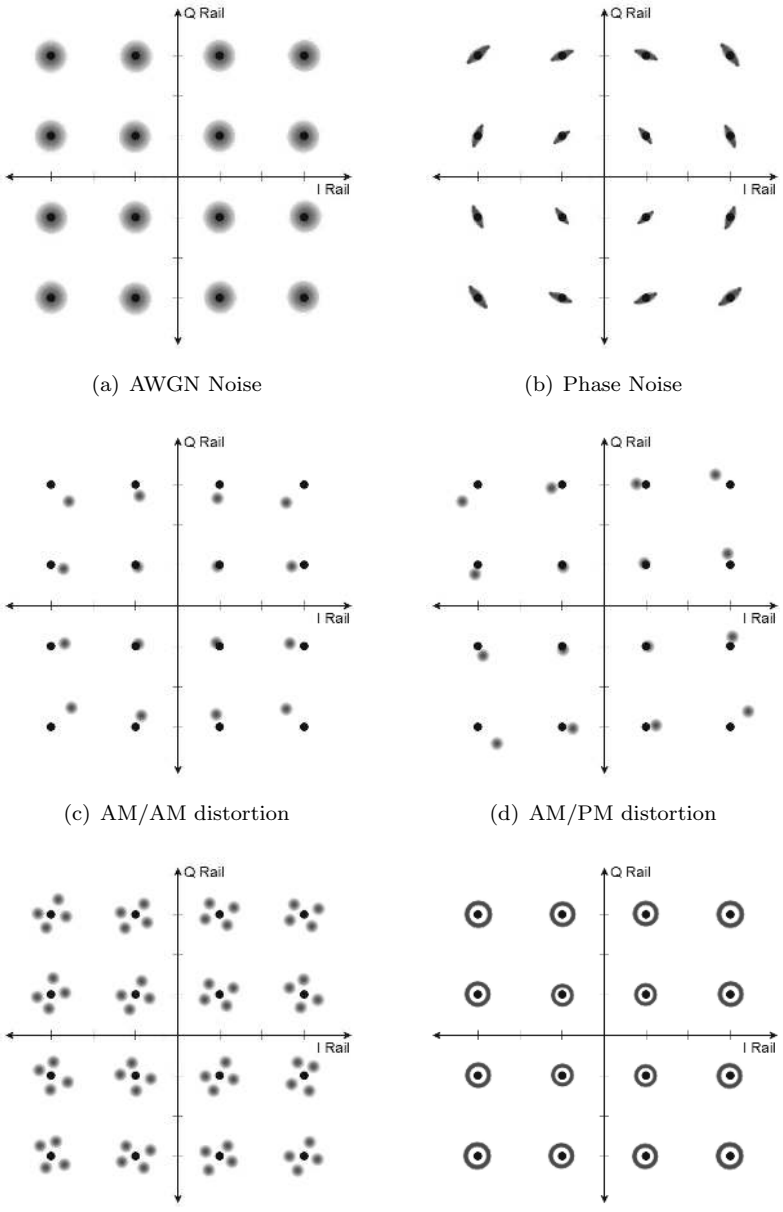
When enough symbols are simulated more information can be extracted from the distorted constellation points, because the points will form a cloud. These clouds can indicate what kind of distortion is present in the system [23].

The required length of the simulation depends mainly on the type of distortion present and the impulse response of the system. For distortion sources that move the constellation points, but that are not depending on previous symbols, i.e. the system is memory less, the minimum length of the simulation required is only M symbols long, where $\log_2 M$ is the number of bits in each symbol. More in general the required minimum number of symbols transmitted in the simulation is given by M^L, where the impulse response of the system is L symbols long [21]. However, for many systems the impulse response is infinite; in that case the results must be approximated by selecting a finite L.

When in the channel between the transmitter and receiver only Additive White Gaussian Noise (AWGN) is added, the constellation points will look like the random noise points in Fig. 2.12a, which has the effect of creating a distribution of sample points around the ideal constellation point. Other sources of noise and distortion will create other distributions of sample points in the received constellation diagram. For example, phase noise is similar to random noise but the constellation points fall only on the angular axis, see Fig. 2.12b. AM/AM distortion often originates from by the power amplifier causing the signal point to move on the radial axis based on the vector length, see Fig. 2.12c, and AM/PM distortion causes the symbol point to have an angular error based on the vector length, see Fig. 2.12d. When ISI is present, because of previous symbols distorting the received symbol, the constellation diagram will have distinct sample points around the ideal sample points, see Fig. 2.12e. Interference with a fixed frequency in the band will cause the sample points to take on a circular shape around the ideal points, see Fig. 2.12f. More types of distortion do exist, but these are the most common types of distortion that can be present at the receiver.

In reality the distortion sources that are present in the system are not only of one type, but a combination of them.

This semi-analytical method has more constraints than the Monte-Carlo method



(a) AWGN Noise

(b) Phase Noise

(c) AM/AM distortion

(d) AM/PM distortion

(e) Inter Symbol Interference (simplified)

(f) Interference with fixed in-band frequency

Figure 2.12: Constellation diagrams for different sources of noise/distortion.

described before. In order to be able to use this approach, several conditions must be fulfilled.

- In the communication system, noise sources should not be followed by components that have non-linearity.
- Other noise sources, such as phase noise are neglectable.

Non-linearities in the communication system can displace the constellation points. The location of the displaced constellation points depend on the original location and on the non-linearity. Since the noise is added a posteriori analytically to the distorted constellation points, it can not take into account the effect the non-linearity has on the noise. Therefore, the assumption that the added noise in the channel is received by the receiver as AWGN is only valid in case the system is linear from the point where the noise is added. If non-linearities in the receiver are being analyzed this condition is not longer fulfilled and the result becomes unreliable. Non-linearities in the transmitter, however, can be analyzed correctly, because it is commonly assumed that the dominant noise is originating from the channel and not from within the transmitter. Therefore this method is more suitable for analyzing the transmitter than the receiver.

The second condition implies that the transmitter and receiver are perfectly locked on each other and that slow varying processes, such as phase noise caused by the timing recovery loop of the receiver, are not taken into account.

2.3 Multi-carrier QAM transceiver

In multi-carrier QAM more data streams are put together. The data is combined according to the Frequency Division Multiplexing (FDM) principle. The different channels are modulated at different frequencies. The transmitter for a multi-carrier system is shown in figure 2.13. The transmitter has many similarities with the single carrier transmitter given in figure 2.4. The most important difference is that, instead of one I and one Q signal, more I and Q signals

are added. Each of these signals are modulated at different frequencies and summed. The data is then mixed up as in the case of the single carrier QAM transmitter.

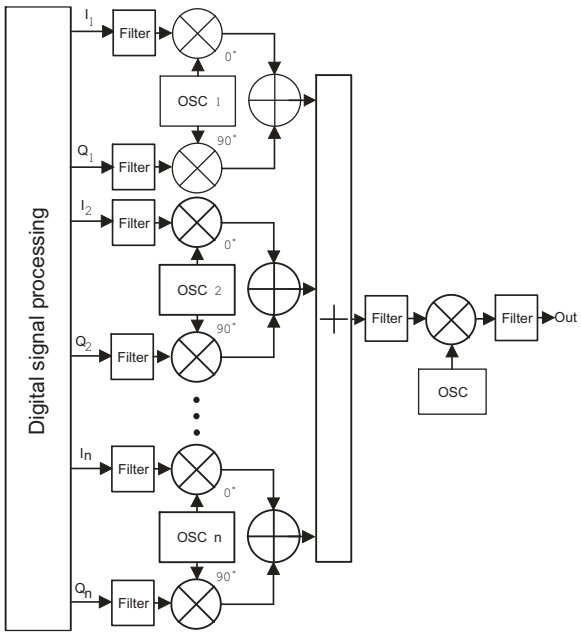


Figure 2.13: Symbolic representation of a transmitter for a multi-carrier system

The carriers can be added in two different ways, non-orthogonal or orthogonal. The first method is usually called Frequency Division Multiplexing (FDM), the second method is called Orthogonal Frequency Division Multiplexing (OFDM).

Systems which transmit data over different carriers, such as FDM, require that the individual carriers do have a sufficient guard band in order to prevent interference between signals from adjacent carriers. However, when the individual carriers are allowed to overlap, the available bandwidth can be used more efficiently. The data from these overlapping carriers can be correctly recovered by using coherent detection and orthogonal carriers. This method is used in OFDM which was introduced by Chang [24]. Using OFDM simplifies the analog design at the cost of more digital signal processing of the transmitter and receiver: because of the orthogonality, a separate transmit and receive filter for

each carrier is not required.

In the OFDM scheme the data to be transmitted is split into N parallel carriers. Each of those channels is modulated at carrier frequencies, $f_0, f_1, \ldots, f_{N-1}$. The bandwidth of the signal is $N\Delta f$, where Δf is the difference between the frequencies of the adjacent carriers.

The main advantage of OFDM, with many narrow-band carriers, compared to a single carrier transmitting the same information, is its ability to cope with severe channel conditions, such as frequency selective attenuation, fading due to multi-path and narrow-band interference. For the OFDM scheme, channel equalization is simpler because the symbol rate for each individual narrow-band carrier is much lower than for the wide band single carrier scheme.

Despite its elegance, until recently its use was limited to military applications due to its implementation difficulties of the real-time digital signal processing. Recently OFDM is used in many commercial systems, such as Digital Audio Broadcasting (DAB), Digital Video Broadcasting - Terrestrial (DVB-T), WiFi (IEEE 802.11b/g), WiMax (802.16e) and Discrete Multi-tone (DMT) in Asymmetric Digital Subscriber Line (ADSL).

However, the orthogonal addition of the individual carriers requires a full-spectrum transmitter: in case of multiple transmitters, synchronization between the transmitters to keep the individual carriers orthogonal becomes difficult. In systems, such as DOCSIS [3], where different carriers from different sources are added together, the OFDM scheme is not used. In addition, the channel (hybrid coaxial, see Chapter 3.1) between the transmitter and receiver is well behaving, which reduces the need for channel compensation techniques, such as for example water pouring techniques (channels with better SNR will use higher order modulation to carry more data than channels with worse SNR) in ADSL where the channel has a strong frequency dependency. In this thesis we will not further focus on OFDM.

2.4 Signal properties of multi-carrier QAM

In a Multi-Carrier Communication system multiple carriers are combined into one signal. Each of these carriers has a certain Crest factor. When more of these carriers are added the Crest factor of the resulting signal increases. This larger Crest factor makes it more difficult to convert the signal in a DAC, because of the large dynamic range needed to prevent clipping. The dynamic range needed to prevent excessive clipping will be discussed in Chapter 2.4.2. However, the chance that this high peak occurs, reduces.

Peak to Average Power Ratio

Instead of quantifying the envelope variations of a signal with the Crest factor, the PAPR (Peak to Average Power Ratio) is often used. The PAPR for a signal $S(t)$ is defined as

$$PAPR = \lim_{T\to\infty} \frac{max|S(t)|^2}{\frac{1}{T}\int_0^T S(t)^2 dt}, \tag{2.11}$$

where T is the duration of the time for which the PAPR is observed. Since the peak event of the signal could be a rare event the signal should be observed infinite, however, in practice the observation time of the signal always is limited.

The PAPR has a direct relation with the earlier mentioned parameter called Crest factor. The PAPR is defined as a power ratio whereas the Crest factor is defined for the corresponding amplitude ratio; therefore

$$CF = \sqrt{PAPR}, \tag{2.12}$$

2.4.1 Multi-carrier versus single sinewave signals

For the characterization of the quality of a DAC sinusoidal signals are typically used. These sinusoidal signals have specific properties that are unlike the properties in multi-carrier signals. In Fig. 2.14a a sinusoidal function is plotted as a function of time. In Fig. 2.14b the amplitude histogram of this function is

shown. This histogram shows that the signal is a longer amount of time near the upper or lower extreme amplitude, than it is in between.

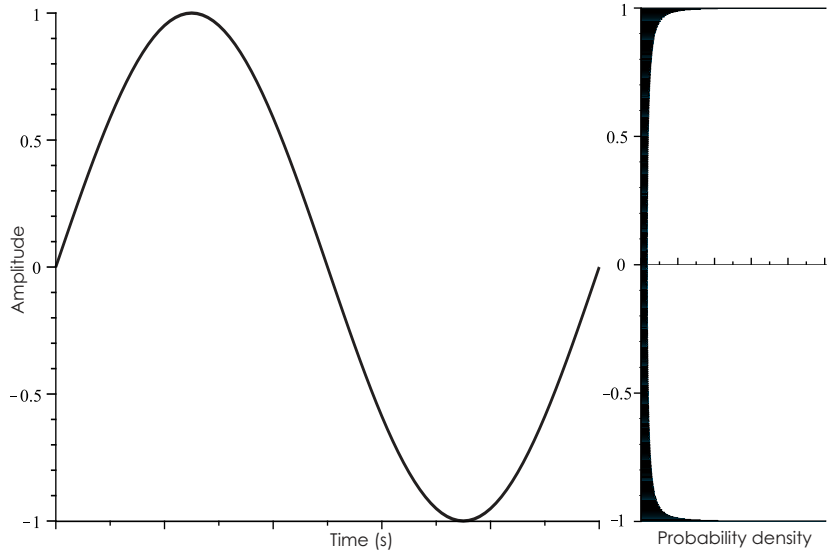


Figure 2.14: a. Sinusoidal signal plotted as a function of time. b. Histogram of the sinusoidal function.

As will be proven in Chapter 2.4.5 a multi-carrier signal can be approximated by a Gaussian signal. In Fig. 2.15 a small snapshot of a Gaussian signal is shown. The amplitude histogram is shown in the second part of the figure. This shows that the amplitude value, opposite to sinusoidal signals, is most likely to be around the center (zero).

2.4.2 Signal clipping

In a multi-carrier system many carriers are added. The sum of these carriers have a large Crest factor, as explained in Chapter 2.4. Therefore, the instantaneous amplitude level of a multi-carrier QAM signal can have a large value. In figure 2.16, an example of the amplitude of a multi-carrier signal is shown. The two horizontal dashed lines denote the clipping levels. When the signal rises above the upper clipping level or below the lower clipping level, the signal

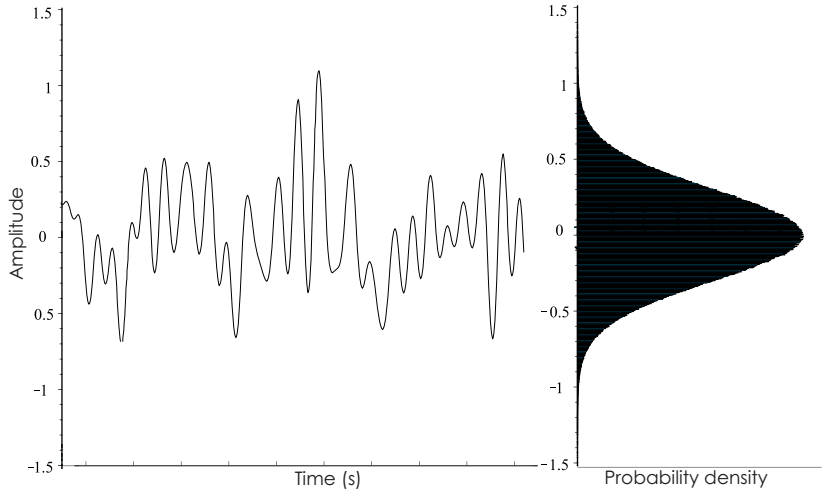


Figure 2.15: a. *Gaussian signal plotted as a function of time.* b. *Histogram of the Gaussian function.*

will be clipped to this level. This clipping introduces additional distortion to the signal.

Clipping can be prevented by making the dynamic range of the DAC and of the amplifiers large enough. When the clipping level is set at the rms signal level nearly all transmitted symbols are clipped; to reduce the chance of clipping, the clipping level has to be increased to a value larger than the rms level of the multi-carrier signal. The ratio of the saturating power level to the average power level is called back-off. The required dynamic range to transmit the signal unclipped can be calculated and depends on the number of carriers used. The required dynamic range increases proportionally to the square root of the number of carriers [25]. The required back-off, apart from the back-off requirements of a single carrier, when no clipping is allowed is given as

$$Back\ off = 10log_{10}(N)\,[dB], \tag{2.13}$$

where N is the number of carriers in the signal [26].

The probability that this peak level occurs is small. Designing the analog

components for this limit can also be difficult because of the constrains for the dynamic range. In addition, designing the dynamic range of the system for this level such that no clipping occurs, does not result in an optimal solution, because of the quantization noise, which is proportional to the dynamic range of the DAC. There is thus a trade off between a high clipping level with larger quantization noise and a low clipping level with lower quantization noise.

When some level of clipping is permitted the system can be optimized for the smallest Bit Error Rate (BER), as will be shown in Chapter 2.4.4.

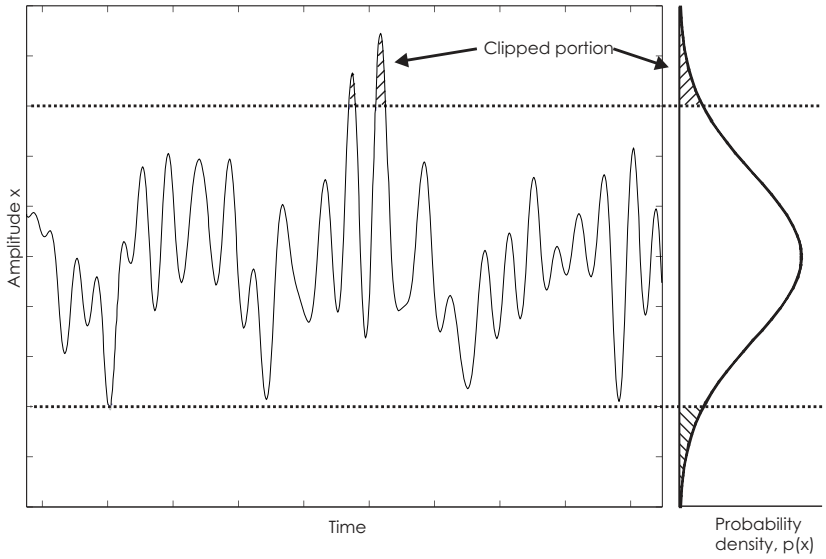


Figure 2.16: Clipping of the signal

For a large number of transmitted carriers that are combined orthogonally and non-orthogonally, Fig. 2.17 shows the probability that the signal amplitude is above a certain clip level. In this figure the vertical lines denote the amount of back-off in dB above the rms level of the signal. The probability density function of the amplitude level for the orthogonally combined signal can be approximated by the complementary cumulative Rayleigh distribution [7]. For the non-orthogonal combined signal the probability of clipping can be approximated by the erf function [25]. For systems with low BER requirements the typical clipping probability is bellow 10^{-5}. In that case, the orthogonally

combined signal drops faster for higher values of the back-off, as shown in the figure. This reduces the dynamic range that is required, compared to the non-orthogonal combined signal.

The clipping has effect on the spectrum of the transmitted signal. Because of clipping, the out-of-band emission increases, possibly also affecting other carriers and systems. In some applications these out-of-band emissions are not tolerated. To prevent, when needed, these out-of-band emissions, a filter has to be applied at the output of the transmitter. The filtering itself also has a negative impact on the signal. The filter has to be made as an analog filter, because the clipping occurs in the DAC or in the amplifier. Analog filters usually do not have a linear phase and constant amplitude level in the pass-band. A QAM signal is a broadband signal. Broadband signals are sensitive to non-constant group delays and to non-constant amplitude characteristics of the channel. The analog filter can therefore distort the QAM signal if the characteristics of this filter are not according to the required characteristics set by the broadband signal. In addition, the analog filter increases the complexity of the system.

2.4.3 Preventing clipping

There are several solutions published to reduce the required dynamic range of the multi-carrier system by changing the transmitted symbols. Two main types of peak-to-mean power ratio reduction techniques are used in the literature, which rely either on introducing redundancy in the data stream or on post processing the time domain signal before transmitting it.

In the first method, where the data has redundancy, more than one amplitude level can be chosen to transmit a certain symbol. The advantage of this approach is that the Crest factor is reduced because the symbols of the carriers are chosen so that the power level of the combined signal is as constant as possible.

The second method reserves one or more carriers in which no information is sent, except for symbols that are chosen such that the amplitude and phase are

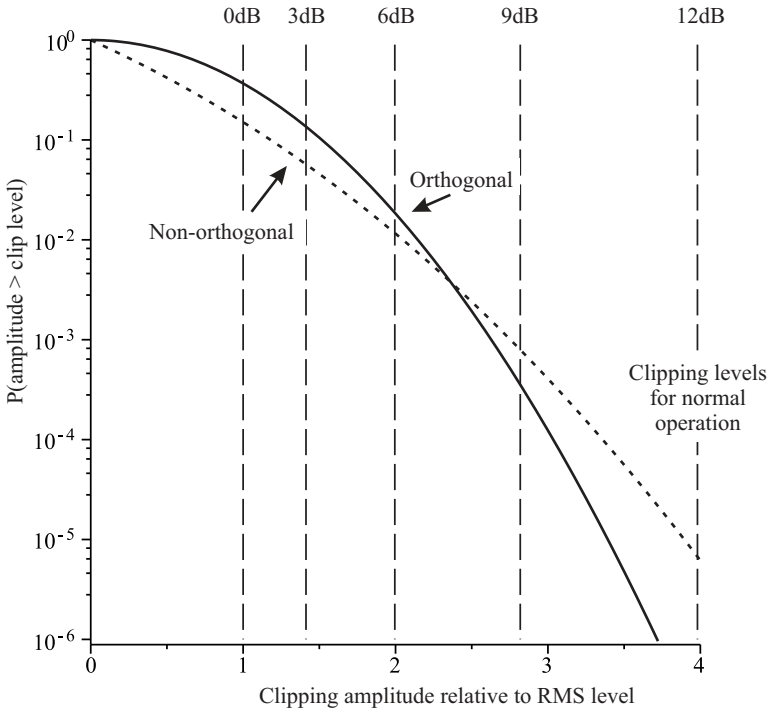


Figure 2.17: The chance that the signal is clipped for orthogonal and non-orthogonal combined signals as a function of the relative clipping amplitude for a large number of carriers.

counter acting to the amplitude of the combined signal containing the carriers.

Other methods do exist that have their own advantages and disadvantage. However, a common disadvantage of most of these solutions is a lower spectral efficiency, because of the additional redundancy in the data stream. In the DOCSIS system described here none of these peak reduction methods are used and they will therefore not be analyzed in more detail in this thesis.

2.4.4 Optimum clip level

The optimum number of bits for the digital-to-analog converter is mainly determined by two phenomena. The first one is the clipping. When clipping is

applied it introduces additional distortion to the signal. The amount of distortion generated by the clipping is inversely related to the level of the clipping: when the clipping level decreases, the amount of clipping distortion increases. The second effect is the quantization noise. The number of bits and the dynamic range of the DAC determine the quantization noise. When the dynamic range increases, the quantization noise will also increase, assuming that the number of bits is constant. The dynamic range of the DAC is given by the clip level that is used. Between both extremes (a small clipping probability but much quantization noise, or little quantization noise but a large clipping probability) an optimum exists.

To find the optimum for non-orthogonally modulated carriers, a number of assumptions are made. The first assumption is that the Gaussian approximation is valid; that means: enough carriers are used. When this assumption does not hold, the solution found here will not be the optimal solution because a too large dynamic range will be predicted by using the Gaussian distribution. This results in a larger quantization noise than needed.

The second assumption is that the quantization noise is determined by the number of bits used and no additional noise sources are present in the DAC. This assumption will not hold in a real DAC, because also other elements affect the signal-to-noise and distortion ratio (SNDR), such as the thermal and 1/f-noise, non-linearities, mismatch and timing problems of the DAC. With respect to the required number of bits the analysis will be too optimistic. All these error sources will affect the SNDR of the DAC, and determine the number of bits needed to achieve this SNDR. In the design of the DAC these additional effects need to be taken into account. In the succeeding chapters the effect of some of the additional error sources that affect the SNDR, such as non-linearities, mismatch, and timing problems are taken into account.

Although the tails of the Gaussian distribution reach up to infinity, the chance that such a peak occurs is also almost zero. Therefore, the system does not have to be designed to be able to reach those extreme values. In systems where many carriers are added, some clipping is usually tolerated to relax the requirements of the components. The chance that the clipping occurs and its

effect on the BER are analyzed in the next section.

Clipping distortion

Clipping introduces additional distortion, and harmonic components to the signal. As mentioned in the previous sections, the signal, that is converted by the DAC, can be modeled by a Gaussian distribution, with the previously mentioned remarks about this assumption.

Since the maximum instantaneous amplitude, A_{max}, has a low probability of occurrence, it can be advantageous to accept some level of clipping to limit the required dynamic range.

The Gaussian random process to model the signal converted in the DAC is given by

$$p(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{\left(-\frac{x^2}{2\sigma^2}\right)}, \tag{2.14}$$

where $p(x)$ is the probability density function that the signal $A(t)$ takes the value x. The pdf has a zero mean and a variance of σ^2, which is equal to the power of the signal, P_{tot}. When the maximum absolute amplitude of the signal is limited to A_{clip}, the total power of the clipped portion is given by [26]:

$$P_{clip} = \int_{A_{clip}}^{\infty} (x - A_{clip})^2 \, p(x) dx \tag{2.15}$$

$$= \frac{2}{\sqrt{2\pi\sigma^2}} \int_{A_{clip}}^{\infty} (x - A_{clip})^2 \, e^{-\frac{x^2}{2\sigma^2}} dx \tag{2.16}$$

To simplify the equations, the total power of the signal $P_{tot} = \sigma^2$ will be normalized to unity, without loss of generality. Equation 2.15 can be split into three parts:

$$\begin{aligned} P_{clip} &= \frac{2A_{clip}^2}{\sqrt{2\pi}} \int_{A_{clip}}^{\infty} e^{-\frac{x^2}{2}} dx - \frac{4A_{clip}}{\sqrt{2\pi}} \int_{A_{clip}}^{\infty} x e^{-\frac{x^2}{2}} dx + \frac{2}{\sqrt{2\pi}} \int_{A_{clip}}^{\infty} x^2 e^{-\frac{x^2}{2}} dx \\ &= I_1 - I_2 + I_3 \end{aligned} \tag{2.17}$$

where A_{clip} is the clip level. The three parts can be written as follows

$$I_1 = \sqrt{\frac{2}{\pi}} A_{clip}^2 \int_{A_{clip}}^{\infty} e^{-\frac{x^2}{2}} dx = A_{clip}^2 erfc\left(\frac{A_{clip}}{\sqrt{2}}\right) \tag{2.18}$$

and

$$I_2 = 2\sqrt{\frac{2}{\pi}} A_{clip} \int_{A_{clip}}^{\infty} x e^{-\frac{x^2}{2}} dx = 2\sqrt{\frac{2}{\pi}} A_{clip} e^{\left(-\frac{A_{clip}^2}{2}\right)} \tag{2.19}$$

and

$$I_3 = \sqrt{\frac{2}{\pi}} \int_{A_{clip}}^{\infty} x^2 e^{-\frac{x^2}{2}} dx = \sqrt{\frac{2}{\pi}} A_{clip} e^{-\frac{A_{clip}^2}{2}} + erfc\left(\frac{A_{clip}}{\sqrt{2}}\right) \tag{2.20}$$

From equation 2.17 - 2.20, we have

$$P_{clip} = \left(A_{clip}^2 + 1\right) erfc\left(\frac{A_{clip}}{\sqrt{2}}\right) - \frac{\sqrt{2} A_{clip} e^{-\frac{A_{clip}^2}{2}}}{\sqrt{\pi}} \tag{2.21}$$

Quantization noise

For the quantizer we assume that it is a uniform quantizer with an output range from $-A_{clip}$ to A_{clip}. The step size related with the maximum output level and number of bits by

$$A_{clip} = \Delta \cdot 2^{b-1} \tag{2.22}$$

where Δ is the LSB step size and b is the number of bits. For the quantization uniformly distributed granular noise is assumed. The quantization noise power is then given by

$$P_{quantization} = \frac{A_{clip}^2}{3(2^b)^2}, \tag{2.23}$$

The quantization noise increases when A_{clip} is increased.

Clipping and quantization noise

The total noise power at the output of the quantizer is the sum of the quantization noise and the clipping noise. Although the clipping noise has a different origin then quantization noise, these distortion sources can be added in the case that there is no excessive clipping. In the case the clipping occurs infrequently, the clipped portions of the signal are shaped as glitches and have high frequency content. In combination with the Nyquist folding the distortion can be assumed to be uniform in the frequency band of interest. However, when the clipping becomes excessive this assumption does not longer hold and the spectral content of the clipped signal becomes harmonic like, and no longer uniform. In this thesis we assume that the clipping occurs only rarely and that the pdf of the clipping noise be assumed to be uniform [27], and is thus given by

$$\begin{aligned} P_{total} &= P_{clip} + P_{quantization} && (2.24) \\ &= \left(A_{clip}^2 + 1\right) erfc\left(\frac{A_{clip}}{\sqrt{2}}\right) - \frac{\sqrt{2}A_{clip}e^{-\frac{A_{clip}^2}{2}}}{\sqrt{\pi}} + \frac{A_{clip}^2}{3(2^b)^2} && (2.25) \end{aligned}$$

This function is differentiated with respect to A_{clip} and setting the result to zero in order to determine the optimum clipping level, we obtain

$$A_1(2^b)^2 + A_2(2^b) + A_3 = 0 \tag{2.26}$$

where the A_i's are given by

$$A_1 = 4A_{clip}Q\left(A_{clip}\right) - \sqrt{\frac{8}{\pi}}\exp\left(-\frac{A_{clip}^2}{2}\right) \quad (2.27)$$

$$A_2 = \sqrt{\frac{8}{\pi}}\exp\left(-\frac{A_{clip}^2}{2}\right) - 8A_{clip}Q\left(A_{clip}\right) \quad (2.28)$$

$$A_3 = \frac{2}{3}A_{clip} + 4Q\left(A_{clip}\right) - \sqrt{\frac{2}{\pi}}A_{clip}^2\exp\left(-\frac{A_{clip}^2}{2}\right) \quad (2.29)$$

where $Q(x) \triangleq \int_x^\infty \frac{1}{\sqrt{2\pi}}e^{-\frac{u^2}{2}}du = \frac{1}{2}erfc\left(\frac{x}{\sqrt{2}}\right)$.

In figure 2.18 the sum of the quantization distortion and clipping distortion is plotted with respect to the normalized dynamic range for DAC. The figure shows where the optimum level of clipping for the given DAC resolution can be found.

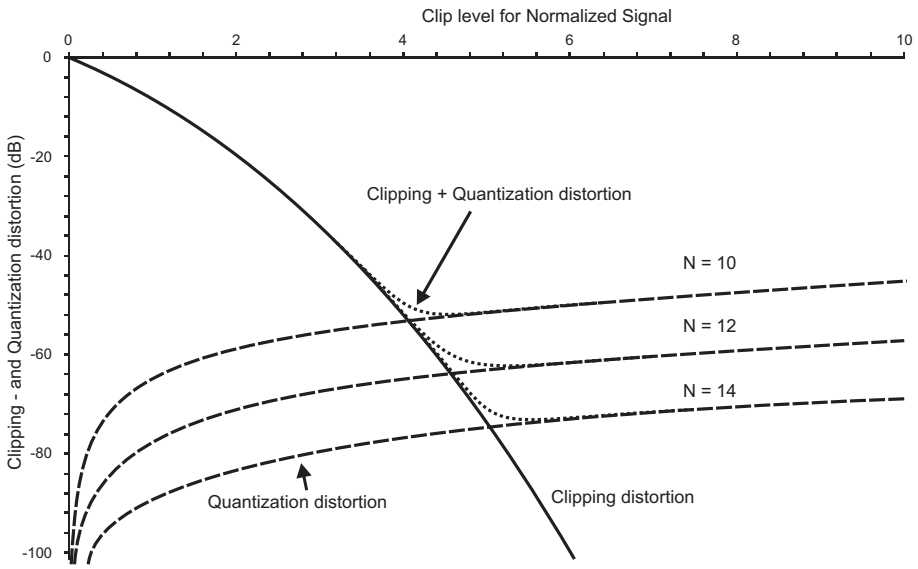


Figure 2.18: Quantization and Clipping Distortion for the Clipping level

2.4.5 Optimum clip level with low number of carriers

To find the optimum in the previous section, the assumption was made that the Gaussian approximation is valid, which means enough carriers were used.

In this section we will show that for a lower number of carriers, using the Gaussian approximation results in a system that has a clipping level larger than the optimal system has. This can result in a too complex system, needed for the signal to be sent with a given maximum BER. The BER can even increase because this too large dynamic range results in more quantization noise.

Approximating the Gaussian distribution

The Central Limit Theorem says that an appropriately normalized (the total power stays constant) sum of independent, identically-distributed random values has a distribution that approaches a Gaussian distribution in the limit of a large number of terms [28]. In this section the effect of the finite number of channels is on how close the distribution is to the Gaussian distribution investigated.

Consider adding N independent channels, as we do in the Multi-Carrier QAM communication. The carriers can be assumed independent, because a scrambler is used for the data in the modulation of each carrier as will be explained in Chapter 3.1. The task of this scrambler is to randomize the data of each carrier, even in the case that the data of each carrier is identical. The resulting signal is the sum of N independent carriers,

$$x_c = \sum_{k=0}^{N-1} X_{uc}[k], \tag{2.30}$$

where $X_{uc}[k]$ is the k'th channel and x_c is the resulting broadband signal. To simplify the calculations it is assumed that the probability density function of the amplitude for each carrier is uniform. For a single carrier with QAM mod-

ulation and limited filtering the amplitude distribution resembles this uniform distribution accurately.

Assuming that all channels have the same statistical properties, the probability density function of the sum can be obtained by convolving the N density functions

$$\begin{aligned} p_c(x,N) &= p_{uc_{[0]}}(x) \otimes \cdots \otimes p_{uc_{[N-1]}}(x) \\ &= p_{uc}(x) \otimes \cdots \otimes p_{uc}(x), \end{aligned} \tag{2.31}$$

where $p_{uc}(x)$ is the probability density function of X_{uc}. The convolution in the time domain is equivalent to the multiplication in the frequency domain. The Laplace transform of the probability density of the sum can be expressed as the N-fold product of the Laplace transform of the uniform density.

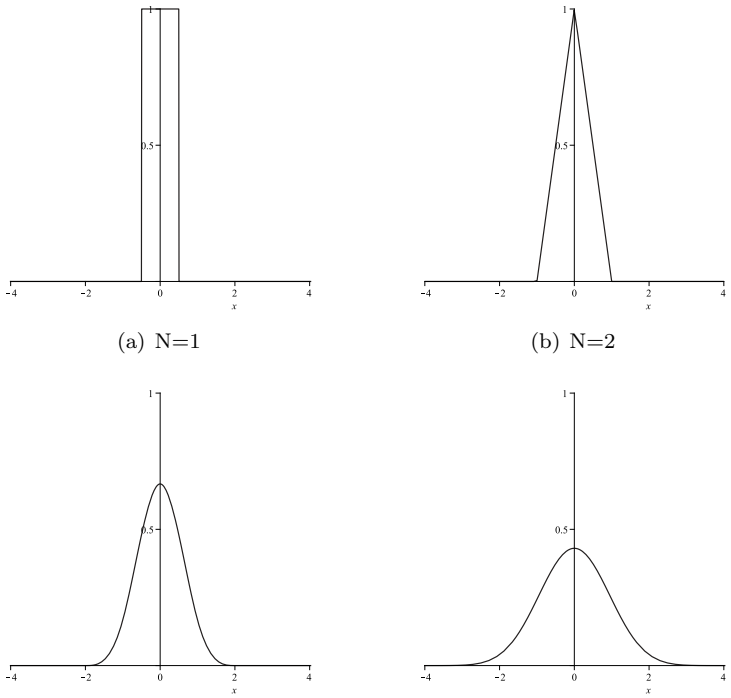
The uniform pdf can be written as the difference between two unit step functions,

$$p_{uc}(x) = u(x) - u(x-1), \tag{2.32}$$

where the unit step function, $u(x)$, see Fig. 2.19a, is defined as

$$u(x) = \begin{cases} 1, & x \geq 0; \\ 0, & \text{elsewhere.} \end{cases} \tag{2.33}$$

The Laplace transform of $p_c(x,N)$ is



(a) N=1 (b) N=2

(c) N=4 (d) N=10

Figure 2.19: N-fold Convolution of uniform distributions

$$\mathcal{L}[p_c(s,N)] = \left(\frac{1-e^{-s}}{s}\right)^N \tag{2.34}$$

$$= \frac{1}{s^N}\sum_{k=0}^{N}(-1)^k \left(\begin{array}{c} N \\ k \end{array} \right) e^{-ks} \tag{2.35}$$

$$\tag{2.36}$$

The inverse Laplace transform of this expression gives the pdf of the sum [29]

$$p_c(x,N) = \frac{1}{(N-1)!}\sum_{k=0}^{N}(-1)^k \left(\begin{array}{c} N \\ k \end{array} \right)(x-k)^{N-1}u(x-k). \tag{2.37}$$

The pdf is formed from polynomial segments. The function value $p_c(x, N)$ is only non-zero for $0 \leq x \leq N$ and is symmetric around $N/2$. The cumulative distribution function (cdf) can be calculated by integrating the pdf:

$$F_c(x, N) = \frac{1}{N!} \sum_{k=0}^{N} (-1)^k \left(\begin{array}{c} N \\ k \end{array} \right) (x-k)^N u(x-k). \tag{2.38}$$

The distribution of the sum has mean $m_c = N/2$ and variance $\sigma_c^2 = N/12$. A zero-mean, unit-variance variate can be created by scaling and shifting the sum,

$$x_{nc} = \sigma_c(x_c - m_c). \tag{2.39}$$

The resultant pdf and cdf are

$$p_{nc}(x, N) = \sigma_c p_c(\frac{x}{\sigma_c} + m_c, N), \tag{2.40}$$

$$F_{nc}(x, N) = F_c(\frac{x}{\sigma_c} + m_c, N). \tag{2.41}$$

For $N = 1, 2, 4$ and 10, respectively, the resulting pdf is shown in Fig. 2.19

The Berry-Essen Theorem [28] gives information about the rate of convergence of the distribution to a Gaussian distribution as the number of carriers, N, increases. The cdf of the normalized sum of distributions can be bounded relatively to the true Gaussian cdf [29] as

$$|F_{nc}(x, N) - N(0, 1)| < \frac{9}{4\sqrt{N}}, \tag{2.42}$$

where $N(0, 1)$ is the normalized Gaussian distribution. This shows that the difference, between the true Gaussian distribution and the pdf of the sum, decreases as $1/\sqrt{N}$ with increasing N. This equation gives an upper bound, for practical values of N, the actual deviation is smaller [29].

Figure 2.20 shows a plot of the pdf $p_{nc}(x, N)$ for $N = 12$, and a true Gaussian pdf. The tails of $p_{nc}(x, N)$ extend from the mean out to $\pm\sqrt{3N}$ and are zero beyond that point. For the given figure, the tails extend out to ± 6 standard deviations.

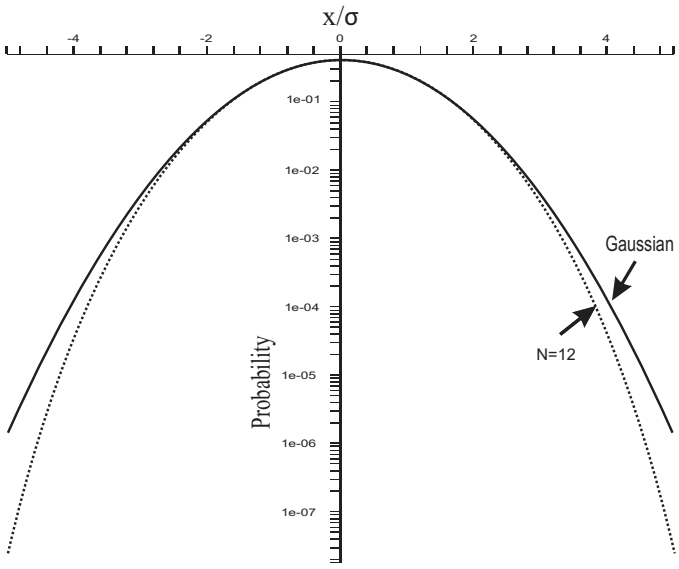


Figure 2.20: Probability density function for a sum of N = 12 carriers

The $p_{nc}(x, N)$ oscillates around the pdf of the true Gaussian density. The difference between the true Gaussian density and the pdf of the sum for different values of N is plotted in figure 2.21. As can be seen the tails of the Gaussian density functions do not fall as fast as for the approximated function that becomes zero beyond a certain point.

Models that use the Gaussian pdf actually assume there is an infinite number of carriers. In the previous section we discussed what changes if the number of carriers is not large enough to be modeled by a Gaussian distribution.

The most important change in pdf, for the amplitude of the sum of carriers, is that the tails of the pdf are shorter than in the case of the Gaussian distribution. In the case of a Gaussian distribution the tails reach to $\pm\infty$, but for a finite number of carriers the highest peak that can occur is limited and not infinite as predicted by the Gaussian model. For any finite number of carriers the

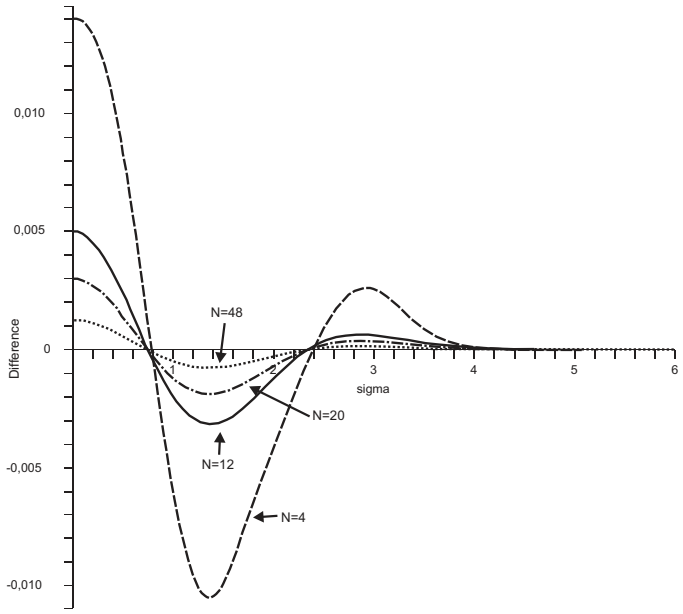


Figure 2.21: Difference between the Gaussian power density function and the pdf of the sum of N uniform carriers

Gaussian distribution is not usable for estimating the tails. In reality, any realizable signal will have a limited number of carriers.

Signal clipping with low number of carriers

In a multi-carrier system many carriers are added. The sum of these carriers have a large Crest factor, as explained in Chapter 2.4. Therefore, the instantaneous amplitude level of a multi-carrier QAM signal can have a large value. When the number of carriers is low, clipping can be prevented by making the dynamic range large enough. However, preventing the clipping of the signal will only be optimal for a system with a few carriers as we will show in this section. This is, because the chance that the signal reaches those peak values increases with a lower number of carriers and the required dynamic range is small. When the number of carriers increases, the level of the peaks increases, but the chance of the signal reaching those peak values decreases.

Combined signals Consider adding N independent channels. Each carrier is a QAM modulated signal, where the I and Q component are orthogonal and are assumed to be independent and uniformly distributed. This last assumption holds when the bandwidth parameter of the Nyquist filter is not too low [30]. If this assumption does not hold, this analysis will be somewhat optimistic for a low number of carriers.

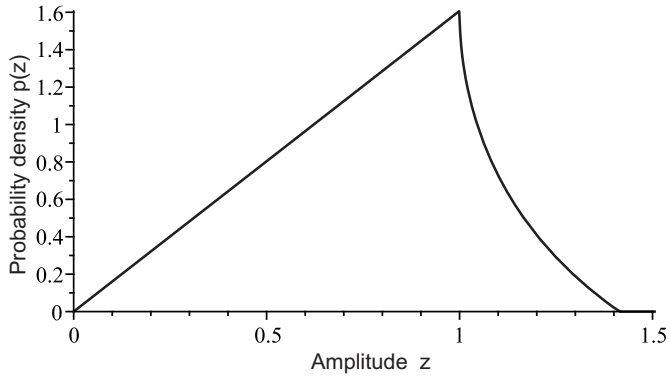


Figure 2.22: Probability Density Function of the amplitude of a non-orthogonal QAM signal, with the maximum I and Q amplitudes normalized to one

The pdf of the amplitude of a single QAM signal in which the I and Q components are orthogonal and the maximum I and Q amplitudes are normalized to one is given in Fig. 2.22. First the pdf of a single carrier is Fourier transformed to the frequency domain. The resulting signal is raised to the N-th power and transformed back with the inverse Fourier transformation,

$$\begin{aligned} p_c(x,N) &= p_{uc_{[0]}}(x) \otimes \cdots \otimes p_{uc_{[N-1]}}(x) \\ &= p_{uc}(x) \otimes \cdots \otimes p_{uc}(x) \qquad (2.43) \\ &= \mathfrak{F}^{-1}\left(\left(\mathfrak{F}\left(p_{uc}(x) \right) \right)^N \right). \qquad (2.44) \end{aligned}$$

The energy of the resulting signal that is clipped, because it is above the clip-level, is summed and is shown in Fig. 2.23, where the complementary cumulative density function (ccdf) function is plotted for $N = 4..16$ and for $N = \infty$.

The case of $N = \infty$ is equal to the result shown in Fig. 2.17. This figure also shows the quantization distortion corresponding to the clip levels for b=10..14 bit.

Notice the small difference between the case of $N = 16$ and $N = \infty$. For the practical realizable levels of quantization this difference can be neglected. Therefore, in the case of 16 or more carriers the much simpler to calculate Gaussian approximation can be used without an over dimensioned system as a result.

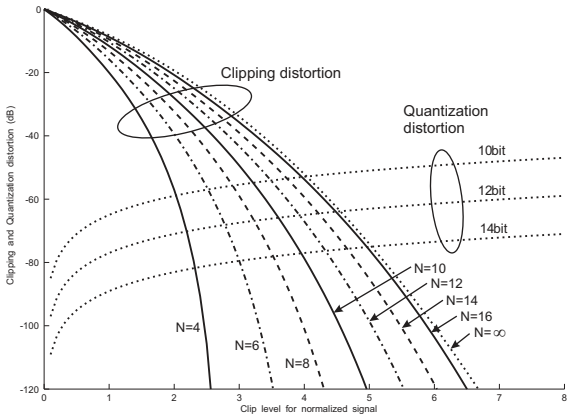


Figure 2.23: Clipping and Quantization distortion as a function of the normalized clipping level

The smallest overall distortion level is close to the crossing point of the clipping distortion and the quantization noise. This optimum clip level is shown in Fig. 2.24, where the lowest overall distortion and its corresponding clipping level is plotted as a function of the number of carriers for several resolutions of the dynamic range.

Fig. 2.25 shows the overall distortion level as a function of the number of carriers when the clipping level is chosen optimally. As expected, when we increase the number of carriers and want to keep the distortion level constant we have to increase the number of bits for the quantization. The total distortion increases fast when adding more carriers in the case of a few carriers, but levels

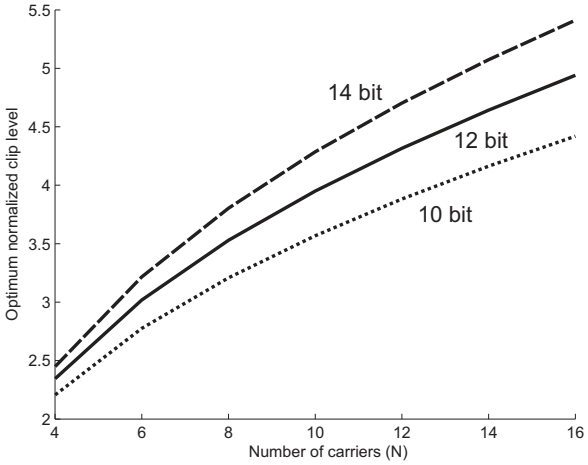


Figure 2.24: The optimal clipping level as a function of the number of carriers

off when the number of carriers is increased further.

Orthogonally combined signals Consider the special case of adding N independent uniform channels orthogonally. In communication standards, such as Orthogonal Frequency Division Multiplexing (OFDM), this orthogonal addition of sub carriers is used. The carriers can be assumed independent as explained before.

$$x_c = \sum_{k=0}^{N-1} X_{uc}[k], \tag{2.45}$$

QAM modulation is the combination of two orthogonal PAM modulated signals. The amplitude of the vector is given by

$$Z = \sqrt{I^2 + Q^2}, \tag{2.46}$$

Let's assume that the I and Q component are independent, which is generally a valid assumption for QAM modulation. The probability density function (pdf)

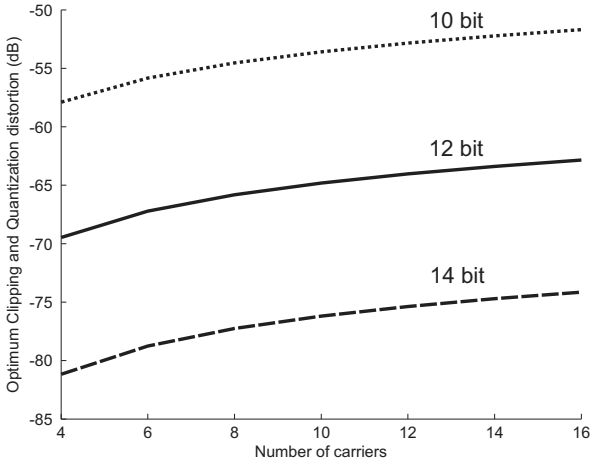


Figure 2.25: The distortion level with an optimal clipping level as a function of the number of carriers

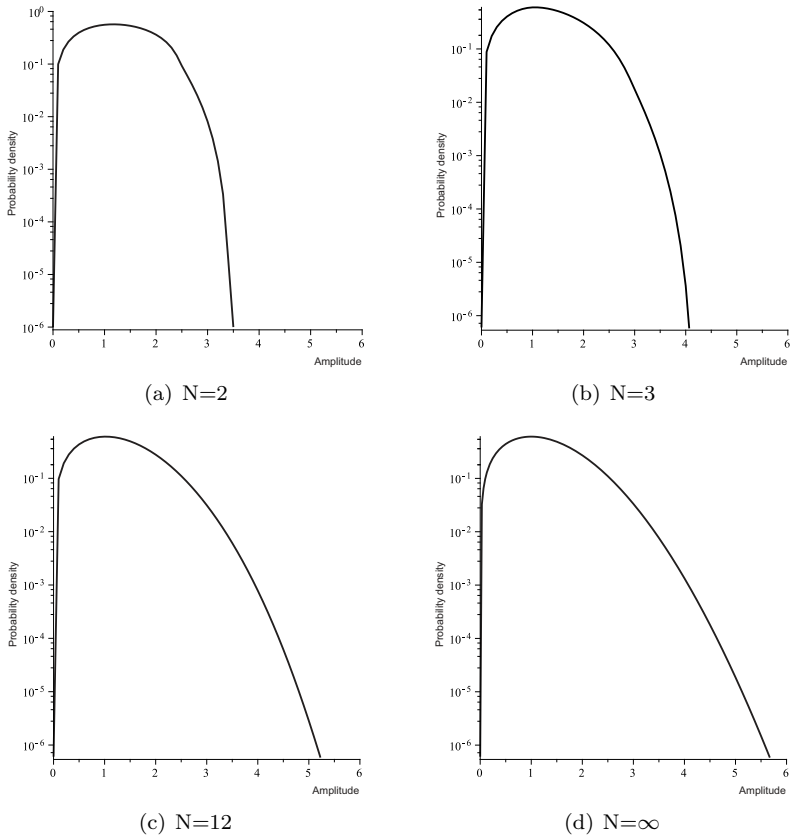
of the vector amplitude is given by [28] for Orthogonal Frequency Division Multiplexing as

$$f_Z(z) = \int_0^z 4 \frac{z p_{IQ}\left(\sqrt{z^2 - x^2}\right) p_{IQ}(x)}{\sqrt{z^2 - x^2}} dx, \tag{2.47}$$

where $p_{IQ}(x)$ is the pdf of the I component and of the Q component. Suppose the I and Q are independent Gaussian with an equal variance, then equation 2.47 simplifies to

$$f_Z(z) = \frac{z}{\sigma^2} exp^{\frac{z^2}{2\sigma^2}}, \tag{2.48}$$

which represents the Rayleigh distribution as was given in Chapter 2.4.2. When the I and Q have the pdfs as were derived in equation 2.40 with the parameter N, which reflects the number of carriers summed together, equation 2.47 becomes,



(a) N=2 (b) N=3

(c) N=12 (d) N=∞

Figure 2.26: The pdf of amplitude of a signal consisting of N normalized orthogonal QAM carriers

$$f_Z(z,N) = \int_0^z 4\,\frac{z p_{nc}\left(\sqrt{z^2-x^2},N\right) p_{nc}(x,N)}{\sqrt{z^2-x^2}} dx. \tag{2.49}$$

Fig. 2.26 shows the resulting pdfs of equation 2.49 for several values for N, which shows the pdf of the signal. The complementary cumulative distribution function of this function can be found by using the following equation

$$f_{ccdf}(a,N) = 1 - \int_0^a f_z(z,N)dz, \tag{2.50}$$

In Fig. 2.27 the complementary cumulative distribution function is shown. The figure clearly indicates the difference between the Rayleigh distribution ($N = \infty$) and the signal consisting of only a few carriers. As can be expected, the lower the number of carriers the lower the likelihood that a certain value is exceeded.

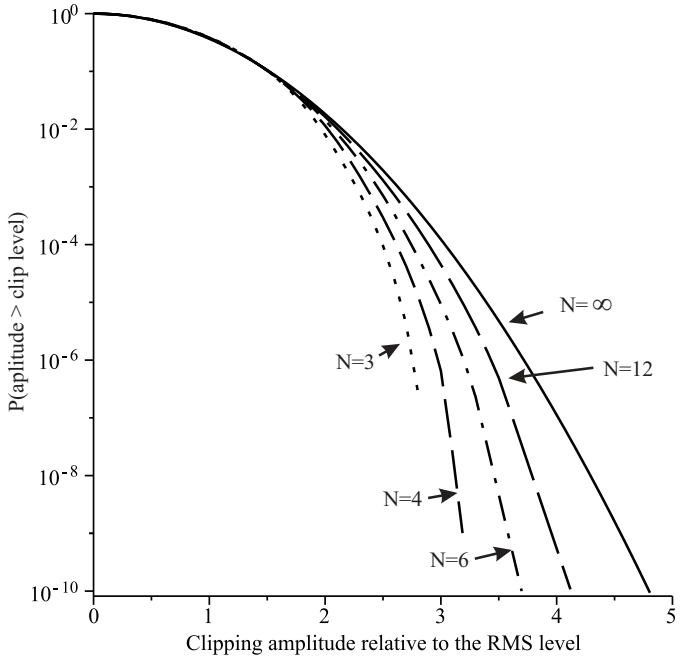


Figure 2.27: Complementary Cumulative Rayleigh distribution for N=3, N=4, N=6, N=12 and N=∞ carriers

2.5 Conclusion

In this chapter, an introduction of the multi-carrier QAM communication system was given, with the description of the transmitter, the channel and receiver on functional level. Methods how the quality of a QAM transmitter can be evaluated efficiently were introduced. One of the largest challenges in multi-carrier communication systems is their high peak-to-average power ratio. Selecting the clip-levels of the system such that clipping does not occur, would result

in a non-optimal system. Therefore some clipping of the multi-carrier signal should be allowed. The clip level of the signal should be selected such, that the combined distortion due to quantization and clipping is minimized.

3

Multi-carrier DOCSIS transmitter

In this chapter the topology of the DOCSIS cable infrastructure will be introduced. In this infrastructure many systems have to work together. In order to ensure that equipment from different vendors can work together, a standard was defined. In this chapter the key parameters of the RF interface specification will be given, which will be used throughout this thesis to derive the component specifications.

3.1 DOCSIS system architecture

Since 1987, the FCC has been encouraging the development of high definition television (HDTV) to replace the analog NTSC system [30]. The HDTV system has a high resolution that approaches the quality of 35-mm film and a wide screen aspect ratio of 16:9 instead of the narrow screen 4:3 aspect ratio.

In 1993 a joint group was formed to define a standard for digital TV (DTV). This resulted in the 1996 FCC DTV standard. The standard is actually several standards combined with different aspect ratios and resolutions [30]. From 4:3 with 640x480p and 24 frames/s up to 1920x1080p and 30 frames/s.

The bit rate required for the uncompressed HDTV video data is vast. For example for video with 1920x1080p video data the required bit rate is given as 1080 lines, 1920 pixels per line, 8 bit per sample, 30 frames per second and 3

primary colors (RGB). The bit rate is 1080 x 1920 x 8 x 30 x 3 = 1500Mb/s. The video data is therefore compressed with a factor of about 75 to a typical bit rate of 19.39Mb/s by using a Motion Pictures Experts Group (MPEG) encoding technique.

The increasing number of digital video channels required the cable operators to adapt their network. Many U.S. cable operators are united in the CableLabs research organization [31]. To set a universal specification that includes both hardware and software specifications the OpenCable initiative was started in 1997. It became the industrial response to an FCC mandate for the development of interoperable set tops that could be sold at retail and to cope with the increasing number of TV channels that were broadcasted. The hardware specifications describe a baseline host device configuration for accessing interactive services and are interoperable with cable systems throughout the U.S., thus creating a retail solution for consumer electronics products for cable. The software specifications, coupled with the hardware specifications, solve the problem of proprietary operating system software, thereby creating a common platform for interactive television applications and services.

Shortly after the OpenCable initiative, DOCSIS (Data Over Cable Service Interface Specifications) was defined as an international standard developed by CableLabs[1, 32, 3]. The DOCSIS standard defines the communication and interface requirements for data, upstream as well as downstream, over the cable network. It is currently used by many cable television operators to provide digital television, internet and phone services to their customers.

The first DOCSIS standard was issued in 1997 [1] and revised as DOCSIS 1.1 in 1999. In 2001 the DOCSIS 2.0 was released to better cope with the increased amount of applications requiring two way communication [32]. Recently, in 2006, DOCSIS 3.0 was released which significantly increases the upstream and downstream speed and adds support for new protocols such as IPv6 [3]. All versions of the DOCSIS standard are backward compatible, which simplifies the deployment of newer versions of the standard without requiring to replace all equipment at once.

The original standard was developed in the U.S. The analog television stan-

dard in the U.S. is NTSC, which has a bandwidth of $6MHz$. In Europe PAL is used as television standard, which has a bandwidth of $8MHz$. Therefore, a European variant of the DOCSIS standard was introduced, called EuroDOCSIS, which has a bandwidth of 8MHz per carrier instead of $6MHz$ for the U.S. version. The modulation type of the downstream carriers is 64-QAM or 256-QAM. For the upstream carriers QPSK to 256-QAM is used, depending on the version. The maximum throughput per downstream carrier that can be achieved is $42.88Mbit/s$ for the U.S. variant or $55.62Mbit/s$ for the European variant. The frequency allocation of the DOCSIS standard also differs between U.S. and Europe. In the U.S. the upstream path has a frequency range from 5 to $42MHz$, while in Europe this is from 5 to $65MHz$. With DOCSIS 3.0 this has been extended up to $85MHz$. The downstream carriers are located at higher frequencies and can start from about $50MHz$ to $1000MHz$. The exact allocation and trade-off between the upstream and downstream bandwidth is up to the cable TV provider to choose.

Parameter	Upstream (from customer)	Downstream (to customer)
Frequency	5 - 42 MHz USA 5 - 65 MHz Europe	42 - 850 MHz USA 65 - 850 MHz Europe
Bandwidth/channel	200 kHz to 3.2 MHz	6 MHz USA 8 MHz Europe
Modulation	QPSK or 16-QAM	64-QAM or 256-QAM
Data rate	0.32 – 10.24 Mbps	27 - 56 Mbps
Transmission mode	Transmits bursts in time slots (TDM) with reserved and contention time slots	Continuous stream of data received by all modems

Table 3.1: The DOCSIS 2.0 physical layer specifications

The DOCSIS architecture has two main components: the Cable Modem (CM) that is located at the users location and the Cable Modem Termination System (CMTS) which is located at the Cable television provider. The infrastructure in between usually is a combination of optical fibre cable and coaxial cables,

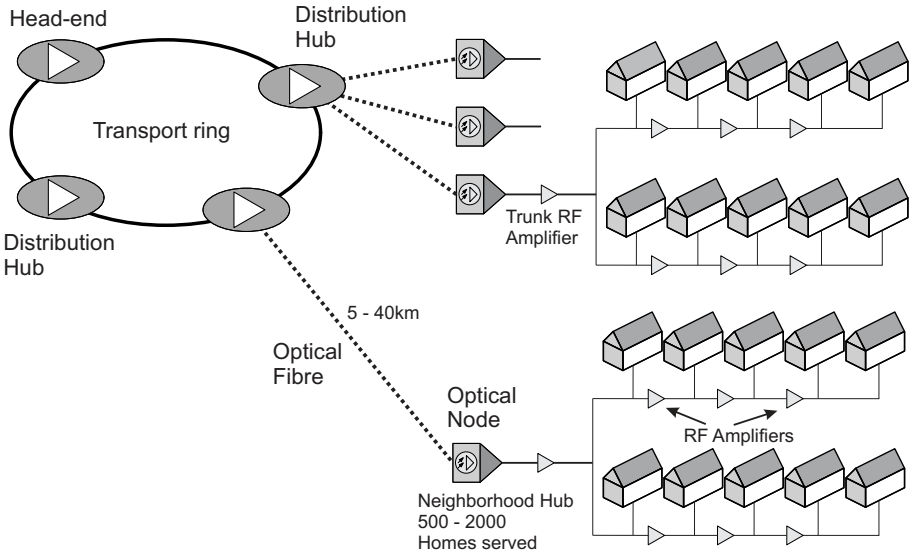


Figure 3.1: The Hybrid Fibre Coaxial network of a typical DOCSIS network

also called Hybrid Fibre Coaxial (HFC), see Fig. 3.1.

The optical fibres extend from the cable operator's head-end to the neighborhood's hubs, see Fig. 3.2. The head-end combines all television, IP and telephony signals and routes them accordingly. The various IP signals are then modulated and upconverted into a RF signal. These RF signals are combined, together with the upconverted analog TV signals, into a single electrical RF signal, which is then fed to an optical transmitter. This optical transmitter converts this RF signal into an optical signal, which is sent through the fibres to the neighborhood hub which translates this optical signal back into an electrical signal without decoding it.

The coaxial connection from the neighborhood hub to the customer has usually a tree-and-branch structure. RF amplifiers are used to restore the signal amplitude to overcome the attenuation of the cable and the losses caused by the splitting of the signal. Each neighborhood hub connects 25 to 2000 homes (typically 500).

The CM receives this signal and filters the information it requires. Depending

on the CM and the connected equipment, it can then translate the digital tv signal into an analog signal, that can be viewed on an analog television. In addition, the CM can route the IP traffic targeted to the local network to and from the cable and it can connect a telephone. As time passes more and more services will be added to the CM.

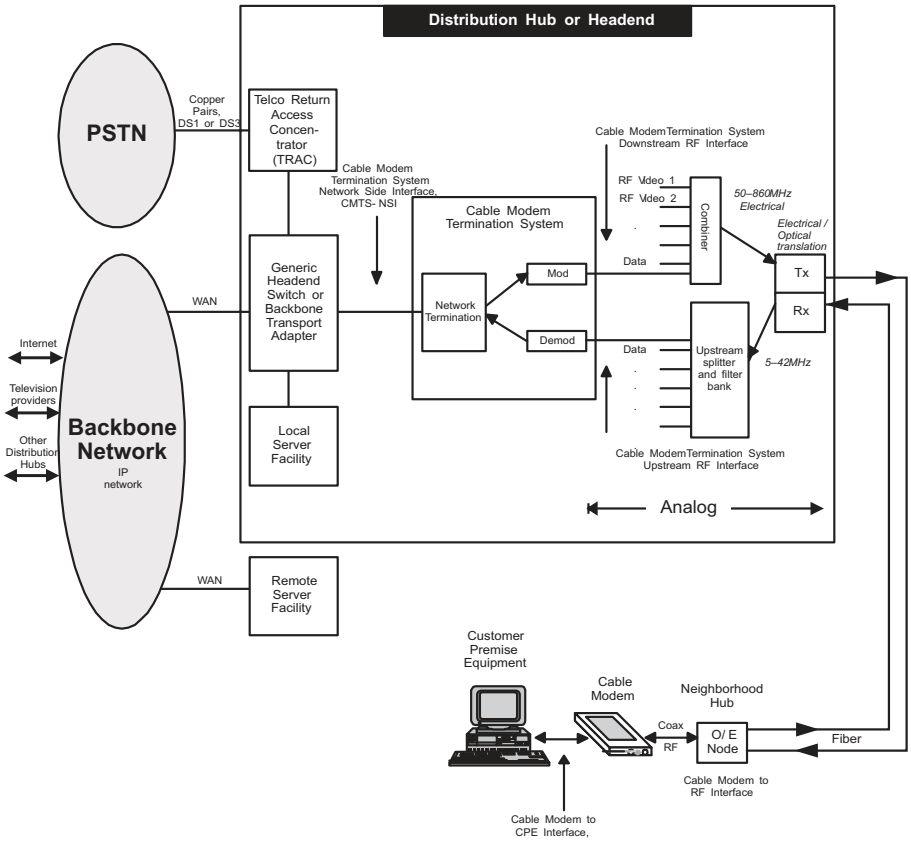


Figure 3.2: The DOCSIS architecture, from Distribution Hub to Customer location [32]

3.1.1 DOCSIS downstream data flow

In this section the encoding and formatting of the downstream data from the cable modem termination system (CMTS) to the cable modem (CM) will be

described.

Historically, the DOCSIS standard was designed only for broadcasting video in the MPEG-2 format. When later other unicast data services, such as IP and telephony were added, the IP data had to be encapsulated into the MPEG packets as framing protocol. This was done to ensure backward compatibility for the cable modems already in use.

The IP data that is sent over the DOCSIS network uses an Open Systems Interconnect (OSI) model, see Fig. 3.3. The IP data from the applications is first broken down into TCP/IP packets, and are put into an ethernet frame. To this ethernet frame the DOCSIS header is appended. The DOCSIS MAC frame is then broken into packets and encapsulated into MPEG-2 frames. Each MPEG-2 frame starts with a 4-byte header. The CMTS inserts a specific packed identifier into the header that identifies the MPEG-2 data as DOCSIS IP data stream. Following the header is an optional one-byte pointer. The pointer is used to reference MAC messages that can extend over multiple MPEG-2 frames. When the pointer is not used this location is filled with data.

Each MPEG-2 frame is 204 bytes long and has a data payload size of 183 bytes or 184 bytes, depending on whether the pointer byte is used. When the length of the data is less that the payload capacity, the remaining locations are filled by ones. These MPEG-2 frames are continuously sent, even if there is no data to transmit. This is done to keep the synchronization between the CMTS and CM correct.

The last 16 bytes of the MPEG-2 frame contains a Forward Error Correction (FEC) code. With this code possible transmission errors can be (partly) corrected, without asking for a retransmission of a complete packet. Common error correcting techniques that are used by TCP can detect errors and in most cases will ask for a packet to be retransmitted. However, retransmission for a real-time, live video stream of packets and data will take too long, therefore FEC is used.

The forward error correction uses Read-Solomon (RS) codes to add redundant bits to the frame that can be used by the receiver to correct for errors, see Fig.3.4. The RS error correction uses a (128,122) code, which means that for

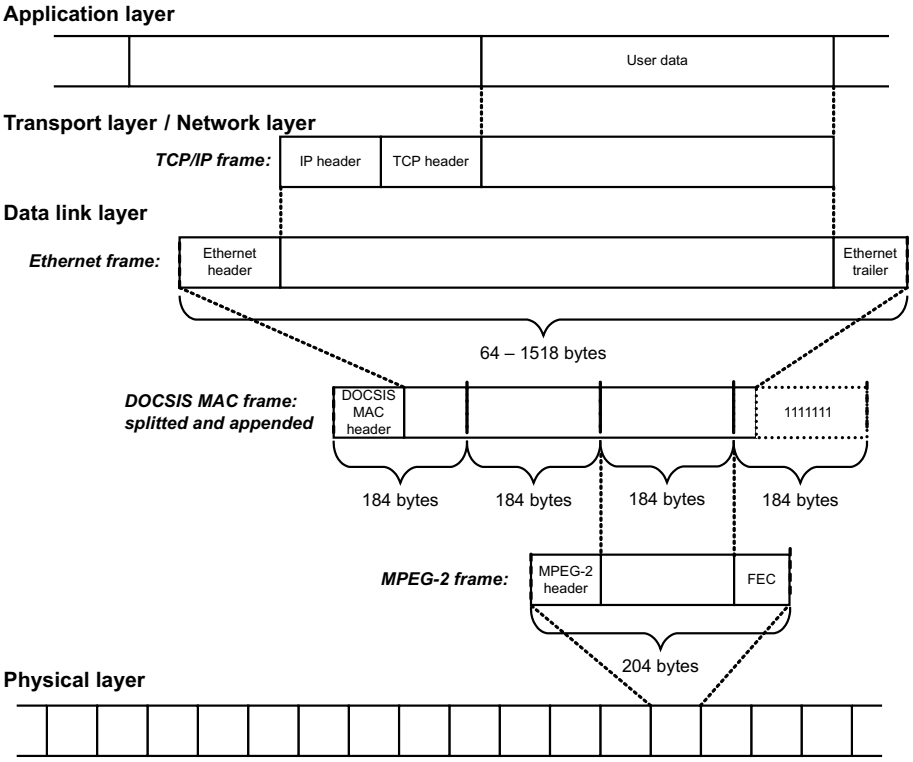


Figure 3.3: The DOCSIS downstream IP data encapsulation, from Distribution Hub to Customer location [32]

every 128 symbols, 122 are used for the data and 6 are used for the error correction [3, 33]. Of these 122-symbols, up to 3 can be corrected by using this code. In addition to this RS-FEC technique, interleaving is used to spread out the errors within a block of data. As errors often occur in bursts, the interleaving process reorders the bits, in an order known both to the sender and to the receiver, that are being transmitted. If a chunk of data is damaged after the reordering by the receiver, the errors will be more spread out. This helps in recovering the data, because spread out errors are easier to detect and to correct by the RS-FEC. The data is interleaved by sending 128-symbols from 128 different packets. The next 128-symbols sent are the second symbol from each of the 128 packets and so on.

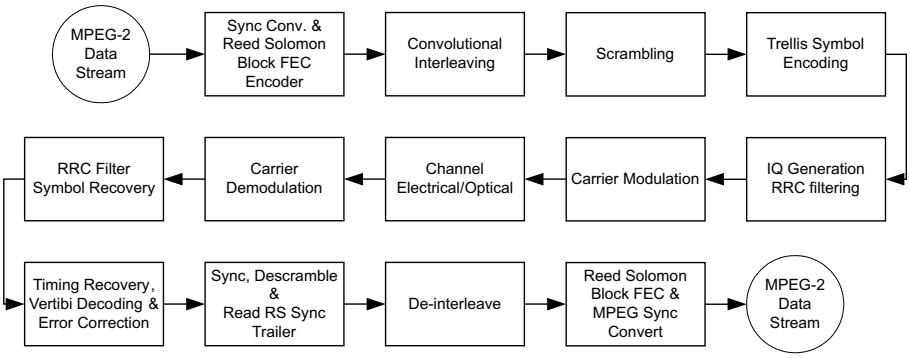


Figure 3.4: The DOCSIS physical layer data flow, from CMTS to CM [32]

The interleaver is followed by a scrambler, to avoid repetitive zeros or ones, and therefore to avoid continuous wave transmission. Then the data is trellis encoded, to further reduce the possible data loss and is mapped to I/Q symbols. These symbols are root-raised cosine (RRC) filtered and modulated onto the carrier. The RF carrier is transmitted over the HFC network and demodulated by the CM. At the CM the process is reversed to recover the data.

The maximum post-FEC BER that is specified in the DOCSIS standard is 10^{-8} for a carrier-to-noise ratio of $23.5dB$ for 64-QAM and $30dB$ for 256-QAM. In order to reach those BER levels the pre-FEC BER should be better than 10^{-7} [34].

3.2 DOCSIS transmitter requirements

In this section a few aspects of the DOCSIS RF interface standard are analyzed. Until end 2006 the DOCSIS specifications (DOCSIS 2.0) specified only single carrier systems. The increasing demand of bandwidth that was used by applications, such as Video on Demand and Internet, placed a further claim on the HFCs digital spectrum. This led to the wish of operators to save scarce rack space and cost per channel. While until as recently as 2004 only a single QAM carrier per RF output port was common, since then there are more and more modulator devices that can generate 2, 4 or even 8 contiguous channels

per RF output port.

When defining the specifications of a multi-carrier transmitter a number of requirements have to change: the spectral distortion mask and the signal energy per carrier. Therefore, these multi-carrier requirements are analyzed in the following sections. Later, in the DOCSIS 3.0 specification, multiple carriers and the corresponding specifications were also defined in the standard. The new spectral mask requirements are equal to the direct translation of the single carrier mask to multi-carrier.

Beside these changes, other specifications changed as well, for example, the frequency range that can be used increased. Other requirements for multi-carrier are for instance somewhat relaxed compared to single carrier, e.g. the signal level requirements.

3.2.1 Frequency range

The RF requirements where a DOCSIS 2.0 head-end termination system should comply with, are summarized in table 3.2. Except for the frequency range these specifications were kept the same in the DOCSIS 3.0 standard. In the DOCSIS 3.0 standard the required frequency range is set to $91MHz$ - $867MHz$ and an optional frequency range of $57MHz$ - $999MHz$. In some parts of this thesis this extended frequency range is used for the analysis. However, some parts use the DOCSIS 2.0 frequency range as standard.

3.2.2 Spectral requirements

The requirements of the transmitter in a telecommunication system are mainly determined by the spectral mask requirements. To prevent that different carriers interfere with each other, mask requirements are set by standards. The challenges in the design of the transmitter are thus related to the spectral purity of the modulated signal at the output of the transmitter. This applies in particular to systems where many carriers are closely spaced in frequency and the spectral impurity of one carrier can affect the neighboring channels.

Parameter	Value
Center Frequency (fc)	91 to 857 MHz ±30 kHz [1]
Level	Adjustable over the range 50 to 61 dBmV
Modulation Type	64QAM and 256QAM
Symbol Rate (nominal)	
64QAM	5.056941 Msym/sec
256QAM	5.360537 Msym/sec
Nominal Channel Spacing	6 MHz
Frequency response	
64QAM alpha	~0.18 Square Root Raised Cosine shaping
256QAM alpha	~0.12 Square Root Raised Cosine shaping
Total Discrete Spurious Inband (fc ± 3 MHz)	< -57dBc
Inband Spurious and Noise (fc ± 3 MHz)	< -48dBc; where channel spurious and noise includes all discrete spurious, noise, carrier leakage, clock lines, synthesizer products, and other undesired transmitter products. Noise within +- 50kHz of the carrier is excluded.
Adjacent channel (fc ± 3.0 MHz) to (fc ± 3.75 MHz)	< -58 dBc in 750 kHz
Adjacent channel (fc ± 3.75 MHz) to (fc ± 9 MHz)	< -62 dBc, in 5.25 MHz, excluding up to 3 spurs, each of which must be <-60 dBc when measured in a 10 kHz band
Next adjacent channel (fc ± 9 MHz) to (fc ± 15 MHz)	Less than the greater of -65 dBc or -12dBmV in 6MHz, excluding up to three discrete spurs. The total power in the spurs must be < -60dBc when each is measured with 10 kHz bandwidth.
Other channels (47 MHz to 1,000 MHz)	< -12dBmV in each 6 MHz channel, excluding up to three discrete spurs. The total power in the spurs must be < -60dBc when each is measured with 10kHz bandwidth.
Phase Noise	1 kHz - 10 kHz: -33dBc double sided noise power 10 kHz - 50 kHz: -51dBc double sided noise power 50 kHz - 3 MHz: -51dBc double sided noise power
Output Impedance	75 ohms
Output Return Loss	> 14 dB within an output channel up to 750 MHz; > 13 dB in an output channel above 750 MHz
Connector	F connector per [ISO-169-24]

1. ±30 kHz includes an allowance of 25 kHz for the largest FCC frequency offset normally built into upconverters.

Table 3.2: DOCSIS 2.0 CMTS specifications [32]

The DOCSIS spectral mask requirements specify the ratio between the energy of the wanted signal and the energy that is leaked in the adjacent channel. This is commonly called the Adjacent Channel Leakage Ratio (ACLR). In Table 3.2 these values are specified for the two adjacent channels.

The spectral mask, defined in the DOCSIS 2.0 standard, for the transmission of

a single carrier is given in Figure 3.5. For multi-carrier transmission this single carrier mask had to be adapted: both the noise and the specifications with respect to the spurious components of a system that transmits N contiguous carriers should match to a combination of N single carrier systems that each comply to the single carrier mask specifications.

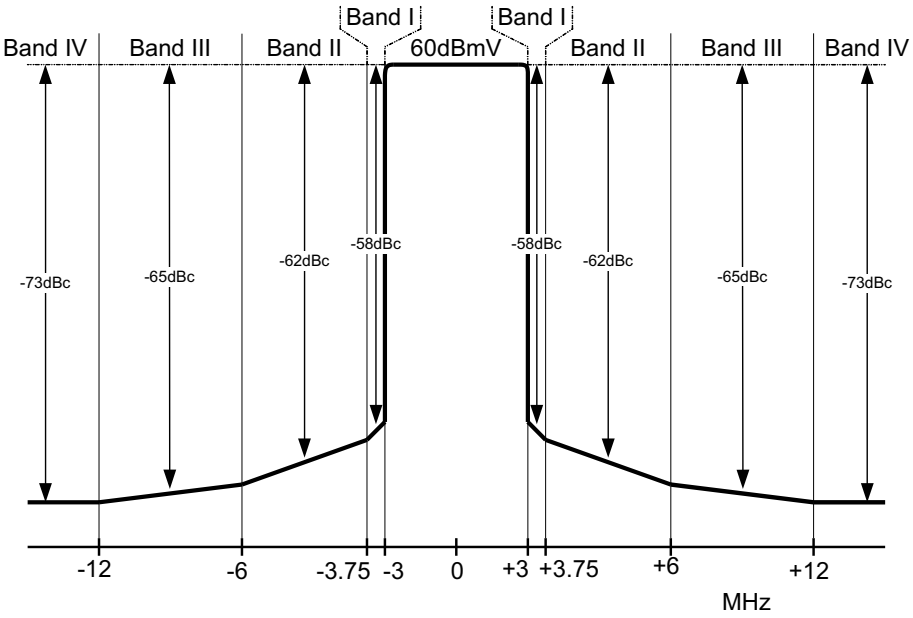


Figure 3.5: Single carrier spectral mask specifications

In Fig. 3.6 the combination of two single carrier masks are shown. The levels for the carriers group mask requirements are given as follows:

Band I:

$$< 10 \log_{10} \left(10^{-\frac{58}{10}} + \left(\frac{0.75}{6}\right) \left[10^{-\frac{65}{10}} + (N-2) 10^{-\frac{73}{10}} \right] \right)$$

Band II:

$$< 10 \log_{10} \left(10^{-\frac{62}{10}} + \left(\frac{5.25}{6}\right) \left[10^{-\frac{65}{10}} + (N-2) 10^{-\frac{73}{10}} \right] \right)$$

Band III:

$$< 10 \log_{10} \left(10^{-\frac{65}{10}} + (N-1) 10^{-\frac{73}{10}} \right)$$

Band IV:

$$< -73 + 10 \log_{10} (N)$$

The computed values are given in Table 3.3. In this table, also the specified DOCSIS 3.0 values are shown [3]. Except for some rounding they are equal to the calculated values.

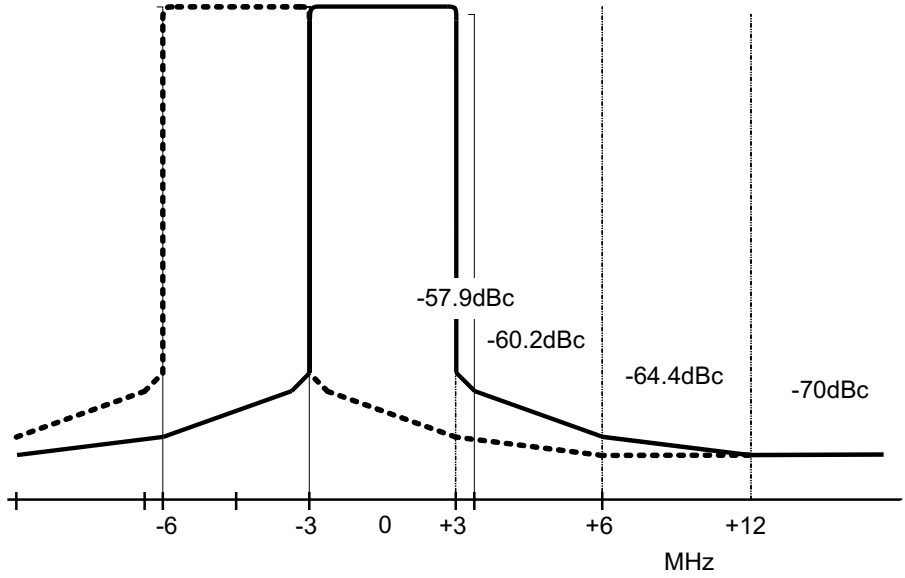


Figure 3.6: Two single carrier spectral mask specifications

3.2.3 Signal level requirements

The total output power for a single carrier is given in table 3.4. It is at most $60 dBmV$ in 75Ω, which is equal to $1 Vrms$ or $11.25 dBm$.

To avoid oversteering the system, when multiple carriers are combined in a single system, the output power per carrier must be reduced. Assuming the

Computed							
$N =$	1	2	3	4	6	8	12
Band I	-58	-57.89	-57.88	-57.86	-57.83	-57.79	-57.73
Band II	-62	-60.42	-60.22	-60.02	-59.65	-59.31	-58.71
Band III	-65	-64.36	-63.80	-63.31	-62.46	-61.76	-60.62
Band IV	-73	-69.99	-68.23	-66.98	-65.22	-63.97	-62.21
DOCSIS 3							
Band I	-58	-58	-58	-58	-58	-58	-58
Band II	-62	-60	-60	-60	-60	-59.5	-59.5
Band III	-65	-64	-63.5	-63	-62	-61.5	-60.5
Band IV	-73	-70	-68	-67	-65	-63.5	-62

Table 3.3: Multi-carrier spectral mask requirements

individual carriers are uncorrelated, the power per channel must be reduced by $3dB$ for every doubling of the number of carriers. However, as given in Chapter 2, the required back-off as a function of the number of combined carriers is more than the $3dB$ that would be expected from the passive combining in the case of multiple single carrier transmitters. It was found that the back-off ratio that preserves the required distortion level by combining two carriers increased by $5dB$ [35] instead of $3dB$, because the carriers will not be fully uncorrelated. Again $5dB$ is required for a further doubling from 2 carriers to 4 carriers. Because the required back-off increases initially more than expected, more amplification is required when the number of carriers increases to keep the energy per carrier constant. In the DOCSIS 3.0 standard, however, they have opted to reserve less energy per carrier, instead of varying the amplification in the CMTS depending on the number of carriers that are combined. This simplifies CMTS design, because not always all outputs are used for a CMTS. For example a CMTS able to generate 4 carriers can also be used to generate a single carrier. With these DOCSIS 3.0 specifications there is no need to change the signal amplification (or hardware). The power levels that are required are given in Table 3.4

'*N*' = number of combined channels:	Required power in dBmV per channel
$N = 1$	60 dBmV
$N = 2$	56 dBmV
$N = 3$	54 dBmV
$N = 4$	52 dBmV
$N > 4$	60 – ceil [3.6*log2(*N*)] dBmV

Table 3.4: DOCSIS 3.0 power requirements [3]: required power per channel for N channels combined onto a single RF port

3.3 Conclusion

In this chapter the topology of a Hybrid Fibre Coaxial (HFC) system was given, and the basic specifications for the RF interface of the DOCSIS standard. When multiple carriers are combined onto a single RF port the specifications change. The effects on the spectral mask and the signal levels were analyzed. These specifications will be used in the thesis to derive the requirements of the various components.

4

Multi-DAC DOCSIS transmitter system

Since transmitters for cable television systems are meant for a specialistic market with only a low number of suppliers for transmission systems, only a few papers are published about those transmitters. However, many more papers are published about DOCSIS receivers. Since the specifications, such as frequency range, signal levels, etc, are similar for the transmitters and receivers on many aspects, these papers are also used as a reference [32]. The main difference in the specifications of the receiver and transmitter are in the required signal quality, such as spurious free dynamic range of the signal and phase noise of the oscillator. The conventional transmitter designed to transmit the DOCSIS carriers has to comply with the specifications as given in the previous chapter, in Table. 3.2. In this chapter the potential architectures and their components are discussed for a single carrier DOCSIS transmitter, including their complexity and power consumption. For this analysis a solution with discrete components will be assumed.

4.1 Architecture options and selection

The frequency range specified by the DOCSIS standard, 50 to $1000MHz$, covers more than 4 octaves. This large range complicates the design of the transmitter. In this section two common transmitter architectures are compared.

The first is the Direct Conversion architecture, as shown in Fig. 4.1. The second is the Dual Conversion architecture as is shown in Fig. 4.3.

4.1.1 Direct conversion transmitter

Fig. 4.1 shows a Direct Conversion transmitter, also called Homodyne architecture. In this transmitter architecture the base-band signal is directly up-converted to the desired RF frequency.

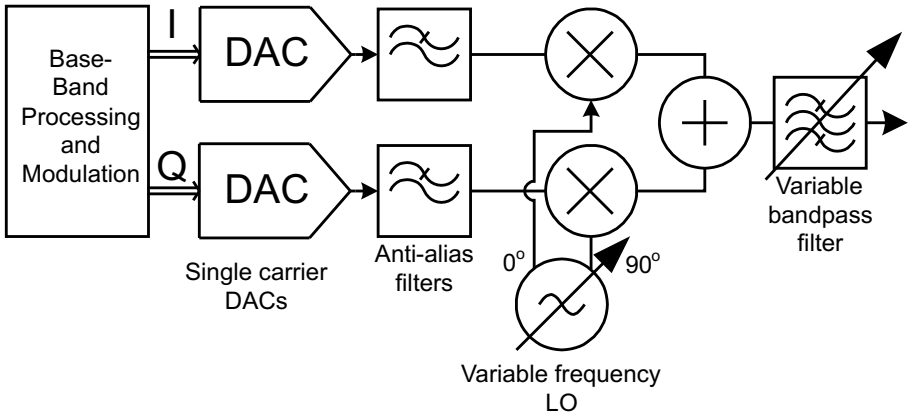


Figure 4.1: Direct conversion transmitter

This transmitter structure has the advantage that it is quite simple, compared to the Dual-Conversion transmitter, as will be discussed in Chapter 4.1.2, that the power consumption is lower and that no external SAW filters are required [36]. Fewer components are required because the IF VCO + PLL circuit components and corresponding mixer and filters are eliminated.

In Fig. 4.2 the frequency plan of the direct conversion transmitter is shown. Fig. 4.2a shows the output frequency range of the transmitter. The complex signal at the output of the DACs is shown in Fig. 4.2b.

However, given the stringent requirements of the DOCSIS standard, the output signal of the Direct Conversion transmitter requires still filtering. These filters are required to prevent the transmitter to transmit harmonics of the RF signal, see 4.2c. This is a side effect of a switching type mixer which is commonly

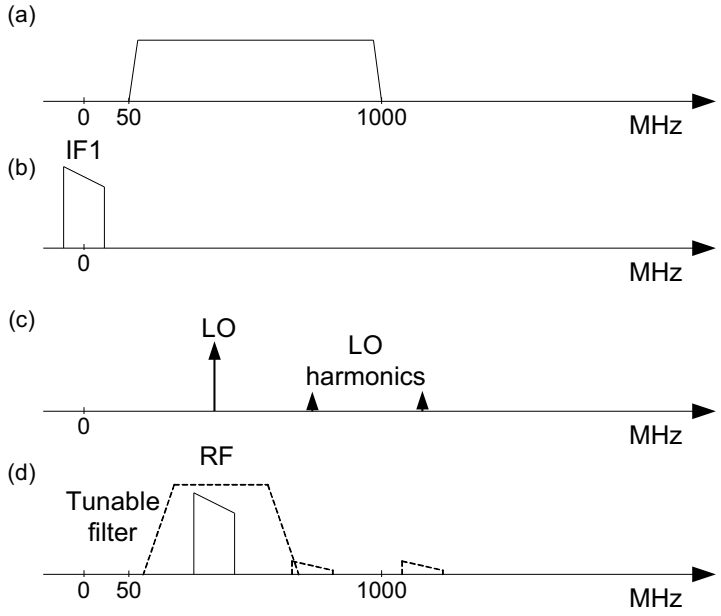


Figure 4.2: Frequency plan direct conversion transmitter architecture

used to achieve the linearity specifications, as is shown in Chapter 4.2.3, that effectively performs a multiplication with a square-wave signal that inherently contains a large number of odd harmonics [37, 38]. The filters must be adjusted to the actual frequency that is transmitted. Given the large frequency range over which these filters should be tuneable, 50 - $1000MHz$, the steepness of these filters and LO harmonic suppression will be limited, see Fig. 4.2d. As a result, the out-of-band attenuation required by the specifications is difficult to reach. Therefore, a high order tunable filter has to be used which has a high complexity, and because of that, is difficult to realize.

To relax the requirements of the filters, the frequency band is usually subdivided into several, e.g. 3, signal bands in order to achieve enough attenuation over the complete signal bandwidth. However, this method increases the complexity of the system significantly and is usually not preferred.

4.1.2 Dual conversion transmitter

In the Dual Conversion transmitter as shown in Fig. 4.3, also called Heterodyne architecture, the signal that has to be transmitted is first up-converted with a fixed LO1 frequency to an intermediate frequency (IF2) signal band. This signal is passed through a fixed filter to remove all harmonic frequencies and LO products. The filtered signal is then down converted with a variable LO2 frequency to the desired RF frequency.

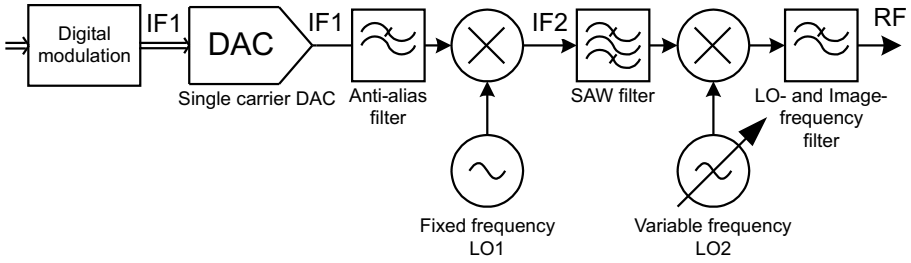


Figure 4.3: Dual conversion transmitter architecture

In this section several common architectures of dual conversion transmitters will be investigated that could be used to implement the conventional transmitter. For each of these architectures it is analyzed whether they can fulfill the requirements as set by the DOCSIS standard.

Although the transmitter architecture, as shown in Fig. 4.3, is commonly called a dual conversion transmitter, there are in fact three locations where the signal is modulated:

- in the digital part of the system,
- at the first LO,
- at the second LO.

In Fig. 4.4 the frequency plan of the "dual" conversion transmitter is shown.

Each modulator can be implemented as a Double Sideband (DSB) modulator or as a Single Sideband (SSB) modulator. This results in 8 possible implemen-

tations. In the following sections four of these possible implementations are considered relevant and will be analyzed further, namely

- DSB/DSB/DSB
- DSB/SSB/DSB
- DSB/SSB/SSB
- SSB/DSB/DSB

DSB/DSB/DSB

In Fig. 4.4 the frequency plan is shown for the dual conversion transmitter as shown in Fig. 4.3, where all the modulators are implemented as DSB. Fig. 4.4a shows the output frequency range of the transmitter. The IF signal band, IF1, is usually centered around a frequency of $44MHz$ (or $36MHz$ in Europe), see Fig. 4.4b, because traditionally this is the IF signal band of the analog tuner, e.g. $44MHz$ for NTSC or $36MHz$ for PAL. Because cheap SAW filters do exist for these frequencies, it has become a de facto standard.

Then, after the first mixer, the wanted signal and its image have a distance of 2 times IF1, see Fig. 4.4c. The IF2 filter after the second mixer needs to attenuate the image frequency to a level below the out-of-band specification, i.e. more than $73dBc$, see Fig. 4.4d.

While the RF frequency of the system is defined in the standard of the system, the transmitter's internal IF2 signal band is commonly not defined. The designer of the transmitter has to select the most optimal frequency. The choice for the IF2 signal band is flexible. However, constraints are present that make certain frequencies more suitable than others.

The IF2 signal band should not be within or nearby the frequency band ($50MHz$ - $1000MHz$) of the wanted RF signal. This enables the filtering of the negative image of the mixer and reduces the unwanted LO leakage to the output.

The typical IF2 signal band frequency for a Dual-Conversion DOCSIS transmitter is above the highest RF frequency that is required. The superiors mix

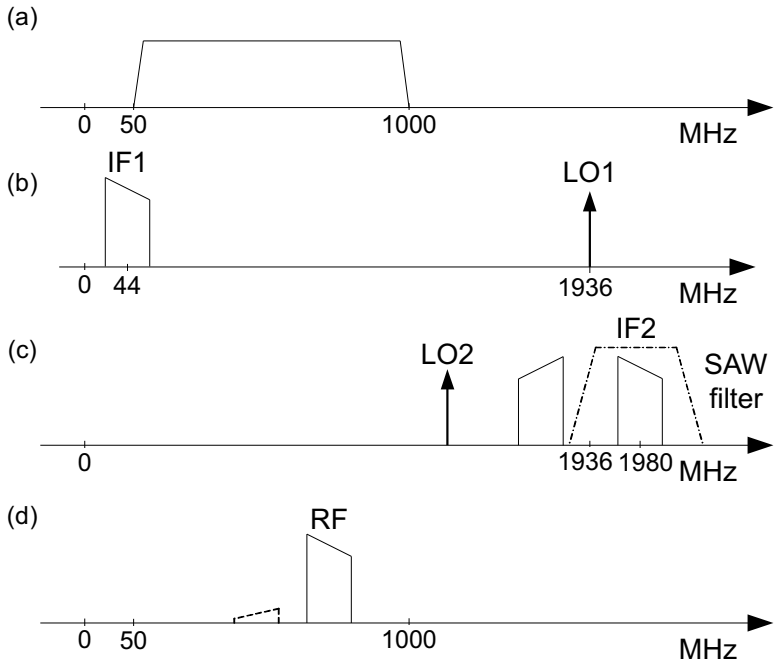


Figure 4.4: Frequency plan dual conversion transmitter architecture with a IF1 signal band around 44MHz

product and their locations of the mixer can be calculated with the following equation.

$$f_{RF} = |\pm m f_{IF} \pm n f_{LO}|\,, \tag{4.1}$$

where m and n are integers that denote the harmonics of the f_{IF} and f_{LO}, respectively. For the second mixer is the the lowest LO2 frequency required to mix to the highest RF frequency. To ensure that the harmonic frequencies of the LO2 signal that will be mixed with the IF2 signal do not fall inside the bandwidth of interest, the IF2 signal band frequency should be sufficiently high. Therefore, the IF2 signal band mixed with the second harmonic, the first unwanted harmonic and commonly the most problematic harmonic, of the LO2 should fall outside the bandwidth of interest. With a frequency range of 50 to $1000MHz$, the IF2 signal band should be higher than $1950MHz$. A higher

IF2 signal band is desired to avoid a steep high pass filter, to filter the the out-of-band components below $50MHz$.

The IF2 signal band SAW filter after the second mixer needs to attenuate the image to a level below the out-of-band specification, i.e. more than $73dBc$, see Fig. 4.4d. Since most SAW filters reach at most $60dBc$ in these frequency ranges [39], additional measures must be taken to ensure enough attenuation of the IF2 image. The options are:

- Increasing the IF1 frequency
- Multiple SAW filters in cascade
- Using a single sideband mixer
- Using zero-IF

By *increasing the IF1 frequency*, the images are further apart and with the SAW filter, additional suppression of the image becomes possible. However, because the additional filtering is done at high frequencies, where it is difficult to achieve a small transition bandwidth, the IF1 signal band should be very high in order to make the filtering effective. Therefore this option is not viable.

By using *multiple SAW filters in cascade* the out-of-band attenuation increases to a level, that is enough to fulfill the DOCSIS requirements. The disadvantage is, however, that the passband loss also increases. This requires more signal amplification to restore the amplitude. Because of this additional attenuation of the signal it becomes difficult to reach to required signal-to-noise ratios. In addition, the passband ripple also increases to levels close to or even exceeding the maximum limits as specified by DOCSIS, which is maximally $0.5dB$ amplitude ripple within the channel bandwidth. For these reasons this solution is not preferred.

Single-carrier DAC sample rate The implications of this architecture for the sample rate of the DAC which is part of the baseband, are mainly determined by the low pass Nyquist filter that follows the DAC. The higher the order

of the filter, the steeper the frequency response (while keeping the other filter parameters constant). At the same time, the complexity of the filter increases. The required suppression of the Nyquist images is more than $73dBc$. From the distance of these images, the filter characteristic and the required attenuation, the minimum order required can be calculated.

Several types of filters can be selected for the low-pass filter at the output of the DAC. As will be shown in Chapter 5.5, the Butterworth filter characteristic is commonly selected for this purpose. For the Butterworth filter characteristic, the order that is required to obtain a given suppression and transition bandwidth is given by the following equation [22]

$$O_{Butterworth} = \left\lceil \frac{\log_{10} \frac{10^{Attn/10}-1}{10^{3.01/10}-1}}{20 \log_{10} \left(\frac{f_s - f_{out}}{f_{out}} \right)} \right\rceil , \tag{4.2}$$

where f_s is the sample rate of the DAC, f_{out} is the highest wanted signal frequency and $Attn$ is the desired attenuation of the Nyquist image. When for example a low pass pass filter is limited to a 5th order Butterworth filter, where the first IF signal band is centered around $44MHz$, the sample rate must at least be equal to $320MS/s$.

DSB/SSB/DSB

Alternatively a *Single Sideband (SSB) mixer* could be used for the first mixer, see Fig. 4.5. This SSB mixer consists of two mixers with a 90 degrees phase shift between them. In the SSB mixer any mismatch between the I/Q phase will result in a residual image frequency (imperfectly rejected). If K is the linear-amplitude imbalance between the I and Q channel and ϕ the phase deviation from quadrature, then the residual sideband suppression in dBc bellow the desired sideband is given by [40]

$$RSB = 20 \log_{10} \sqrt{\frac{K^2 - 2K \cos \phi + 1}{K^2 + 2K \cos \phi + 1}}, \tag{4.3}$$

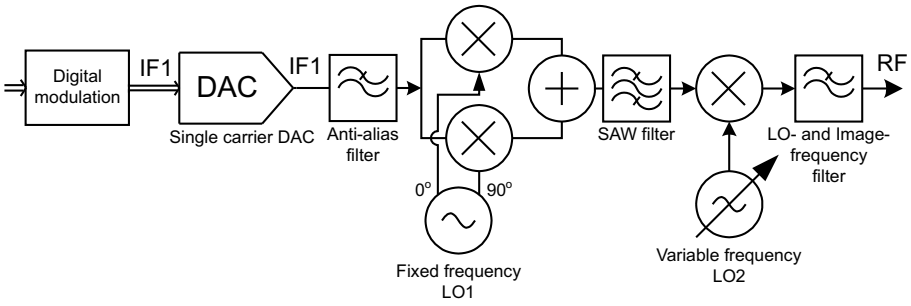


Figure 4.5: Dual conversion transmitter architecture with a first single sideband mixer

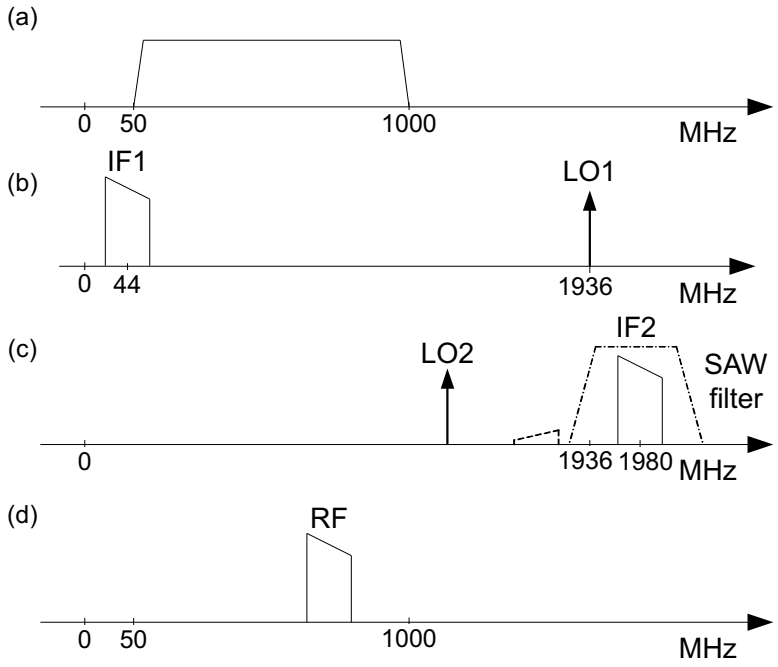


Figure 4.6: Frequency plan dual conversion transmitter architecture with a IF1 signal band around 44MHz and a single sideband mixer for the first stage

Typical residual sideband suppressions in off-the-shelf quadrature upconverters at frequencies around $1000MHz$ are about $-40dBc$ [40]. This results in enough attenuation of the unwanted sideband, in combination with the attenuation of the IF SAW filter. Therefore, the combination of a low IF1 signal band with a

first SSB mixer is a viable option to reach the required performance.

Single-carrier DAC sample rate The implications of this architecture for the sample rate of the DAC which is part of the baseband is similar to the previous architecture. The minimum sample rate when a fifth order Butterworth filter is used, is equal to $320MS/s$.

DSB/SSB/SSB

In addition also the *second mixer can be replaced by a SSB mixer*, see Fig. 4.7.

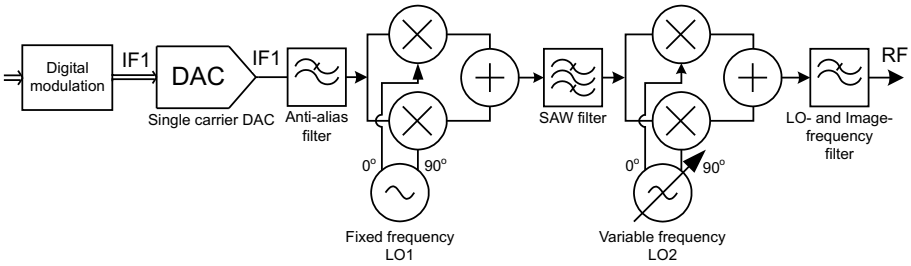


Figure 4.7: Dual conversion transmitter architecture with two single sideband mixer

The advantage of using a SSB mixer for the second stage is the possibility of using a lower frequency band for the IF2, because the second harmonic mixing product of the LO is suppressed by the SSB mixer, see Fig. 4.8. However, this requires suppression levels that are in practice hard to reach. The aforementioned suppression levels of $-40dBc$ are reached with a fixed LO frequency, for the LO2 the frequency range is about one octave making it more difficult to ensure the required 90° phase shift between the two phases. Therefore, by using a SSB mixer for the second LO in combination with a lower IF2 signal band, it becomes difficult to reach the required image suppression levels.

Single-carrier DAC sample rate The implications of this architecture for the sample rate of the DAC which is part of the baseband is similar to the pre-

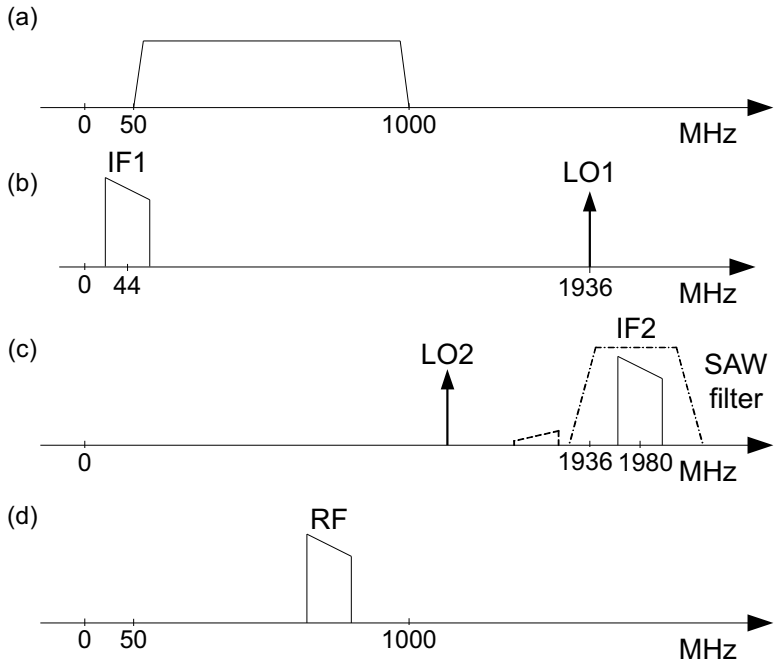


Figure 4.8: Frequency plan dual conversion transmitter architecture with a IF1 signal band around 44MHz and a single sideband mixer for the first and second stage

vious architecture. The minimum sample rate when a fifth order Butterworth filter is used, is equal to $320MS/s$.

SSB/DSB/DSB

Another method to relax the requirements on the IF SAW filter is by *using zero-IF for the first IF*. The frequency plan of the zero-IF transmitter is shown in Fig. 4.10. Fig. 4.10a shows the output frequency range of the transmitter. This zero-IF, see Fig. 4.10b, reduces the need for a steep filter transition band, because the filter does not need to filter a close by image frequency, see Fig. 4.10c.

For the zero-IF architecture the IF1 signal band is centered around zero. When a SAW filter with a center frequency of $1980MHz$ is used, the first LO1 fre-

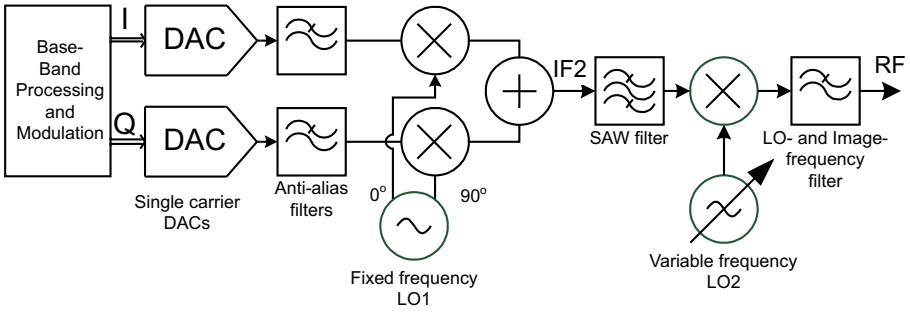


Figure 4.9: Dual conversion transmitter architecture with Zero-IF for IF1

quency is therefore equal to $1980MHz$.

To achieve the output frequency range of 50 to $1000MHz$, the tuning range that is required for the LO2 of the Dual Conversion DOCSIS transmitter is from $980MHz$ to $1930MHz$, which is a tuning range of about one octave. The output frequency and tuning range are important specifications that can have a significant impact on the complexity of an oscillator. In general, the larger the relative tuning range and center frequency the higher the complexity.

The Zero-IF implementation requires two DACs and filters, see Fig. 4.9. Those DACs and filters should be well matched, in order to keep the signal distortion within the limits as specified in the DOCSIS standard.

The dependence of the Modulation Error Rate (MER) on the I/Q phase offset and amplitude balance is, for signals having a small deviation from the ideal constellation, given as [35]

$$MER^{-1} \approx \frac{1-(1-2\delta^2)\cos\theta}{2}, \tag{4.4}$$

where θ is the angular deviation from quadrature and the amplitude imbalance is defined as

$$I/Q\ Gain\ Imbalance = 20\log_{10}\left[\frac{1+\delta}{1-\delta}\right], \tag{4.5}$$

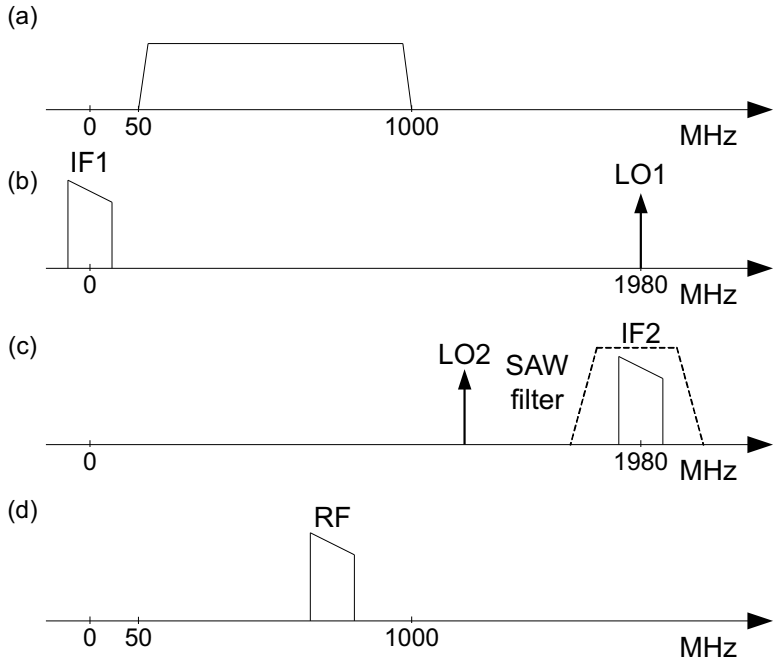


Figure 4.10: Frequency plan dual conversion transmitter architecture with Zero-IF for IF1

and the MER is related to the EVM as

$$MER_{dB} = 10\log_{10}\frac{EVM_{rms}}{Average\ symbol\ magnitude} \tag{4.6}$$

The worst case deviations allowed by ITU-T-J.83 (part of the DOCSIS standard) is $\theta = 1^\circ$ which gives a MER of $41.8dB$ and for $\delta = 0.00289$ (a gain imbalance of $0.05dB$) a value of $50.8dB$ is obtained for the MER. When both exist simultaneously, the composite MER is equal to $40.73dB$.

Single-carrier DAC sample rate The sample rate for the single carrier DACs, as shown in Fig. 4.9 can be calculated using the same analysis as given before. Both of them should be able to at least handle a bandwidth of half the signal bandwidth. Since a DOCSIS carrier has a bandwidth of $6MHz$, the

minimum bandwidth for each DAC is $3MHz$. When for example a low pass pass filter is limited to a 5th order Butterworth filter, a sample frequency of at least $20MS/s$ is required for the zero-IF architecture.

This architecture uses Zero-IF for the first IF instead of $44MHz$ for the architectures described before. In both cases the filters were chosen to be a fifth order Butterworth filter. Although the filters are both 5th order, the first filter has a higher complexity because of its higher frequency. The sample rate of the zero-IF architecture compared to the architecture with a $44MHz$ IF frequency, the sample rate of the digital circuits and of the DAC are decreased by a factor of 16. With all other components being equal this will increase the power consumption significantly.

Given the lower complexity of the Zero-IF1 dual conversion transmitter compared to the Low-IF1 in combination with the single sideband mixer, the Zero-IF architecture is preferred and used for the further analysis.

4.2 Components options and selections

4.2.1 Single carrier DAC

The signal that has to be transmitted over the cable is an analog signal, while the signal source is in a digital format. Therefore the signal must be converted at some point in the transmit system. The location where this conversion takes place is not defined by the specification of the DOCSIS standard and is selectable by the designer of the transmitter.

The signal quality requirements of the DAC in the single carrier transmitter architecture are mainly determined by the out-of-band requirements as given in Chapter 3.2. The architecture of the DAC and its typical performance in relation to the physical imperfections will be treated in more detail in Chapter 7.

In the previous described section two frequencies where analyzed for the IF1 frequency, Zero-IF and a IF of $44MHz$. The main advantage of the higher IF

frequency would be that by using that architecture, impairments, caused by I/Q phase offset, I/Q crosstalk, I/Q amplitude imbalance and I/Q timing skew errors, are less relevant because only a single DAC is being used. The zero-IF architecture requires two DACs: one for the I-path and one for the Q-path. The output signal of these DACs should behave in a similar method to achieve enough suppression of the previously given impairments.

A clock frequency of at least $20MHz$ is required, as given before. The required dynamic range of a single carrier as given by the DOCSIS standard can be achieved by a DAC with an effective resolution of more than 10 bits. A more detailed analysis for the requirements of the DACs will be given in Chapter 5.1.

4.2.2 Local oscillator

The basic function of an oscillator in the DOCSIS application is to generate a periodic signal with certain properties, such as a given amplitude, frequency and quality. The frequency of the oscillator for the second LO should be variable, in order to transmit the channels over the complete frequency band of interest.

The most common types of oscillators are the crystal oscillator, LC oscillator and ring oscillator. The crystal oscillator has excellent spectral purity and very good long term frequency stability [41, 42], but its output frequency is not directly tunable. The LC oscillator and the ring oscillator are tunable, but require more power to achieve the same spectral purity [43] and do not have the required frequency stability by itself. These oscillators are therefore often used inside a Phase Locked Loop (PLL) which locks it with a reference frequency from a crystal oscillator. Crystal oscillators used for the reference clock have very good phase noise levels that levels off near 10kHz offset frequency at around $-150dBc/Hz$ [44].

LC oscillators have inherently better phase noise performance than RC oscillators, alleviating the requirements on the PLL loop bandwidth [45]. This allows the use of a narrowband loop with low jitter generation. Another advantage

of an LC oscillator is in its frequency stability and low sensitivity to process variations.

Tuning range

In general, tuning of an LC oscillator can be performed by varying the L or C. The L and C can be varied in a continuous manner or in discrete steps. The most common method is a fixed L with a variable C [43].

The tuning range of an LC oscillator is often limited by the capacitance variation of the varicaps and the tuning voltage. Increasing the intrinsically narrow tuning range of an LC VCO, without significantly degrading the noise performance is a challenge. Band-switching techniques are often used and are a successful method to increase the tuning range and decrease the tuning sensitivity [46, 47, 48]. These methods are needed especially when integrated tuning diodes are used, because of their limited capacitance ratio between the highest capacitance and the lowest capacitance they can achieve. When discrete tuning diodes can be used, other varactors can be applied that have a larger capacitance ratio. An example of such a varactor is the abrupt diode or hyper-abrupt diodes [49]. Capacitance ratios C_{max}/C_{min} of more than 20 are possible with these diodes, which enable large tuning ranges. However, the VCO will have a high tuning sensitivity.

The tuning range must be met under the worst case conditions. Therefore frequency deviations because of temperature and process spread should be taken into account in the tuning range.

Phase noise

The quality factor of an oscillator is usually defined by its phase noise. The phase noise is characterized by the single sideband phase noise to carrier ratio $\mathcal{L}(fm)$ at an offset frequency f_m from the carrier frequency f_{osc}. Oscillators are made of both passive and active components which introduce noise into the system. The noise has various forms in which it manifests itself, including thermal noise, flicker noise and shot noise [50]. When this noise is added to

the periodic signal of the oscillator, it leads to random variations of the output frequency and amplitude. These random variations lead to random changes of the zero crossings or phase of the signal.

The required phase noise of the local oscillator should be low enough in order not to distort the information in the signal that is modulated by the LO. If the phase noise of the modulated signal is too much degraded by the transmitter, constellation points will cross the decision boundaries at the receiver and bit errors will occur. The sensitivity to phase errors increases with the increasing complexity of the modulation. Phase noise is therefore a bigger problem for 256-QAM than it is for 64-QAM. The DOCSIS specification is very detailed for phase noise, specifying the maximum noise power relative to the carrier in the bands above and below the carrier. This type of specifications is typically not used for oscillators. Instead, phase noise is often presented in dBc/Hz, measured at some offset, e.g. $10kHz$, from the carrier [43]. The maximum phase noise specification of $-33dBc$ double sided noise power in $1kHz$ to $10kHz$ [3], see Table 3.2, can be converted into the this spot phase noise by using some assumptions. Assuming symmetry in the noise power spectral density the single side noise power is equal to $-36dBc$. The integral of the phase noise to carrier ratio over this frequency range is specified in the standard to be

$$\int_{1k}^{10k} \mathcal{L}(f)\, df \leq -36dBc. \tag{4.7}$$

Assuming the power spectral density is proportional with $1/f^2$ in this frequency range, the equivalent spot phase noise can be calculated to be $-75dBc/Hz$ at $1kHz$ offset and $-95dBc/Hz$ at $10kHz$ offset.

This specification is well below the typical phase noise performance achieved by today's QAM tuners for cable modems, which typically achieve a phase noise of $-80dBc/Hz$ to $-87dBc/Hz$ at $10kHz$ offset. [51, 36, 38].

To reach the required specifications with integrated VCOs is difficult [43, 52] therefore a discrete solution for the oscillator will be assumed in this chapter.

An early semi empirical phase noise model for LC oscillators was proposed by Leeson in 1966, see Fig. 4.11. This model describes quantitatively the phase

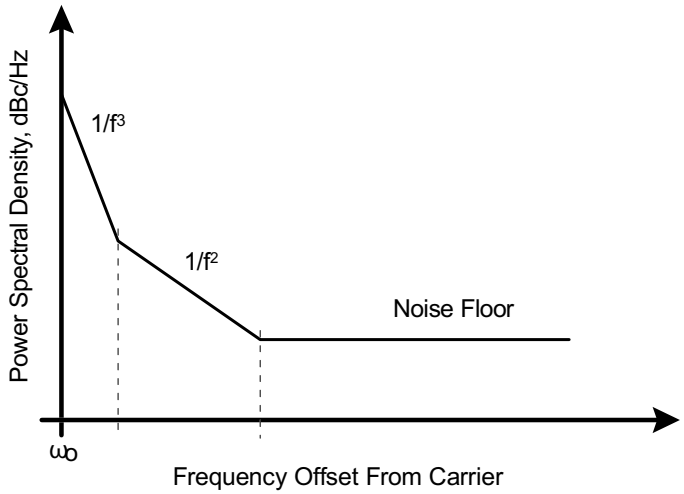


Figure 4.11: Phase noise in the frequency domain

noise as [53]

$$\mathcal{L}(f_m) = kTR\frac{F}{Q^2V_o^2}\left(\frac{f_{osc}}{f_m}\right)^2, \tag{4.8}$$

where Q is the quality factor of the LC tank and R is the equivalent resistance of the LC tank, k is the Boltzmann constant, T is the absolute temperature and F is a fitting parameter describing the noise in the circuit. The main problem of using this equation is the lack of knowledge about the constant F. This constant is, in addition, dependent on the chosen circuit topology. Although the above equation has largely ignored the nonlinear time-varying mechanisms contributing to phase noise in practical oscillators, it provides an insightful equation showing dominant effects.

The constant F for several oscillator topologies is determined by several authors, e.g. [43, 54]. For the bipolar LC oscillator topology, as is shown in Figure 4.12, the LTI approximation is given in [43] as:

$$\mathcal{L}(f_m) = \frac{1}{2Q^2}\frac{kT\left(\frac{\alpha_{ol}}{2}+1\right)}{R_p\frac{2}{\pi^2}I_{tail}^2}\left(\frac{f_{osc}}{f_m}\right)^2, \tag{4.9}$$

where I_{tail} is the current through the current source, R_p is the equivalent tank

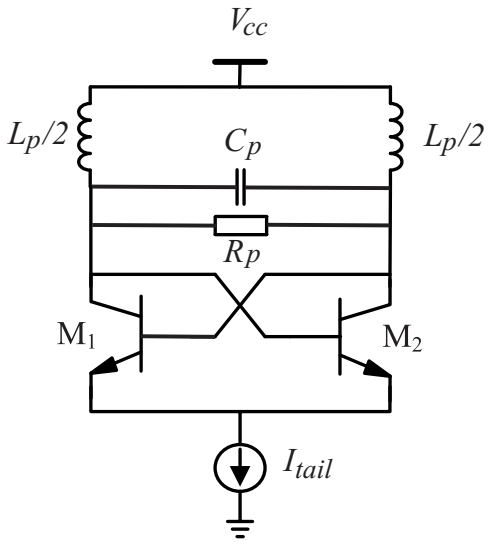


Figure 4.12: Bipolar cross coupled LC oscillator

resistance and α_{ol} is the open loop gain. From this equation an estimate of the power consumption of the VCO can be made, as is done in Chapter 4.3.2. Equation 4.9 approximates the phase noise of an oscillator that is ideal in all respects except for the finite Q of the LC tank. This equation therefore gives the minimum achievable phase noise for a given Q, f_{osc} and power dissipation.

As phase noise is inversely proportional to the square of the quality factor of the tank circuit and the derivative of the phase with respect to the frequency of the LC tank is directly proportional to Q, it is obvious that one can not get very good phase-noise performance along with a large tuning range at a low power consumption [45]. For the frequencies required in the tunable LO2 a typical Q for a good quality inductor over a wide frequency range is equal to about 30 [55]. In Chapter 4.3.2, the power consumption using typical values for the components will be calculated.

4.2.3 Mixers

Mixers are important components of a modulation and demodulation system. The principle of mixing in communication systems is the frequency translation of the signal. The ideal mixer with a perfect LO, so without harmonics or phase noise, will for a given IF signal produce a RF signal at only two frequencies. Filtering can be applied to reject the unwanted frequency component. The relation between the IF, RF and LO frequencies is given by

$$f_{IF} = |f_{RF} \pm f_{LO}|\,, \tag{4.10}$$

Any device that exhibits non-linear amplitude behavior can serve as a mixer [56], as non-linear distortion results in the production, from the signal present at the input of the device, of signals at new frequencies.

The circuit implementation of mixers can be divided into two basic categories; active mixers and passive mixers. This classification is based on the standby power the mixer dissipates.

Active mixers

Active mixers dissipate standby power in the pre-amplification transconductance stage, as shown in Fig. 4.13. The mixer operation is performed by passing the current through a network of switches driven by the LO. The variations in architecture that do exist is almost endless. However, when one considers only the integrated mixers with a frequency range up to a few GHz, only a few mixer architectures dominate.

Active mixers can be made unbalanced, single balanced and double balanced. The double balanced architecture improves the circuit performance with respect to supply and substrate noise at the cost of circuit complexity [57]. The most commonly used integrated mixer architecture is the Gilbert cell multiplier [58] or variants of this architecture. This double balanced differential circuit is insensitive to common mode noise which makes it particular suitable for integration.

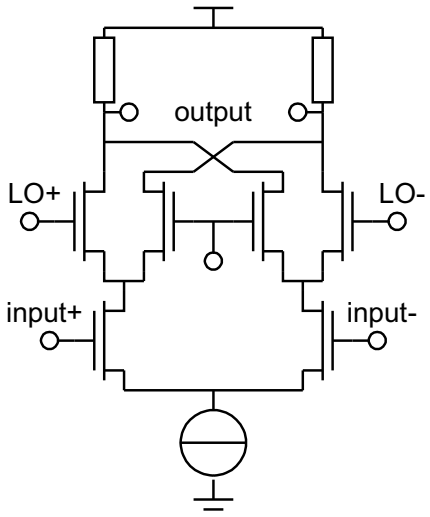


Figure 4.13: Double balanced differential active mixer

However, the transconductance stage of the active mixers is difficult to make linear enough, given the requirements of the DOCSIS standard. Active mixers therefore are not commonly used in cable modem receivers. Passive mixers are used instead [51, 38].

Passive mixers

The passive mixer does not use static power, however, the mixing action introduces a loss in the signal power between the input and the output. This loss of signal power often needs to be compensated by an amplification stage. Because of this loss, it becomes more difficult to keep the NF low. On the other hand, the linearity performance of passive mixers tends to be better [59]. Another issue of this type of mixer is the LO drive strength in order to turn on/off the switches fast and to reduce the on resistance of them to reduce the nonlinearity. For these reasons the LO signal must have a large amplitude. This large LO signal and the signal amplification stage take a considerable amount of power at high frequencies which should be taken into account when comparing the

active and passive mixers.

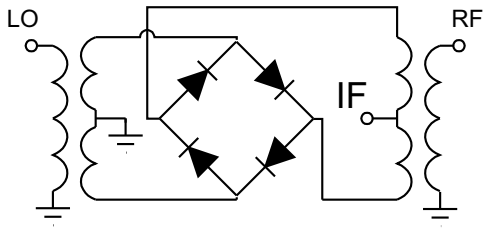


Figure 4.14: Passive diode mixer

For the non-linear elements in the passive mixer diodes, MOSFETs or PHEMTs are often used. Discrete passive mixers modules commonly use diodes, because they normally have a lower Rd_{on} and therefore a lower loss, but they require a higher LO drive strength. The passive mixer can also be made balanced and unbalanced. A double balanced switching mixer uses four switching devices arranged in a ring configuration. Both the LO and RF part are balanced and all ports are inherently isolated from each other. Compared to the single balanced mixer this has as advantage that the linearity increases and the isolation between all ports improves. Because of the double balanced structure the even order products of the LO and RF are suppressed, which results in a reduction of the spurious products. The amount of suppression of the mixer products varies and strongly depends on the quality of the diode matching and the accuracy of the balun balance. The disadvantage of the double balanced mixer is the requirement of two baluns and the higher LO drive level [60].

The double balanced diode mixer is shown in Fig. 4.14. The mixer diodes are being constantly switched on and off within the ring by the high-powered LO stage. The RF signal is alternately sent through the diodes, and thereby mixing the two signals in a nonlinear manner, producing the IF output frequency. Double balanced Mixers commonly function up to $8GHz$ and beyond by using hot-carrier (Schottky) diodes, which possess low-noise and high conversion efficiency [60].

Conversion loss The theoretical conversion loss of an ideal passive mixer without the switch resistance is equal to [61]

$$C_l = \frac{2}{\pi} \approx 3.9dB, \tag{4.11}$$

Additional passive mixer conversion losses are caused by the mixing diodes internal resistance, port impedance mismatches, mixer product generation, and the inevitable $3dB$ that is wasted in the undesired sum or difference frequency. This sum or difference frequency is removed by filtering, cutting down the mixers final output power to half. [60]. The conversion loss of a passive double balanced diode mixer, as shown in Fig. 4.14, is given as [56]

$$\begin{aligned} Loss_{dB} = \quad & Image\,frequency\,loss \\ & + Transformer\,loss \\ & + Losses\,due\,to\,harmonic\,generation \\ & + Diode\,loss. \end{aligned} \tag{4.12}$$

In the case of the double balanced mixer two transformers are used and two diodes are in series. The typical values for the losses are [56]

$$\begin{aligned} Loss_{dB} = \quad & 3 \quad dB\ (Image\,frequency\,loss) \\ & + 1.5 \quad dB\ (Transformer\,loss) \\ & + 1 \quad dB\ (Losses\,due\,to\,harmonic\,generation) \\ & + 0.5 \quad dB\ (Diode\,loss) \\ = \quad & 6 \quad dB. \end{aligned} \tag{4.13}$$

In the case of MOSFET switches with an Rds_{on} of 25Ω, the insertion loss increases with $2.5dB$ to a value of $8.5dB$ [56].

Linearity When the input amplitude rises above a certain level, the output level fails to follow the input level changes proportionally. The Figure of Merit P_{1dB}, the $1dB$ compression point, gives the single tone signal level for which

the output level has dropped $1dB$ below the expected output level. As a rule of thumb for the double balanced diode mixer, this is approximately $6dB$ below the LO power level. To avoid driving the signal into compression another few dB should be added as margin. The highest input level for the mixer should, as first order guide, be $10dB$ smaller than the LO power level.

Multi-tone Intermodulation Distortion (IMD) is a form of common mode mixing in which two or more tones enter the RF/IF port and nonlinearly mix with each other and the LO. Multi-tone IMD can generate interference tones that fall within the bandwidth of interest and therefore places an upper limit on the dynamic range of the transmitter.

The level of the Inter Modulation Distortion (IMD) depends on the intrinsic nonlinear characteristic of the devices, i.e. diodes, MOSFETs, etc., and the balance of the mixer. The most common used Figure of Merit (FOM) for IMD performance is the two-tone third-order intercept point, or IP3. As a rule of thumb, for the double balanced diode mixer the level of the IP3 is approximately $8dB$ greater than the LO power [56]. Increasing the LO drive strength while keeping the RF level constant, decreases the intermodulation distortion of the mixer.

Passive mixers are classified by their LO drive strength. A passive mixer which has a maximum LO drive strength of $7dBm$ is called a level 7 mixer. Increasing the level of the LO further than this maximum value does not increase the linearity much and can damage the mixer. Increasing the LO drive strength can only be accomplished by increasing the number of diodes in each mixer leg from one to two or more in series. Other levels for the LO drive strength that are often used for double balanced passive diode mixers are $10dBm$, $13dBm$ and $17dBm$. Selecting a higher LO level results in better linearity at the cost of a higher power consumption for the LO generation.

Noise figure A mixer contributes to the noise of the signal like any network. The amount of degradation of the SNR of the signal is evaluated in the Noise Figure (NF).

For a passive mixer the NF is almost equal to the mixer conversion loss. How-

ever, the switching components, such as the diodes or MOSFETs, do slighty contribute to the mixers white noise. According to an analysis made in [56], the correction factor to compensate for these switching components is $0.5dB$ for a typical double balanced diode mixer. The total NF for a double balanced mixer is therefore equal to

$$NF_{dB} = (Conversion\ loss)_{dB} + 0.5dB. \tag{4.14}$$

4.2.4 IF filters

After the first upconversion mixer an RF filter is used to remove the images from the mixing stage. The type of filter that is commonly used is a SAW filter [39]. In the transmitter, it effectively hinders spurious signals from being emitted, thus avoiding interference. In the IF stage, SAW filters efficiently limit the signal bandwidth without distorting the signal.

The usage of RF SAW filters in dual-conversion tuners, instead of microwave ceramic filters or discrete LC filters, has several advantages [39]:

- high stopband attenuation (local oscillator (LO) and image frequency rejection, typically 55 - $65dB$);
- low insertion attenuation and flat passband frequency response;
- balanced input and output matching to the IC impedance (e.g., in the range of 50 - 200Ω);

Because the basic SAW transducer has a capacitive reactance at the input and output, some impedance matching of the SAW device is often required. Generally, a simple one- or two-element matching circuit at the input and/or output of the SAW filter is used to reduce insertion loss and to improve its voltage standing wave ratio (VSWR). Only a few types of SAW filters are designed to have input and output impedances that are matched to 50 ohms. In general, the input and output impedances at the terminals of a SAW filter will not be 50 ohms. The procedure for matching the SAW filter will depend on

the required specifications as well as on the type of SAW filter device chosen. Thus, an impedance matching circuit may be required to interface to the SAW filter. For some types of SAW filter, the matching circuit must not provide an ideal match to the external transmission lines, as an improved match results in a larger acoustic radiation condition that exhibits a low insertion loss but at a cost of increased amplitude and phase ripple. Such devices are often purposely mismatched to some degree. [62]

Due to the superior performance of RF SAW filters and the balanced operation at the input and output ports, they are perfectly suited for the application in dual conversion tuners. A disadvantage is the additional board space and the cost of the filters. However, often SAW filters are smaller and cheaper and have a much steeper transition band, compared to the discrete LC filters they replace [63].

The SAW filter required for the IF stage has a fixed center frequency of 1500 - $2000MHz$, depending on the exact choice of the IF frequency. SAW filters in this frequency range have typically an insertion loss of about $6dB$ [39].

The higher the IF2 signal band the lower the required relative tuning range of the VCO for the LO2. At the same time less mixing products of the harmonics of the LO will fall into the band of interest. Therefore, a SAW filter of $1980MHz$, for example the B1639 from Epcos [64], is selected as reference for the calculations given in Chapter 4.3.

4.3 Power estimation of a transmitter

In this section the power for a single carrier conventional dual conversion transmitter will be estimated. The power estimation will use the previously given first order approximations and as a reference for the calculations some commercially available components are applied.

The power will be estimated for the modulator system as shown in Fig. 4.15. For the power calculations several assumptions are made:

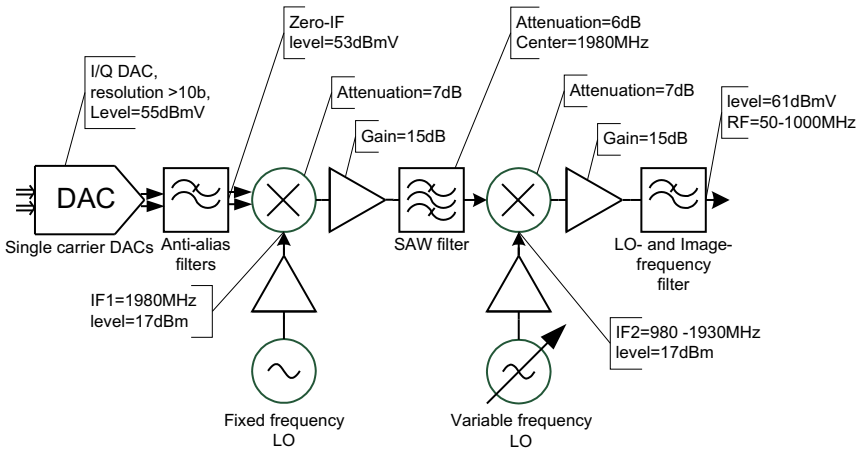


Figure 4.15: Dual conversion transmitter with the signal levels and frequencies

- The interconnections between the components are lossless. Only the components themselves have losses.
- The power supplies of the different components have an efficiency of 100%.
- The feedback paths that are available in commercial systems to monitor the system (and if needed to correct or pre-distort) are neglected.

In commercially available systems a programmable pre-distortion is often available to compensate for the increased attenuation of the cables at higher frequencies. To compensate for this frequency selective attenuation the frequency response of the output is tilted. Alternatively, the signal amplification can be adjusted, depending on the selected output frequency. These compensation techniques are not taken into account in the remaining part of the chapter.

Using these assumptions the calculations will give an estimation of the power consumption in the best case.

Table 4.1 shows the system components specifications, with the gain (or loss) of the RF building blocks together with their Noise Figure (NF) and linearity (IP3). With the IP3 and NF known, the maximum SFDR of the RF building

blocks and system of the transmitter can be computed using the the following equations [40]

$$SFDR = \frac{2}{3}\left(IIP3 - Noise\ floor\right), \tag{4.15}$$

where

$$Noise\ floor = NF - 174dBm + 10\log_{10} BW. \tag{4.16}$$

For the DOCSIS transmitter the Band Width (BW) is equal to $6MHz$. With the values shown in the table the transmitter fulfills the DOCSIS transmitter specifications.

	DAC	Low pass filter 1	Mixer 1	Amplifier 1	Bandpass filter	Mixer 2	Lowpass filter 2	Amplifier 2	**Total**
Gain (dB)	0	-2	-7	15	-6	-7	-2	15	**6**
NF (dB)	3	2	7.5	4	6	7.5	2	4	**14.8**
IIP3 (dBm)			24	19		24		19	**20.1**
OIP3 (dBm)									**26.1**
Signal level									
(dBmV)	55	53	46	61	55	48	46	61	**61**
(dBm)	6.3	4.3	-2.7	12.3	6.3	-0.7	-2.7	12.3	**12.3**
Noise floor									
(dBm)	-103.2	-102.1	-98.9	-92.8	-92.7	-91.9	-91.4	-91.4	**-91.4**
SFDR									
(dB)			83.3	77.8		75.2		74.4	**74.4**

Table 4.1: Single carrier DOCSIS transmitter components specifications (Note: impedance levels are referenced to 75Ω)

4.3.1 DAC power consumption

For the DAC a clock frequency of at least $20MS/s$ is required, as given before and the required dynamic range as is given by the DOCSIS standard can be achieved by a DAC with an effective resolution of more than 10 bits. DACs that fulfill these specifications can be made using several architectures, such as switched capacitor DACs, R-2R DACs and current steering DACs. The ideal DAC does not consume more power than the signal power at the output. Since the required signal power at the output of the DAC is equal to $55dBmV$ in 75Ω, the ideal DAC has a power consumption of $4.2mW$. However, in a practical DAC, power is spent to the re-synchronization and conditioning of the digital signals. In addition, many DACs do have some binary to thermometer decoder which increases the total power consumption. DACs published in the last several years matching these specifications, consume from 10 to $25mW$. Examples of these DACs are given in [65, 66, 67, 68]

4.3.2 LC oscillator power consumption

Using the first order equations as given in Chapter 4.2.2, the power for this LC oscillator can be estimated. Given typical values for the parameters in equation 4.9 are:

$$\begin{aligned} Q &= 30 \\ C &= 6pF \\ L &= 1nH \\ R_p &= Qf_{osc}L \\ \alpha_{ol} &= 10R_pI_{tail} \end{aligned} \tag{4.17}$$

At a frequency of about $2GHz$, a tail current, I_{tail}, of $26mA$ is required to achieve an estimated phase noise of $-100dBc/Hz$ at $10kHz$ offset. With a supply voltage of $5V$ an estimated power consumption of $135mW$ is required. This simplified estimate matches with a commercially available component

such as the CVC055BE-1000-2000 [69], which has a frequency tuning range of $1000MHz$ to $2000MHz$ at a typical power consumption of $150mW$ operating at a $5V$ supply, achieving a typical phase noise of $-100dBc/Hz$ at $10kHz$.

The complete frequency synthesizer will also contain a frequency divider, phase detector and filter. Although the VCO is not the only component in a frequency synthesizer, it is the component which typically consumes most of the power of the PLL [52]. An example of such a commercially available product is the TRF3750 of TI, it consists of an Integer-N PLL Frequency Synthesizer suitable for a external VCO with a frequency up to $2.4GHz$ that has a typical power consumption of $13mA$ at a supply voltage of $3.3V$; this corresponds to $43mW$.

To isolate the output of the VCO from the remaining circuits connected to it, such as the mixer, the output is usually first buffered. The estimated power consumption of this buffer is estimated in the next section.

4.3.3 Amplifiers and buffers power consumption

The amplifier/buffer used in the signal path should be linear in order not to distort the signal too much. A class A amplifier has a good linearity at a reasonable efficiency. The efficiency of an amplifier, defined as the relation between the output power, input power and dc power, can be used to estimate the power required to amplify a signal to the desired level. The Power Added Efficiency (PAE) is defined as:

$$\eta = \frac{P_o - P_{dr}}{P_{dc}}, \tag{4.18}$$

where P_o is the output power of the signal, P_{dr} is the input signal power and P_{dc} is the dc power from the power supply.

For a class A amplifier the peak efficiency is equal to 50%. However this efficiency is only achieved when driving the amplifier with a sinusoid to its clipping levels, but in order to achieve a better linearity, amplifiers are usually not driven up to the clipping levels but a certain back-off is employed. In

addition, whereas the efficiency of power amplifiers, such as used for base-stations, are pushed to be as efficient as possible, because of the high powers that are involved, this is much less the case for low power IF amplifiers that are required in this DOCSIS transmitter. The effective efficiency, η, then becomes much lower, in the order of 5% [70].

Although passive mixers themselves do not consume power, they do attenuate the signal. The combination of the passive mixer, low pass filter and the IF filter attenuate the signal by about $7dB + 2dB + 6dB = 15dB$. To restore the signal level an amplifier with a gain of $15dB$ is required. At the input of the amplifier the signal level is $46dBmV$ @ 75Ω which corresponds to a power of $P_{dr} \approx 0.53mW$. At the output of the amplifier the signal level is $61dBmV$ @ 75Ω which corresponds to a power of $P_o \approx 16.8mW$. With an efficiency of 5% for the amplifier the power consumption becomes equal to

$$P_{dc} = \frac{P_o - P_{dr}}{\eta} = \frac{16.8mW - 0.53mW}{5\%} = 325mW. \tag{4.19}$$

The second passive mixer is again followed by an amplifier. This amplifier needs again a gain of $15dB$ to restore the signal to its original amplitude and has the same input and output levels which results in an equal power consumption.

The amplification for the LO signal to drive the mixer requires much less linearity. For the LO signal, square wave signal shapes are commonly used. Harmonics generated by the amplifier will fall, with a good frequency planning of the RF and IF signal, outside the band of interest. Therefore efficiencies of up to 70% can be achieved [70]. Since the output power of a typical VCO is equal to about $5dBm$ [69, 71], which corresponds to a power of $P_{dr} \approx 3.3mW$, the required amplification is equal to $12dB$. The output power becomes equal to $17dBm$ which corresponds to $P_o \approx 53mW$. The power consumption of the LO buffer amplifier will be

$$P_{dc} = \frac{P_o - P_{dr}}{\eta} = \frac{53mW - 3.3mW}{70\%} = 68mW. \tag{4.20}$$

4.3.4 Total power consumption

The estimated total power consumption that can be ascribed to the total system, see Table 4.2, is equal to about 1.2W. This value assumes that the interconnect between the components is lossless, and that the power supplies for individual components have an efficiency of 100%.

Component	**Count**	**Power (mW)**	**Power consumption (mW)**
DAC	2	10	20
Amplifier 1	1	325	325
Amplifier 2	1	325	325
VCO	2	150	300
PLL synthesizer	2	43	86
LO amplifiers	2	68	136
Total			1192

Table 4.2: Estimated power consumption of the single carrier DOCSIS transmitter

4.4 Conclusion

In this chapter a single carrier DOCSIS transmitter is analyzed. The direct conversion transmitter is difficult to implement, because of the stringent requirements on the tunable filter at the output of the direct conversion transmitter. The architecture that is selected is the dual conversion transmitter, with a zero-IF input. This architecture requires the least amount of digital signal processing and the requirements for the analog components are relatively moderate. For this zero-IF architecture the specifications for the individual components are derived from the system specifications as given in the DOCSIS standard. Using these component specifications, the power consumption for the components are estimated using first order equations, commercially available components and published papers. The minimum total power consumption for the single carrier transmitter is estimated to be about $1.2W$ using the power consumption of the individual components, assuming that the interconnects between the components are lossless and the power supplies are lossless.

5

Digitization of multi-carrier DOCSIS transmitter system

Digital signal processing capabilities and power consumption follows Moore's law. This leads to smaller areas of the digital circuit and also it results in considerable power savings. This increase of digital capacities enables the possibility to replace some of the signal processing traditionally done in the analog domain, by digital signal processing. The advantage of replacing analog signal processing by digital signal processing is the reduced complexity of the analog system. Analog mixers require tuning to calibrate them to the desired frequency, which is not required in the digital system. Moreover, problems like aging and temperature drift will not affect the performance of the digital system. Another advantage is the reduced size of the system. In the traditional approach, as described in the previous chapter, the size of the modulation system is rather large due to the large amount of required analog components. By moving the DAC closer to the PA the number of analog components reduces. In the ultimate case, all the processing is performed in the digital domain and a single DAC converts this digital RF signal into an analog RF signal. This enables the integration of the digital modulator and DAC into a single IC with only one analog Nyquist filter at the output, for which no calibration is required.

The traditional transmitter as given in Chapter 4 used a dual conversion architecture with Zero-IF at the first stage. This architecture requires the least amount of digital processing, because almost all the signal processing is done in the analog domain. In this section the options of reducing the amount of analog signal processing are analyzed and methods of combining multiple channels are given.

5.1 Increased digitization of a single carrier transmitter

The digital input data of the transmitter has to be converted into an analog signal. This can be done at several locations in the transmitter, see Fig. 5.1. The filter, placed between location A and B, is a high order filter to reduce the bandwidth needed by the signal. Often a matched Raised Root Cosine (RRC) filter is used for this Nyquist filter in the transmitter and the receiver.

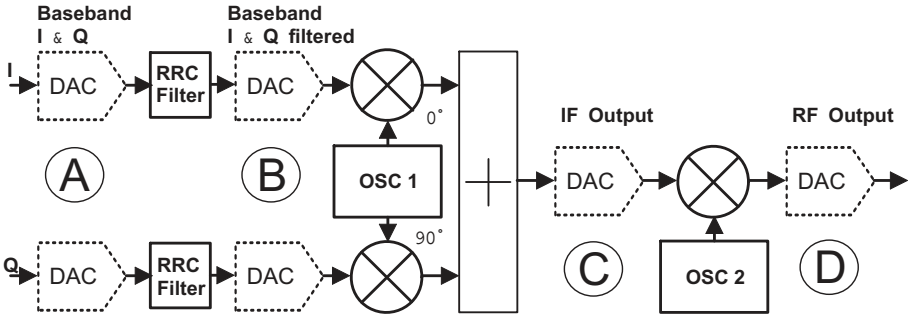


Figure 5.1: Direct conversion transmitter with several alternatives indicated for the position of the DAC

The amount of analog signal processing can be minimized by moving the DAC as far as possible to the right in Fig. 5.1. The figure shows possible locations for the DAC in a direct conversion transmitter. Although it reduces the analog processing, the required digital processing increases by doing so. The further the DAC is moved towards the output, the higher the signal frequencies become and the faster the digital signal processing has to operate. As time progresses

and newer technologies become available, the easier it becomes to perform increasing amounts of processing in digital. In this section a number of possible locations are analyzed with some of the advantages and disadvantages of each of them.

In the following sections several possible locations for this conversion from digital to analog are given with their requirements for the digital-to-analog converter, see Fig. 5.1

- (A) Before Nyquist filter (heterodyne)
- (B) After Nyquist filter before first mixer (heterodyne)
- (C) After first mixer and combiner (heterodyne)
- (D) At RF signal (homodyne)

Some of these locations are equivalent to the architectures as described in the previous chapter. When the DACs are placed at location B, the SSB/DSB/DSB architecture as described in Chapter 4.1.2 results. This architecture is commonly known as the Zero-IF dual conversion transmitter. When the DAC is placed at location C and the input frequency band is centered around 0Hz, the direct conversion transmitter results. When an additional mixing stage is added to Fig. 5.1, location C becomes equivalent to the DSB/DSB/DSB transmitter.

5.1.1 Before Nyquist filter

The first possible location is directly after the data is split into an I and Q phase, as shown in figure 5.1 denoted by A. An advantage of this location is the low conversion rate needed for the DACs. The DACs need only to convert the streams into analog values at the symbol rate, which is at relatively low speed. In addition, the dynamic range needed for the DACs is also very low. The I and Q symbols have only a few amplitude levels, which need to be converted into an analog value. In case of 64QAM, 8 amplitude levels are required i.e. a 3-bit DACs and for 256-QAM, 16 levels are required, i.e. a 4-bit

DACs. Despite these advantages there are several drawbacks at this location. One of the drawbacks is that almost all processing has to be done in the analog domain. The filtering, modulation and the combination of the I and Q phase is performed in the analog domain. The filter that is used in the transmitter is a high order filter to reduce the bandwidth needed by the signal. Often a matched Raised Root Cosine (RRC) filter is used for this Nyquist filter in the transmitter and the receiver. These filters that follow the DACs are rather complex in the analog domain due to the required steep roll-off. An example of an analog implementation of these filters with a role-off factor ($\alpha = 0.5$) can be found in [72]. However, it is difficult to generate a bandwidth efficient signal as is required by the DOCSIS standard where a steep role-off factor ($\alpha = 0.12$) is needed. These Nyquist filters are therefore almost always implemented in the digital domain, where achieving high order filters is easier.

A disadvantage of this architecture is the possible mismatch between the two DACs and mixers, which can cause I/Q phase offset, I/Q crosstalk, I/Q amplitude imbalance and I/Q timing skew errors. When these impairments become too large, the signal quality is reduced and the impairments will cause bit errors in the communication channel.

5.1.2 After Nyquist filter before first mixer

The second possible location is after the mixer before the combiner, denoted by B in Fig. 5.1. This is done in the traditional heterodyne Zero-IF transmitter, described in Chapter 4.1.2.

Except for the Nyquist filter all the signal processing is performed in the analog domain. By shifting these Nyquist filters from the analog to the digital domain, the requirements for the DACs increase somewhat, as was described in the previous chapter. The sample rate is at least $20MS/s$ and the resolution of the DAC must be 10-bit. Similar to the previous architecture has this architecture as disadvantage that the possible mismatch between the two DACs and mixers, can cause I/Q phase offset, I/Q crosstalk, I/Q amplitude imbalance and I/Q timing skew errors. When these impairments become too large, the signal quality is reduced and the impairments will cause bit errors in

the communication channel.

5.1.3 After first mixer and combiner

The third possible location is after the combiner, denoted by C in figure 5.1. This excludes the option for a Zero-IF transmitter[1]. Therefore this architecture is usually called a low-IF transmitter. At this location only a single DAC is needed, but the DAC requires a higher conversion rate and a somewhat higher dynamic range than in the Zero-IF case. As was described in the previous chapter, for a low-IF signal band around $44MHz$, a sample rate of $320MS/s$ is needed when a low complexity analog Nyquist filter is selected.

In this architecture, the mixing and addition of the I and Q phase is done in the digital domain, therefore mismatch between I and Q channel is not present. Because of this, impairments such as I/Q phase offset, I/Q crosstalk, I/Q amplitude imbalance and I/Q timing skew errors are negligible.

Because of the increased amount of digital signal processing and the increased sample rate of the DAC, the requirement on the efficiency of the digital circuit increases. Advanced CMOS processes become therefore more advantageous.

5.1.4 At RF signal

The fourth possible location is after the mixing to the RF frequency, denoted by D in figure 5.1. In this case all the signal processing steps are done in the digital domain, including the mixing to the RF frequency. No complex mixers or other complex analog components are needed except for the DAC and its low-pass filter and possibly the amplifier to drive the cable. Compared to location A and B, the main disadvantage of this location for the DAC is the required conversion rate and dynamic range needed to convert the signal. In the remaining part of this chapter this architecture is analyzed further.

[1] If we would use two DACs and filters (I/Q), Zero-IF would be possible. The resulting architecture would be equivalent to the direct conversion transmitter as described in Chapter 4.1.1

5.2 Single-carrier 'all-digital' transmitter

As discussed, ultimately all the processing is performed in the digital domain and the signal is only converted to the analog domain at the power amplifier, i.e. a power DAC. The transmitter structure, presented in Fig. 5.2, uses all-digital signal processing to generate the QAM signal and to modulate it on a RF frequency.

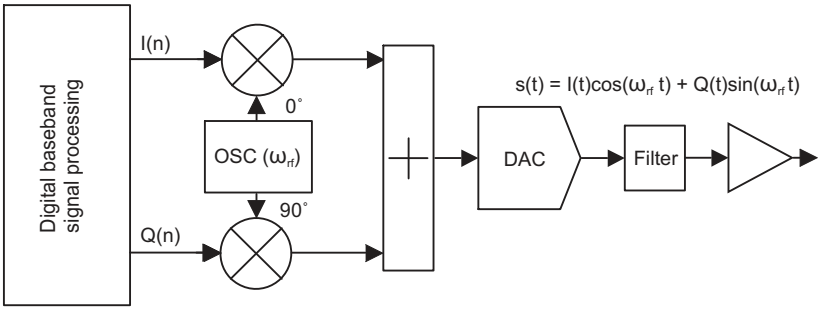


Figure 5.2: The 'All-digital' transmitter architecture.

In this transmitter structure, also the pulse shaping filters and frequency synthesizers are performed in the digital domain. The main advantages are that the modulation and addition of the I/Q path do not suffer from any kind of physical limit that is present when analog signals are multiplied and added, and that the frequency resolution of the up-conversion frequency can be selected arbitrarily, by increasing the length of the frequency tuning word at the cost of an increased digital power consumption. This allows to select the frequency of the carrier freely. In addition, analog signal processing requires tuning to calibrate to the desired frequency and to attenuate the unwanted signal components, which is not required in the digital system. Moreover, problems like aging and temperature drift will not affect the performance of the digital system. Using this architecture is also beneficial for the size of the system, because analog filters are bulky and many are needed in the traditional approach. On the other hand, the digital modulator can be integrated into a single IC with only a single analog filter at its output. This filter can be a simple low pass filter for which no calibration is required, because it is only required to suppress

the Nyquist images produced by the DAC.

The main disadvantage is the high sample rate of the signal at the last stages of this architecture, which results in high power consumption. The requirements for the DAC do also increase significantly because of this high sample rate as will be shown latter.

5.3 Multi-carrier DOCSIS transmitter

When multiple carriers have to be transmitted, in the traditional approach multiple transmitters are typically used and their RF outputs are combined. This approach gives full flexibility in the frequency planning, because each individual carrier can be modulated at any wanted RF frequency. However, this approach can be inefficient in case of a large number of carriers. Each individual carrier requires its own modulator and upconvertor. When the traditional architecture is used it would require for N parallel channels $2N$ DACs, $2N$ local oscillators, and $3N$ mixers, see Fig. 5.3. In addition, all those analog mixers require many analog components such as filters.

As the carriers are usually placed adjacent to each other in the frequency band [73], they could be combined already at the modulator. The most important change to the transmitter is that the bandwidth of the RF components must be increased in order to transmit the combination of carriers with enough signal quality. Combining several carriers in this way can make the system more efficient, since the increased signal bandwidth has a limited influence on most of the RF components involved. Components, such as the VCO/PLL are unaffected by an increased bandwidth. However, for other components, such as the amplifiers, filters and converters, this increase in bandwidth can have a big impact. For the RF amplifiers, the main difference is the increased PAPR, which was described in Chapter 2.4. The largest impact is in the digital base band and for the digital-to-analog converter. The required operation speed of the digital modulator increases proportionally to the increased bandwidth. The same applies to the sample rate and bandwidth requirements of the DAC. The number of carriers that can be combined at the modulator depends on the

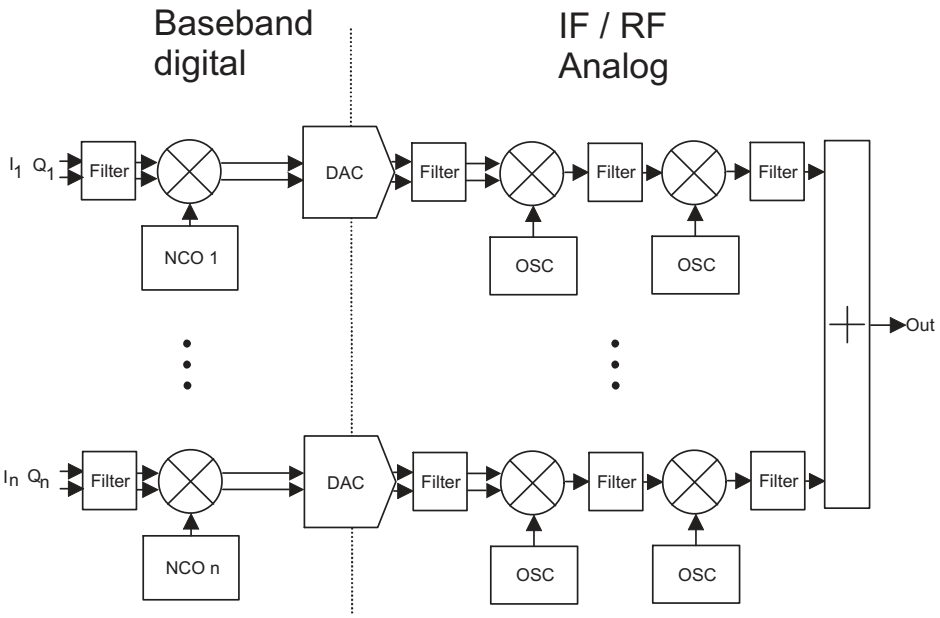


Figure 5.3: Architecture of a conventional multi-carrier transmitter

bandwidth of the RF components. In practice the limitation for the traditional transmitter is set by the SAW filter that filters the IF signal. In general, SAW filters have a trade-off between out-of-band attenuation and signal bandwidth. When the bandwidth is increased, to accommodate more channels, the attenuation of the unwanted signal components is reduced. When this attenuation becomes too low, the transmitter will not comply to the specifications set by the DOCSIS standard. The SAW filter [64], used as an example in the previous chapter, has a bandwidth of about $40MHz$, which limits the modulator to 6 consecutive channels. When more channels are required multiple modulators are needed or different architectures must be used. In the following sections these architectural options are analyzed.

5.4 Multi-carrier 'all-digital' transmitter

Although it is possible to generate N channels by using the N 'All-digital' transmitters, as shown in Fig. 5.2, in parallel, it is often preferred to increase the number of channels by changing the digital processing and convert this multi-carrier digital RF signal with a single DAC into an analog signal.

This potentially more advantageous system when many carriers have to be generated is given in Fig. 5.4. This 'all-digital' multi-carrier transmitter is based on digitally combining multiple single-carrier transmitter as is shown in Fig. 5.2. All the mixing and modulation of the carriers is done in the digital domain. Therefore, only one accurate fixed frequency clock source is required, instead of multiple independent clock sources that are tunable over a large range. Extending the system such that more carriers can be transmitted becomes easier as the main changes are in the digital domain. The limit of the number of carriers that can be combined and converted into a RF signal are constrained by the DAC, the limit on the power dissipation of the chip and the peak-to-average ratio as is given in Chapter 2.

However, since the carriers are upsampled to the sample rate of the DAC and upconverted to the final RF frequency individually, the power consumption could become significant when many carriers are combined. Because often the carriers that are being transmitted are in close proximity of each other or even adjacent, combining the individual carriers as early as possible will reduce the complexity of the system and thereby the power consumption. Less upsamplers and upconverters are required and more operations are performed at a lower sample rate. This architecture is shown in Fig. 5.5 and further discussed in the next chapter. The upsample factor $N1$ determines the available bandwidth of the combiner and thereby the number of carriers that can be combined. The final NCO translates the complete frequency band of the combiner to desired location. The relation between N, $N1$ and $N2$ is given by

$$N = N1 + N2 \tag{5.1}$$

When $N1$ is made equal to the upconversion factor N of the architecture as

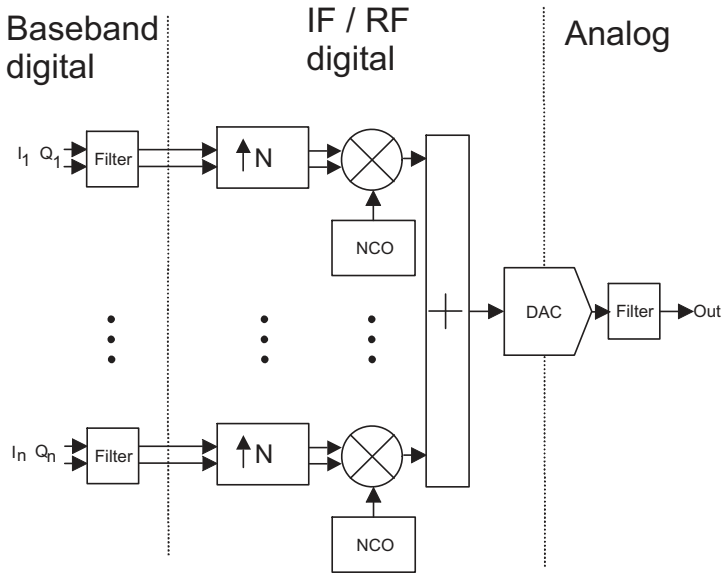


Figure 5.4: The full flexible 'all-digital' multi-carrier transmitter

given in Fig. 5.5, the upconverter $N2$ is not longer needed and the architecture is equivalent to the one in Fig. 5.4. When the upsample rate $N2$ is higher than one, it is not possible to generate carriers at any desired frequency and the band can be filled partly. To be able to fill the full Nyquist bandwidth of the DAC, multiple of these baseband digital and IF/RF digital stages are required as is shown in Fig. 5.5. The signals from these stages are then added before the DAC. In Chapter 6.4.3 the number of stages that are required for minimum power consumption will be analyzed.

The main focus of the digital implementation aspects in this thesis will be on the part noted 'IF/RF digital' in Fig. 5.5. The requirements on the baseband processing are much less demanding because of the lower sample rates involved and will not be analyzed further.

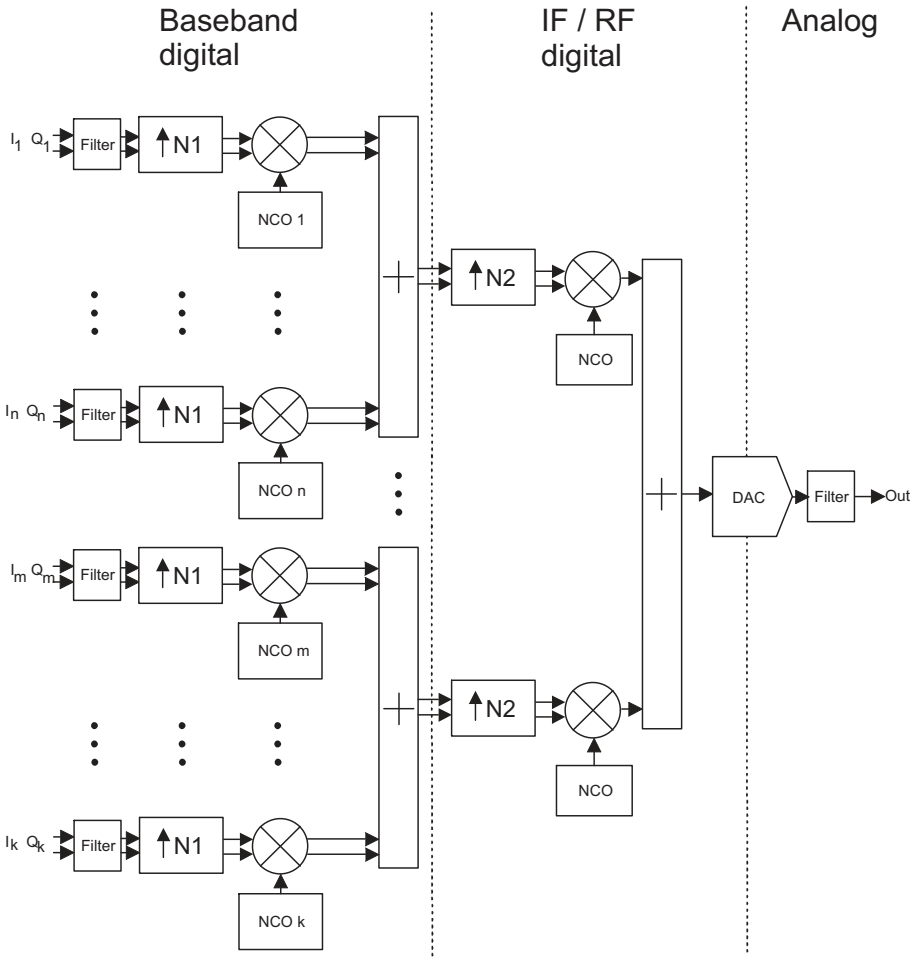


Figure 5.5: Architecture of the multi-carrier transmitter

5.5 Sample rate selection

When all carriers are directly generated at the RF frequency by the DAC, no analog upconversion stage is used. Then, the sample rate that is required for the DAC is at least twice the highest signal bandwidth according to the Nyquist theorem. For a DOCSIS 2.0 transmitter the required bandwidth is equal to 45 - 860MHz, and the band may extend from 50MHz up to 1000MHz for a

DOCSIS 3.0 transmitter [32, 3]. The minimum sample rate is therefore equal to 2GS/s.

5.5.1 Band repetition used for upconversion

There are possibilities to use a lower clock frequency of the DAC by using not the first, but the second or third Nyquist zone, see Fig. 5.6. The main advantage is that the output frequency of the signal can be above $f_s/2$. However, using these Nyquist zones has several disadvantages. Firstly, the signal in the second Nyquist zone the frequency spectrum is inverted, which must be compensated for by correcting it in the digital domain. Secondly, the output power in higher Nyquist zones decreases and close to the clock frequency f_s the signal is attenuated severely, as is shown in Fig. 5.7. Therefore the output signal can not be placed at any wanted signal frequency, because of the attenuation at those frequencies. A method to prevent this signal attenuation around the clock frequency is by using a return-to-zero (RTZ) signal at the output of the DAC. This has the disadvantage that the signal power at the output of the DAC is reduced by $6dB$.

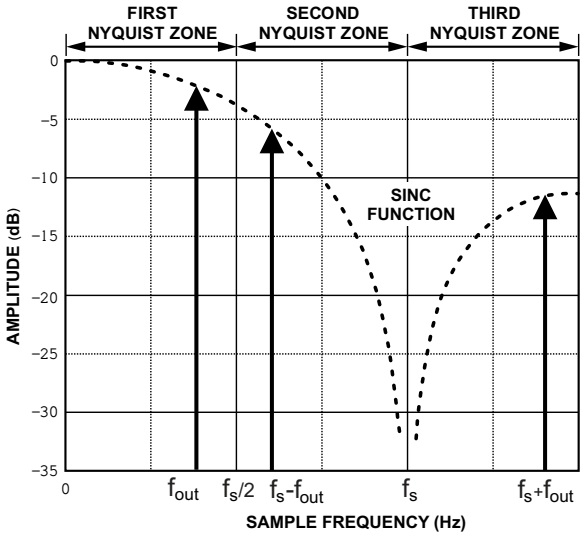


Figure 5.6: The DAC output images.

Another drawback of using Nyquist zones other than the first one is the increased complexity of the filter following the DAC. Instead of a low-pass filter that is required for the first Nyquist-zone, band-pass filters will be needed for the other zones. When for example a 1GS/s DAC would be used to generate a channel at $750MHz$, which is in the middle of the second Nyquist zone, then the image in the first Nyquist zone is located at a frequency of $250MHz$. This signal must be attenuated to a level of $73dB$ below the wanted signal according to the DOCSIS standard, see Chapter 3. Due to the additional sinc attenuation of the wanted signal at $750MHz$ compared to its image at $250MHz$, which is equal to $9dB$, the total attenuation required becomes at least $82dB$, which results in a 9th order Butterworth filter, as will be shown in the following section. Selecting RTZ at the DAC output reduces the required filter to order 8. However, when the output frequency is changed to $600MHz$ the required filter order increases to 24, because of the closer proximity of the image. This high order is difficult to realize with an analog filter. Consequently, using this architecture, signal frequencies between $350MHz$ and $650MHz$ are hard to achieve, when the mask requirements are taken into account. For these reasons the signal should be located in the first Nyquist zone when a flexible system is required that can change its output frequency to anywhere within the band.

5.5.2 Sample rate vs analog low-pass filtering

The DOCSIS specification specifies a superior emission limit of $-55dBc$ for frequencies above $1000MHz$ [3]. The low-pass filter at the output of the DAC should suppress the images enough to keep them below this limit. As the DAC output frequency approaches $f_s/2$, so does the first image frequency in the second Nyquist zone. As a result the required transition bandwidth of the filter decreases. The first image frequency is located at $f_{image} = f_s - f_{out}$, with the signal located at f_{out}. The transition bandwidth of the filter is equal to $f_{tran} = f_s - 2f_{out}$, so a trade-off between the sample rate of the DAC and the required order of the filter exists.

To filter these images, many types of filter characteristics can be selected for the low-pass filter at the output of the DAC [21]. The three most popular filter characteristics are the Bessel, Chebyshev and Butterworth. The Bessel

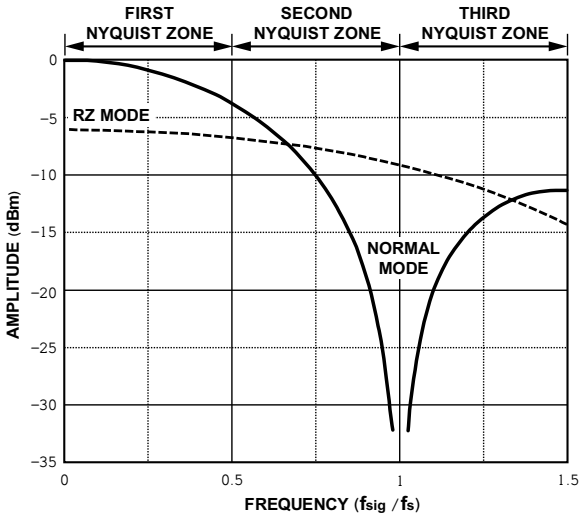


Figure 5.7: The attenuation of the signal caused by the zero-order-hold at the output of the DAC

filter is optimized to obtain better transient response due to a linear phase in the pass-band. The frequency response is however, relatively poor, i.e. a high order filter is required to obtain a good attenuation in the stop-band. The Chebyshev filter is optimized for attenuation in the stop-band, however, this filter has the penalty of amplitude variation in the pass-band and poor phase response. The Butterworth filter is the best compromise between attenuation and phase response [21]. It has no ripple in the pass-band or stop-band. The Butterworth filter achieves it flatness at the expense of a relative wide transition region.

The Butterworth filter order that is required to obtain a given suppression and transition bandwidth is given by the following equation [22]

$$O_{Butterworth} = \left\lceil \frac{\log_{10} \frac{10^{Attn/10}-1}{10^{3.01/10}-1}}{20 \log_{10} \left(\frac{f_s - f_{out}}{f_{out}} \right)} \right\rceil . \tag{5.2}$$

Since the DAC implicitly uses zero order hold function, its output is already filtered by the sinc response. The attenuation of higher frequencies caused by

the sinc response is shown in Fig. 5.7. The closer f_{out} is to the sample frequency, the higher the attenuation becomes. At frequency $f_s/2$ the attenuation is equal to 3.95 dB. A method to reduce the droop in the frequency band is to use Return-to-Zero (RZ). Then, the droop at half the sampling frequency is only $0.9dB$; however, the signals amplitude is reduced by a factor of two, i.e. $6dB$, see Fig. 5.7. This additional loss commonly needs to be amplified in the system to to restore the signal level. Therefore, a Non-Return-to-Zero (NRZ) DAC is selected. To prevent distortion of the signal by this sinc filtering, it has to be compensated by an inverse sinc filter. This filter amplifies the higher signal components such that the DACs output spectrum has a flat frequency response. The sinc frequency response in the second Nyquist zone is helping to reduce the image signal components. The lower the signal frequency, the more the images are attenuated and at the same time the filter transition band increases. This reduces the order of the filter that is needed.

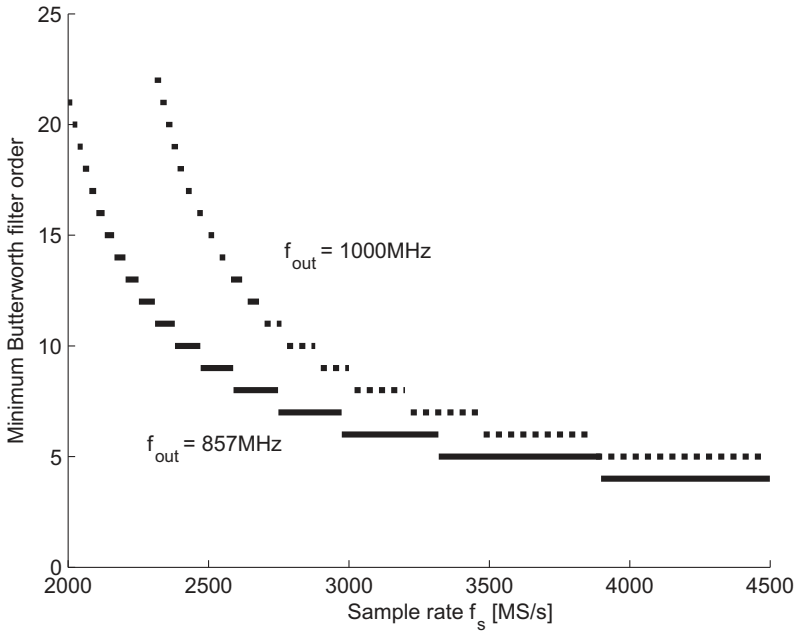


Figure 5.8: The minimum low-pass Butterworth filter order at output of the DAC to filter the image frequencies

Fig. 5.8 depicts the required filter order as a function of the sample rate of the DAC. It shows that the lower the sample rate, the higher the required filter order. However, these high order filters at those frequencies are difficult to manufacture. Increasing the sample rate does increase the complexity and power consumption of the system, but decreases the complexity of the analog filters. For a maximum signal frequency of $860MHz$ and a sample frequency above $2400MS/s$ the filter order becomes lower than 9, which is feasible with a moderate complexity [74], at an acceptable power consumption in the system.

5.5.3 Sample rate vs symbol rate

As discussed, for the DAC a clock frequency of more than $2400MS/s$ is required. In a US DOCSIS transmission system every channel has a symbol rate f_d of $5.36MS/s$. The sample rate of each channel has to be increased from the symbol rate to the DAC clock frequency f_s, which is about 450x f_d. It is advantageous that the upsample factor can be factorized in small prime numbers, as will be shown in Chapter 6.2.3. The upsample ratio preferably has only factors of two. The nearest number which is a power of two is 512, i.e. 2^9, which results in a sample rate of $f_s = 2744.6MS/s$. Other numbers that have many low prime number factors are 448, i.e. $2^6 \times 7$, which results in a sample rate of $f_s = 2401.5MS/s$, and 480, i.e. $2^5 \times 3 \times 5$, which gives a sample rate of $f_s = 2573.1MS/s$. For the system a sample rate of $f_s = 2744.6MS/s$ is selected as target.

5.6 Digital logic

Digital logic families come in many different styles [75]. The first basic split can be made among static logic and dynamic logic. *Static logic* is a logic form in which the function of the circuit is not synchronized by a global signal. The output is solely a function of the input of the circuit and it is asynchronous with respect to the inputs. The timing of the circuit is defined exclusively by its internal delay. *Dynamic logic* is a logic in which the output is synchronized by a global signal, namely the clock. The output is then a function of both the

input of the circuit and of the clock signal. The timing of the circuit is defined by both its internal delay and by the timing of the clock.

Examples of static logic families are conventional CMOS static logic and Current Mode Logic. Examples of dynamic logic are Domino logic, No Race (NORA) logic and True Single Phase Clock Logic (TSPC) [76]. These dynamic logics commonly have the advantage that they only use NMOS transistors at the input, which reduces the input capacitance and transistor count, compared to conventional CMOS logic. However, these types of logic have also several disadvantages. One of the disadvantages is the sensitivity to noise on its inputs. In addition, commonly these dynamic logic styles have a higher switching activity compared to, for example CMOS logic. The output node of the Domino logic gates, for example, are pre-charged every clock cycle, which results in a large dynamic power and, hence, EMI [76]. Since interference to the analog DAC and its output should be prevented, these dynamic logic styles will not be analyzed further. In the next sections conventional static CMOS logic and Current Mode Logic (CML) are analyzed in more detail.

As will be shown later in Chapter 6.3, two implementations of the 'all-digital' transmitter will be made. The first implementation will use CML logic for the DSP core to prevent interference from the digital circuits as much as possible while the second implementation will use a conventional static CMOS implementation for the DSP core. In this version various circuit and architecture techniques are implemented to reduce the interference.

5.6.1 Conventional static CMOS logic implementation aspects

Conventional static CMOS logic is a style of logic circuit. It uses a combination of n-type and p-type transistors to implement the logic gates and other digital circuits. In the CMOS logic circuit, the output is always connected to either a V_{DD} or a V_{SS} through a low ohmic path. To accomplish this, the paths that connect to the V_{DD} must complement the paths that connect the output to the V_{SS}.

CMOS logic is quite fast, it does not dissipate power in the standby state except for some leakage power, and it has a good noise margin. The power is only consumed when a node changes state and its load capacitance has to be charged/discharged from the supplies[2].

These properties make CMOS logic very attractive for the implementation of digital circuits, especially circuits that are operating at low frequencies.

For the CMOS implementation standard cell library CMOS logic circuits are used. The digital circuit is synthesized from a high level description language VHDL. Therefore the implementation aspects of the CMOS logic circuits will not be examined in more detail.

5.6.2 Current mode logic implementation aspects

In general, logic circuits must satisfy the constraints assigned to them in terms of speed, power consumption and silicon area. Moreover, additional requirements on the switching noise and interference must be taken into account in the design process of mixed-signal ICs, which consist of both analog and digital circuitry sharing the same substrate.

The static CMOS logic style, as described before, has an appealing speed, performance, static power consumption, area and noise margin. However, it also generates a considerable amount of switching noise due to current spikes at the transition moments. These current spikes cause voltage drops across the parasitic resistors and inductors of the power supply network and bondwires. These voltage fluctuations are partly coupled into the substrate or other paths and can couple through it to the sensitive analog circuits.

Many methods have been proposed to reduce the performance reduction caused by the switching noise. These methods can be categorized to have an effect on one ore more of the following three points: the source, the path, and the receiver.

[2]Power is only drawn from the V_{DD} when the transition is from L to H. However, since static CMOS is an inverting logic style a transition from H to L on a gates output is triggered by a L to H transition of one of its inputs or an internal node of the gate.

To reduce the coupling between the source and the receiver, the path can be made more high ohmic by using a Silicon-on-Insulator (SOI) technique or using a highly doped epitaxial CMOS waver at an increased cost. In most advanced technologies, CMOS 90nm and beyond, the wafers are made high-ohmic. Another method of decreasing the coupling is by optimizing the floorplan and increasing the distance between the source and the receiver. Often this will increase the cost, because of the larger die size that is required. The effects of the switching noise can be mitigated by reducing the common impedance of the paths from the supply to the analog and digital blocks. By using separate bonding pads, bonding wires, and pins, the common impedance can be reduced. An additional reduction can be achieved by placing multiple pads and bondwires to reduce their parasitic inductance at the cost of additional supply pads and area.

The receiver can be made more immune to noise originating from the power supply and substrate by exploiting differential topologies, since they are intrinsically more immune to common mode external interference and have a high Power Supply Rejection Ratio (PSRR) .

For high performance circuits the above remedies could be insufficient to reach the desired performance levels. A solution is to reduce the source of the interference by replacing the static CMOS logic by alternative logic styles [77, 78, 79]. The switching interference can be mitigated by reducing the supply current variation. A logic style that has a nearly constant supply current is CML logic.

CML gates are based on source coupled pairs of NMOS transistors, see Fig. 5.9. These NMOS networks are biased by a constant current, I_{ss}, which is commonly implemented as an NMOS current source. At the drain of the NMOS pairs resistances are connected to the positive power supply rail. These resistances can be implemented as physical resistors or as transistors that are biased in the linear region.

To implement a two-input AND/OR/NAND/NOR gate, the network as shown in Fig. 5.10 can be used. Current $I_{a,b}$ is only approximately equal to I_{ss} when transistors Q_1 and Q_3 are on, which occurs if $A = 1$ and $B = 1$. This current is then converted into a voltage by a resistor R. The current through the inverting

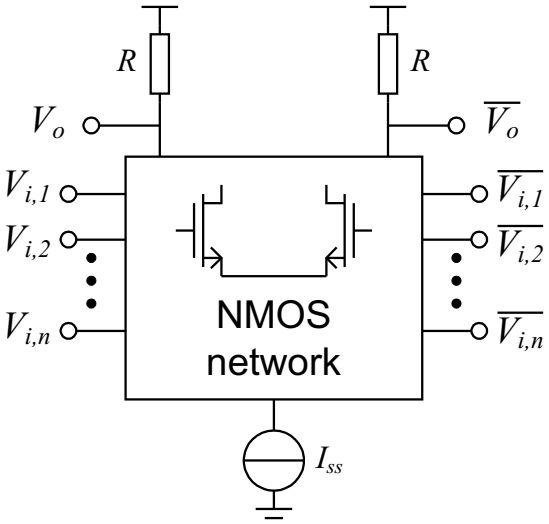


Figure 5.9: A two-input AND/OR/NAND/NOR CML gate network

output terminal is almost equal to zero, the output voltage is therefore close to the V_{DD}. The logic operation given the names in the figure results in a NAND gate. By exchanging the output terminals, through De Morgan laws, the gate can be used as an AND gate. By exchanging the positive and negative output as well as the positive and negative input terminals, the OR gate can be made, etc.

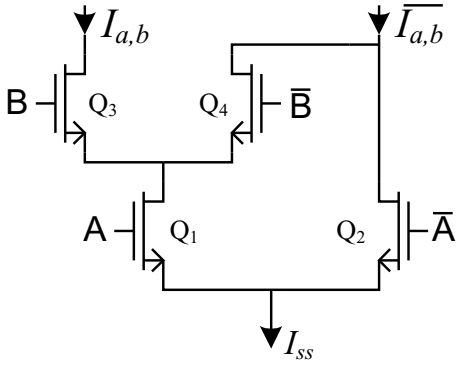
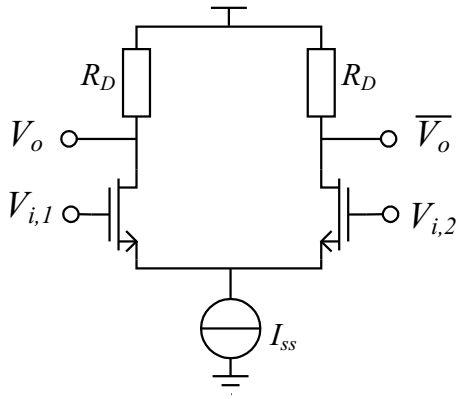
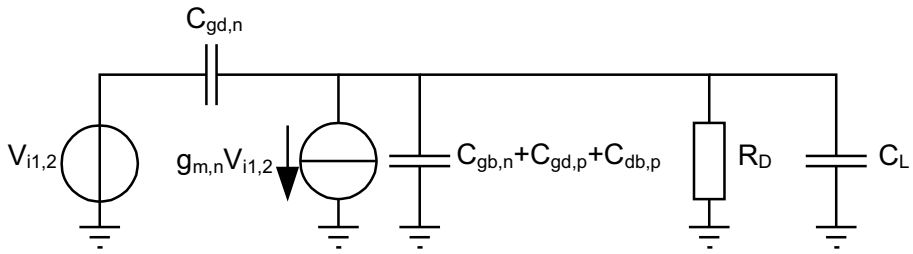


Figure 5.10: The general topology of a CML gate

In the design of CML gates many degrees of freedom exist in the selection of the parameters. For conventional CMOS logic only two parameters exist, the transistor sizes[3] and the power supply voltage, which can be selected independently from each other. The power supply voltage is commonly defined by the technology that is used, only when the power consumption is critical the supply voltage is sometimes reduced. In the case of CML gates many degrees of freedom exist. The parameters that can be tuned, such as the transistor sizes, currents and supplies are dependent on each other, which gives a complex optimization problem [80].



(a) The CML inverter



(b) The equivalent linear circuit of a CML inverter

To reach high speed the switches of the CML stage operate in the saturation region most of the time. The source voltage of both switch transistors are equal to each other, since this voltage is determined by the switch transistor that is in the on-state and draws the current I_{ss}, see Fig. 5.11(a). Because the circuit

[3]When the logic transition level is given, commonly vdd/2, the ratio between the NMOS and PMOS transistor size are defined by the process parameters.

is symmetric it can be simplified by applying the half circuit concept [81]: the circuit is linearized around the bias point $V_{diff_{in}} = 0$. The equivalent linear circuit of the CML inverter gate is given in Fig. 5.11(b), where C_{gd} is the gate drain overlap capacitance, C_{db} is the drain bulk capacitance and C_{load} is the loading capacitance. By assuming a unit step at the input of the gate the propagation delay is given as

$$\begin{aligned} \tau_{PD} &= 0.69 R_D \left(C_{gd} + C_{db} + C_L\right) \\ &= 0.69 \frac{\Delta V}{2 I_{ss}} \left(C_{gd} + C_{db} + C_L\right) \end{aligned} \tag{5.3}$$

where ΔV is the differential voltage between the two output nodes. To reduce the propagation delay given a certain load capacitance, I_{ss} can be increased or ΔV can be reduced. Reducing ΔV decreases the robustness of the circuit against interference and power supply fluctuations.

For the circuit to operate properly, ΔV must be within certain boundaries, ΔV_{min} to ΔV_{max}. The noise margin of the CML gate is estimated as [81]

$$NM = \frac{\Delta V}{2} \left(1 - \frac{\sqrt{2}}{A_v}\right). \tag{5.4}$$

where A_v is the gain of the differential pair. By rearranging this relationship for ΔV, the minimum ΔV_{min} can be estimated

$$\Delta V_{min} = \frac{2NM}{\left(1 - \frac{\sqrt{2}}{A_v}\right)}. \tag{5.5}$$

For ΔV_{max} the swing $R_D I_{ss}$ on each of its outputs must be low enough to ensure the switch transistors to be kept out of the linear region. When the switches enter the linear region the driving capabilities of the gate are reduced. In addition, the capacitance seen on the input of the gate increases, thereby increasing the load in the driving gate as well [81]. To avoid the switching

transistor to enter the linear region its gate-drain voltage must comply to the following condition

$$V_{gd} = V_{DD} - (V_{DD} - R_D I_{ss}) = R_D I_{ss} \leq V_{t,n}. \tag{5.6}$$

This gives the upper bound for ΔV as

$$\Delta V_{max} = 2V_{t,n}. \tag{5.7}$$

For an optimal design, the A_v of the CML gate should be designed to have a value of around 4 [81]. ΔV should be between ΔV_{min} and ΔV_{max}. In case power consumption of the gate is of concern, the logic swing should be set equal to ΔV_{min}, while for high speed operation the swing has to be set to ΔV_{max}.

The power, power-delay, and energy-delay for static CML logic are approximated by [82]:

$$\begin{aligned} P_{CML} &= I_{ss} V_{DD} \\ PD_{CML} &= C \Delta V V_{DD} \\ ED_{CML} &= \frac{C^2 V_{DD}^2 \Delta V^2}{I_{ss}} \end{aligned} \tag{5.8}$$

where C is the load capacitance of the gate, V_{DD} is the supply voltage, I_{ss} is the tail current of the gate and ΔV is the voltage swing at the output of the gate. One interesting property to note is that CML circuits do not have a theoretical minimum to the energy-delay product whereas the CMOS circuits do [82]. A designer can arbitrarily reduce the ED product by increasing the current for a given C, V_{DD}, and voltage swing. In practice, this is not possible for very large currents because the robustness of the circuitry will deteriorate [80].

5.6.3 Technology scaling of conventional static CMOS logic

While for analog circuits technology scaling hardly brings any power savings, and in some cases the power could even increase by using a more advanced technology, because of the reduced voltage headroom in advanced processes, for CMOS digital circuits the power decrease is substantial [83]. Digital signal processing capabilities and power consumption follow Moore's law. This leads to smaller areas of the digital circuit and results in considerable power savings.

Scaled Parameter	Ideal Scaling factor
Feature sizes: W, L, T_{ox}	S
Substrate doping	$1/S$
Voltages: V_{DD}, V_t	S
$\mathbf{Id_{sat}}$	S
$\mathbf{C_{gate}}$	S
$\mathbf{R_{on}} \propto V_{DD}/Id_{sat}$	1
$\boldsymbol{\tau} \propto CV_{DD}/I$	S
Power $\propto CV_{DD}^2 f$	S^2
Area/Device	S^2
Power/Area	1

Table 5.1: Ideal technology scaling conventional CMOS

Porting a digital circuit from one technology to the next one reduces the total capacitance, which is the dominant cause of the power consumption in active circuits, by a factor S, with S being the technology scaling factor [83]. The ideal scaling of the process parameters and its effect on the power, area and speed are given in Table 5.1. Hence the power consumption scales by S^2 and the area scales by S^2.

Until CMOS090 the supply scaling was keeping pace with the technology scaling and from one technology to the next generation the scaling factor was about 0.7. Porting the same circuit from one technology to the next resulted in a power saving of about 65%.

From CMOS090 and beyond the power supply voltage hardly scales with the minimum feature size anymore. The supply voltage of a CMOS090 process is 1.2V and for CMOS045 it is $1.0V$ which corresponds to a factor of $S_{supply} \approx 0.8$,

while the technology minimum features scaled down by more than two times in size.

Technology	**0.25μm**	**0.18μm**	**0.13μm**	**90nm**	**65nm**	**45nm**
$\mathbf{L_{drawn}}$ [μ**m**]	0.25	0.18	0.13	0.1	0.06	0.04
$\mathbf{L_{eff}}$ [μ**m**]	0.16	0.1	0.07	0.05	0.035	0.025
$\mathbf{V_{DD}}$ [**V**]	2.5	1.8	1.5	1.2	1.1	1
$\mathbf{V_t}$ [**V**]	0.65	0.45	0.375	0.3	0.225	0.2
$\mathbf{T_{oxide}}$ [**Å**]	50	40	30	25	20	15
$\mathbf{C_{jo}}$ [$\mathbf{e^{-3}F/m^2}$]	1.08	1.35	1.69	2.11	2.64	3.30
$\mathbf{C_{jsw}}$ [$\mathbf{e^{-10}F/m}$]	3.75	4.69	5.86	7.23	9.16	1.15
Metal pitch [μ**m**]	0.65	0.5	0.37	0.28	0.21	0.15
Metal thickness [μ**m**]	0.5	0.46	0.34	0.26	0.2	0.14
Dielectric thickness [μ**m**]	0.65	0.5	0.36	0.32	0.27	0.21
Dielectric $\varepsilon_\mathbf{r}$	4	3.3	2.7	2.3	2	1.7

Table 5.2: Key characteristics of several technology nodes [6]

With the supply voltage scaled by S_{supply}, the gate-oxide thickness scales by S_{supply}. The power consumption of the scaled circuit at a constant frequency thus becomes

$$P_{dig} \rightarrow P_{dig} \cdot S \cdot S_{supply}^2. \tag{5.9}$$

Table 5.2 shows the smallest feature size of the technology and its supply voltage. Using this table it can be calculated that scaling from CMOS065 to CMOS045 results in a power reduction of about 40%. A according to the ITRS roadmap [6] the supply voltage scaling will slow down from one technology to the next. In addition, the metal back-end of the processes does not scale down as fast as the minimum transistor sizes. Therefore, the load capacitance seen will scale less than S, which reduces the power consumption advantage even more [83].

5.6.4 Technology scaling of CML

The ideal scaling of the technology for CML can be analyzed in a similar method as for static CMOS logic. For high speed operation the ΔV of the gate is often selected to be close to two times the threshold voltage. Because CML circuits do not have a minimum propagation delay, τ_{pd}, as increasing I_{ss} given a certain load capacitance will decrease the delay at the cost of increased power consumption, the scaling properties can only be analyzed assuming a parameter to be constant, such as I_{ss}, τ_{pd} or ΔV. When the circuit after the process scaling has to operate at the same clock frequency, the τ_{pd} is assumed to be constant. In that case the ideal scaling results are given in Table 5.3. It is always possible to exchange a part of this power reduction for a smaller τ_{pd} in order to achieve higher operation speeds.

Scaled Parameter	**Ideal Scaling factor**
Feature sizes: W, L, T_{ox}	S
Voltages: V_{DD}, V_t	S
$\mathbf{C_{gate}}$	S
$\boldsymbol{\tau_{pd}}$	1
$\mathbf{\Delta V} \propto V_t$	S
$\mathbf{I_{ss}}$	S
Power $\propto I_{ss}V_{DD}$	S^2

Table 5.3: Technology scaling for CML logic for constant τ_{pd} ("ideal")

5.7 Conclusions

In this chapter the digital signal processing of the 'All-digital' DOCSIS transmitter is analyzed. The main advantage of using this architecture is the reduced number of analog components, thereby exploiting the advantages of the scaling properties of digital circuits in advanced CMOS technologies. In addition, the number of carriers that can be transmitted using a single 'All-digital' transmitter is significantly larger, compared to the traditional transmitter. Although it is possible to convert each carrier from baseband to RF individually, it is more economic to combine the carriers as soon as possible and then upsample the group of carriers and mix them to the desired frequency.

The sample rate that is required to cover the full DOCSIS bandwidth of almost $1000MHz$ is mainly determined by the low-pass filter that suppresses the images that are created by the DAC to an acceptable level.

While for analog circuits technology scaling hardly brings any power savings, and in some cases the power could even increase, by using a more advanced technology, because of the reduced voltage headroom in advanced processes, for CMOS and CML digital circuits the power decrease is substantial.

6

All-digital multi-carrier single-DAC transmitter

In this chapter the requirements of the digital signal processing of the 'All-digital' multi-carrier single-DAC transmitter are analyzed the implementation aspects are studied.

In the previous chapter the concept of the 'All-digital' transmitter was introduced together with the required sample rate. It was shown that the increased digitalization was beneficial for the power consumption of the digital circuits, when the transmitter is implemented in an advanced CMOS process. Furthermore, the reduction of the analog circuits reduces the need for tuning.

In this chapter the architecture that is used to prove the concept of the 'All-digital' transmitter is given. The architecture is broken up into its subfunctions. Using the DOCSIS specifications the requirements for these subfunctions are set. Given these requirements, the subfunctions are analyzed and the complexity and power consumption of several alternative architectures are compared. For each subfunction the best alternative is then selected for the implementation.

6.1 Single DAC transmitter architecture

To prove the concept of the DOCSIS transmitter, the architecture that is proposed in Fig. 5.5 could be implemented. Using this architecture it would be possible to fill the complete DOCSIS band that ranges from $50MHz$ to $1000MHz$. However, to implement this architecture many input pins would be required to supply the data to the transmitter, thereby creating a large and complex transmitter IC that would require specialized equipment to generate the data. Since the main challenge is in the DAC and the digital circuits that have to operate at high frequencies and not in the generation of the data that has to be broadcasted, the architecture as shown in Fig. 6.1 will be implemented. The difference between this architecture and the architecture shown in Fig. 5.5 is the reduced maximum bandwidth, because only a single digital IF stage is implemented. Therefore, the number of input pins that are required is reduced by a factor two or more. As will be shown later the implemented architecture has a bandwidth that is limited to $420MHz$, instead of the $950MHz$ that is used by the DOCSIS standard. Although the bandwidth does not cover the complete DOCSIS bandwidth, the bandwidth which is covered by this 'All-digital' transmitter is large enough to prove the validity of this concept.

6.2 Components options and selections

In this section the components that are required to implement the Digital Signal Processing (DSP) for the multi-carrier 'All-digital' transmitter transmitter are studied. The requirements and implementation aspects, such as complexity and power consumption, of these components are analyzed.

6.2.1 Clock source

For the clock of the 'All-digital' transmitter a single clock source is required, compared to the many clock sources required for the conventional multi-carrier transmitter, since all the frequency division is done in the digital domain. The

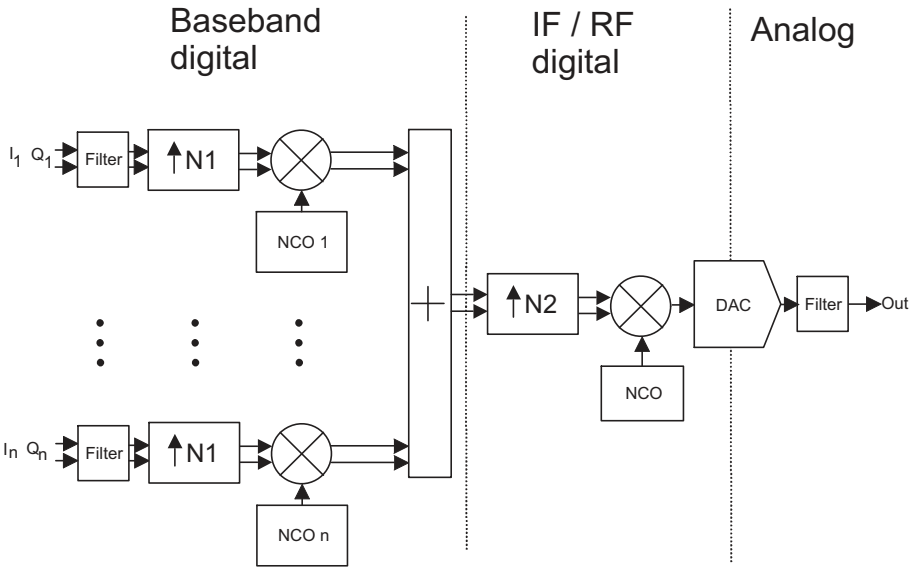


Figure 6.1: Architecture of the proposed multi-carrier transmitter

requirements for the quality of this clock can be derived from the DOCSIS specifications. The quality of the local oscillator is usually defined by its phase noise, as given in Chapter 4.2.2. It should be low enough not to distort the information in the signal that is modulated. Compared to the conventional transmitter, the requirements for the 'All-digital' transmitter are different. While for the conventional transmitter the tuning range of the local oscillator was large, the 'All-digital' transmitter has a fixed frequency. This eases the design of the oscillator. The highest frequency of the LO is somewhat higher for the 'All-digital' transmitter compared to the conventional transmitter, viz. $2.745GHz$ vs. $1.930GHz$.

The maximum allowed phase noise for the 'All-digital' transmitter system can be calculated by assuming that the phase noise of the clock source follows Leeson's model, see Chapter 4.2.2, and assuming that the signal output frequency is lower than the clock frequency of the DAC. The carrier frequency on which the signal is modulated can be described as a frequency divider. Therefore the output frequency, f_{out}, of the DAC and the clock frequency, f_{clk}, have the

approximately following relation [84]

$$\left(\frac{f_{out}}{f_{clk}}\right)_{dB} \simeq -20\log_{10} N \tag{6.1}$$

where N is the ratio of the output frequency and the clock frequency. Assuming a clock frequency of $2744MS/s$ and a highest output frequency of $1000MHz$, $N = 2.744 \simeq 8.8dB$. As the phase noise of the transmitter at the signal frequency must be better than $-95dBc/Hz$ at $10kHz$ offset as calculated in Chapter 4.2.2, the required phase noise of the clock source must be better than $-86dBc/Hz$ at $10kHz$ offset. This is about the same level as commercial DOCSIS receivers require for their oscillator [51, 36, 38].

6.2.2 Data rate converter

An important function of the digital circuit is the upsampling of the data that has to be transmitted. In applications, such as digital radios, cell phones, base stations, etc., upsampling is often used to simplify the design of the analog filters, because of the larger transition band. The up- and down sampler components are important building blocks. The principle of upsampling is shown in Fig. 6.2 and Fig. 6.3. As a first step, the incoming data is (theoretically) interpolated with zeros. The number of zeros that are being inserted in between contiguous samples is $N - 1$ where N is the upsample ratio. The spectrum of this new interpolated signal is shown in Fig. 6.5. To remove the unwanted replicas in the spectrum the signal is filtered.

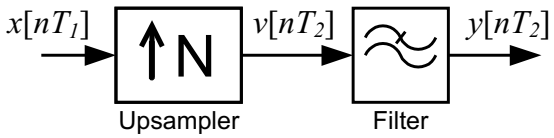


Figure 6.2: The principle schematic of the upsampling.

The complexity of the upsampling is almost completely determined by the filtering that is required, especially when the ratio between the input sample rate and output sample rate becomes large.

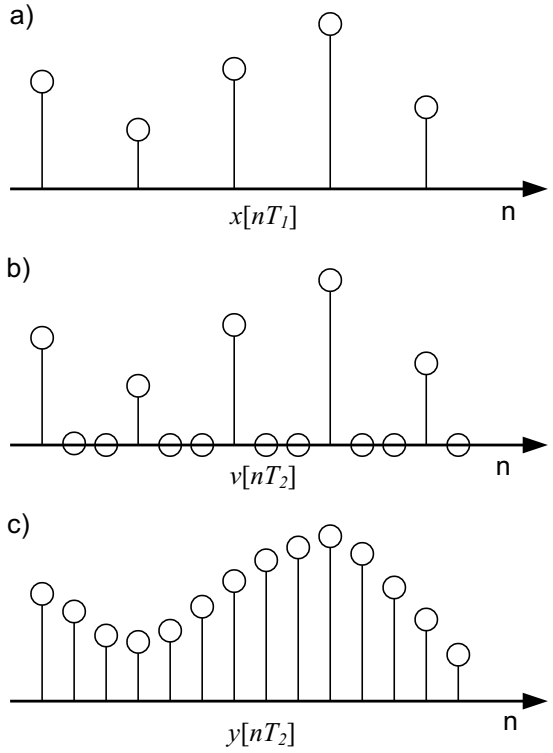


Figure 6.3: The time domain signals at various stages of the upsampler. a. the input signal, b. the interpolated input signal, c. the filtered signal.

In the DOCSIS system, every channel has a symbol rate of $5.36MS/s$. The sample rate of the DAC is set at $f_s = 2744.6MS/s$, see Chapter 5.5. The total upsample rate is equal to 512. Theoretically it would be possible to implement this upsample ratio in one stage. However, this would result in a inefficient implementation [85]. When an upsample filter with a large non-prime upsample factor has to be realized, it is often much more efficient to design a cascade connection of a number of interpolating filters, each with a lower interpolation factor [85]. The total number of multiplications per second that is needed and the amount of coefficients that has to be calculated will be smaller.

6.2.3 Upsample filters

The principle of the upsampling and the filtering that follows it is shown in Fig 6.4. Fig. 6.4a, shows the frequency spectrum of the original input signal. Fig 6.4b shows the frequency spectrum immediately after the upsampler; the signal contains images of the original signal at multiples of $\frac{f_s}{R}$, where N is the upsample ratio and F_{s2} is the new sample frequency. The purpose of the filter is to remove the images added by the upsampler, as shown if Fig 6.4c.

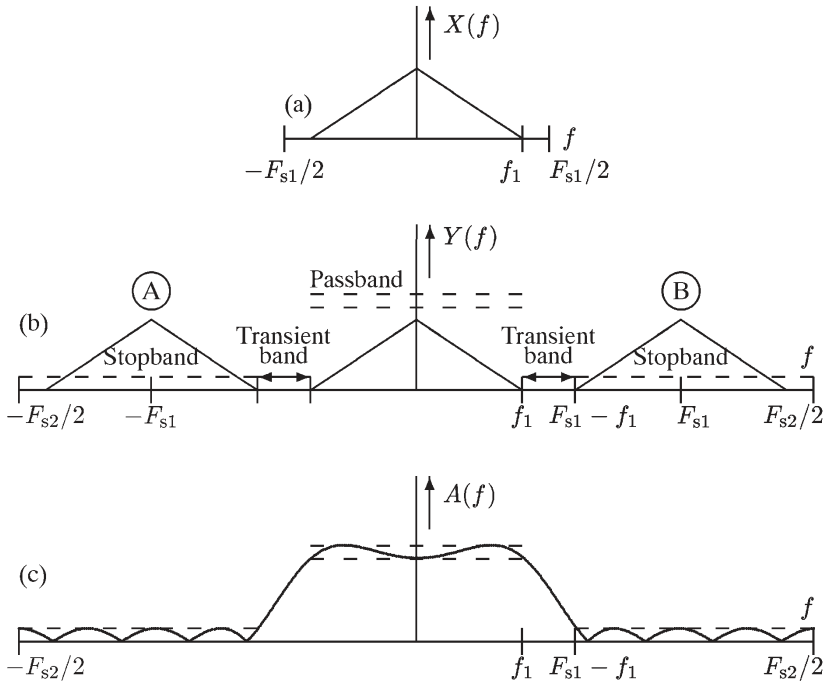


Figure 6.4: Increasing the sample rate by a factor three: a. the original signal, b. the interpolated signal, c. the filter characteristic that suppresses the images.

Filter characteristic

A number of the characteristics of filters are shown in Fig. 6.5.

The *Stop-band suppression* defines the amount of suppression of the unwanted

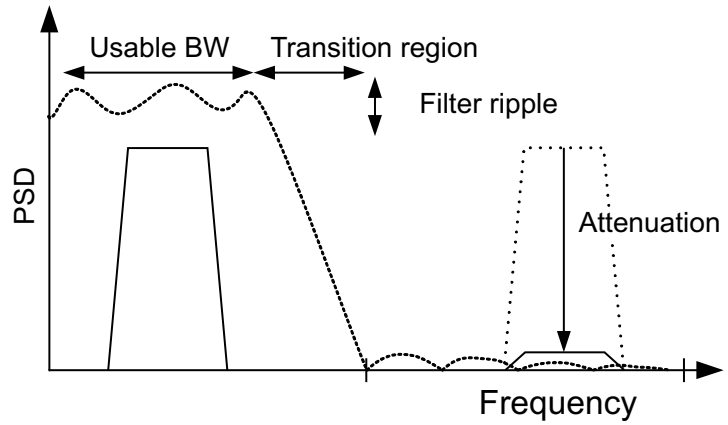


Figure 6.5: Upsample filter specifications

replicas. The suppression should be better than the out-of-band spectral mask requirements. The allowed *pass-band ripple* of the filter is defined by the total ripple of all the interpolation filters. The *transition bandwidth* should be less than $\Delta f = f_s - 2BW$, as the first replica that has to be suppressed is located at $f_s - BW$, where BW is the bandwidth of the input signal and f_s is the sample rate.

Stopband suppression Ideally the filter should remove all the unwanted signal components. But a practical filter has a finite reduction of all stopband components. Usually this attenuation can be increased at the cost of a larger complexity. The filter should attenuate the signal outside the passband band enough. The amount of attenuation that is required depends on the application. In many systems the frequency band outside the passband folds back into a neighboring channel. The required amount of attenuation depends in that case on the requirements of the adjacent channel leakage. For the DOCSIS standard as given in Chapter 3 the suppression must be better than $-72dBc$.

Passband amplitude and phase response Another important property of the filters is their amplitude and phase response in the passband. The phase response should ideally be linear. If the phase response is not linear, then the

group delay for the different frequency components of the signal are no longer equal and the signal will be distorted.

Most digital modulation techniques are sensitive to these imperfections in the channel. The amount of amplitude ripple and group delay that is allowed depends on the type of signal that is transmitted. If the signal is modulated with for example QPSK the allowed ripple is larger than for higher order modulation systems such as 256-QAM. To ease the specifications on these aspects, most communication standards define an equalizer in the receiver, to compensate for these non ideal characteristics of the transmitter and the channel between the transmitter and receiver.

For downstream digital carriers DOCSIS 1.0 specifies a maximum ripple of $0.5dB$ in $6MHz$. In DOCSIS 1.1 the specification is relaxed to $3.0dB$ in $6MHz$. The in-channel frequency response is compensated in the equalizer at the input of the receiver. In DOCSIS 1.1 the requirements for the equalizer are increased to relax the specifications for the transmitter, filters, cables and amplifiers.

The group delay of the Cable Modem Termination System (CMTS) must be less than 75ns within the designed bandwidth. For digital signals the group delay can lead to QAM symbol misinterpretation. For most types of digital filters this requirement is automatically met, because many digital filters have a linear phase, such as symmetrical FIR filters. However, for digital filters such as the IIR filter, the phase relation is never linear (for a realizable causal implementation) and care should be taken to meet this specification.

Transition region The transition region of an ideal brick wall filter is zero. In any practical filter the transition region is larger. This will limit the usable bandwidth of the system. The application in which the filter is used determines the width of the transition region. For most types of filters the transition region width also determines the complexity of the filter. The smaller the transition region the higher the complexity of the filter.

Complexity An important property of a filter is the complexity. The complexity of a filter depends on many things, but usually is expressed as the

number of multiplications and additions needed per second. A more complex filter consumes more power and therefore is less efficient.

Operation speed Not all types of filters can be used at the high frequencies that are required in this system. Filters that require feedback, with coefficients that are unequal to one, are less suitable for high speed operations, because they require a feedback from the output to the input often within a single clock cycle. In that case, pipelining can not be used to increase the operation speed of the filter, which will limit the highest operation frequency of the filter.

Filter classes

Two classes of digital filters can be distinguished.

- The Finite Impulse Response (FIR)
- The Infinite Impulse Response (IIR)

IIR filters have the advantage that they are small compared to FIR filters with similar transfer characteristics. But in this QAM modulation system they are impractical. The phase characteristic is nonlinear, which will result in distortion of the signal. In addition, the IIR filter structure requires a feedback from the output to the input within one clock cycle. This limits the use of pipelining in the multipliers and adders. Therefore, the operation speed is reduced. Several transformations have been proposed in order to pipeline IIR filters. In [86] the clustered look ahead (CLA) transformation is introduced. But this transformation has some drawbacks. Although the original transfer function is stable, the stability of the pipelined IIR filter in general is not guaranteed [87]. A modified transformation was introduced in [88] called scattered look ahead (SLA). This transformation guarantees stability, but the complexity increases. For both of these highly pipelined IIR filters applies that they are no longer more computionally efficient than their FIR counterparts. For these reasons the IIR filters are not practical for implementation reasons.

FIR filters are inherently stable, because all the poles of the filter are located at the origin and are thus located within the unit circle. They can be designed to have a linear phase response by making the coefficients sequence symmetric. The FIR filter is very flexible, because it has many parameters that can be adjusted to accommodate the required frequency response. The passband ripple, stopband suppression and transition band can be exchanged for complexity.

FIR filters

The transfer function of a FIR filter can be described by its difference equation

$$y[n] = \sum_{k=0}^{N} b_k x[n-k] \tag{6.2}$$

where x is the input signal, $b_0 ... b_N$ are the filter coefficients and $N+1$ is the number of coefficients.

The choice of architecture for the implementation of a FIR filter includes considerations of several factors, such as hardware complexity, throughput and power consumption. Many different structures exist, most of which provide some trade-off between complexity and throughput. For the system designer the choice of selecting an architecture becomes to select the least complex architecture with the lowest power consumption that can achieve the desired throughput. The ability to exchange area, power consumption and throughput makes the choice for an optimal architecture not straightforward, because many combinations exist that fulfill the requirements. In [89] several architectures have been investigated and compared. They include the *direct form* and the *transposed direct form*.

Many other architectures do exist. Some are optimized for reduction in area, by calculating the coefficients sequentially at the cost of a reduced throughput. Others are optimized for coefficients that are dynamic.

The filters that are required here need high throughput. Therefore, filters that calculate coefficients sequentially are not suitable. Since the coefficients that

are used in the filter do not need to change, the multipliers in the FIR filter can be optimized to minimize the required power and area.

A common method of carrying out multiplications by a constant value is by using a sequence of shifts and adds. To reduce the number of adders and subtractors, the Canonic Signed Digit (CSD) format is often used. The advantage of the CSD format is that no value has more than $(q+1)/2$ non zero bits; often fewer [90], where q is the word length. Multiplication by a constant requires no more than that number of additions for its implementation. For efficient multiplication, the number of non-zero CSD digits should be as low as possible for the FIR filter coefficients. The actual number depends on the accuracy of the coefficients. As the accuracy decreases the frequency response of the filter degrades and the filter's stop band attenuation decreases. As a rule of thumb, the number of CSD digits for a coefficient multiplication is one non-zero digit for every $20dB$ of stopband attenuation for each coefficient [91].

Direct form architecture The direct mapping of the difference equation describing a FIR filter into a hardware realization, see Eq. 6.2, results in the direct form architecture, see Fig. 6.6.

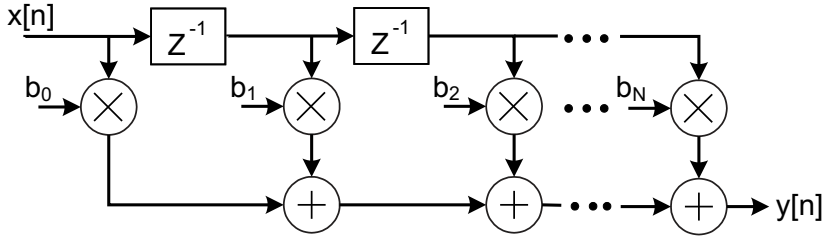


Figure 6.6: The direct form FIR filter

The delayed versions of the input are multiplied by the appropriate filter coefficients and the results are added together to form the output of the filter. The direct form architecture has the advantage that every tap of the filter is equivalent. Therefore, arbitrary length filters can be generated by cascading filter taps. FIR filters that are implemented in software often use this property, where a higher order filter requires just more clock cycles. FIR filters that are

made in hardware with filter coefficients that are fixed by design have the disadvantage that the input of the multipliers are not equal. Therefore, common sub-expressions that exist in the multipliers can not be combined and reused. In many applications the FIR filter is designed to have a linear phase. Consequently, the impulse response is symmetric. This property can be utilized in the direct form filter to reduce the number of multiplications by a factor of approximately two.

For designs where high throughput rates are required, the last addition where N terms have to be added is difficult to achieve within a single clock period. Additional pipelining will be necessary.

Transposed direct form The transposed direct form, as shown in Fig. 6.7, has, compared to the direct form implementation, as advantage that the coefficient multipliers all have the same input. Therefore common subexpressions in the coefficients can be combined. Combining all common subexpressions can reduce the number of adders in the multiplier by 50% [90]. However, the routing of the FIR filter could then become complicated, which reduces the manufacturability. Therefore, commonly not all common subexpressions are combined; only a few. Combining the two most common subexpressions already gives a reduction of 30% [90].

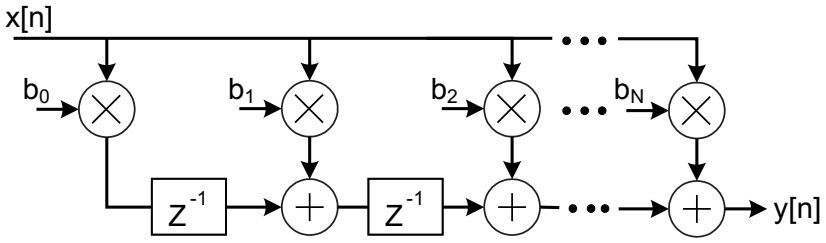


Figure 6.7: The transposed direct form FIR filter

While the direct form implementation has a final adder, where N terms are added, the transposed direct form, inherently has this pipelined. A drawback of the transposed form is the increased number of registers in the summation path. The word length after the multiplication is larger than at the input, es-

pecially when the multiply-add units are implemented based on the carry-save arithmetic to achieve high performance. While the direct conversion architecture requires

$$\#registers = (N-1)q, \tag{6.3}$$

where N is the number of tabs and q is the input word length, the transposed form requires [92]

$$\#registers = 2N(q + m + \log_2 k) + 2q, \tag{6.4}$$

where m is the coefficient word length. However, this comparison assumes that no pipelining is required in the adders and multipliers. Especially in the direct conversion architecture without additional pipelining, the speed is limited by the final adder, because N words need to be added within one clock cycle. To speed up this adder, pipelining could be applied, which reduces the difference in the number of registers that are required between the two architectures. Whether pipelining is needed depends on the sample rate, the intrinsic speed of the adders and the number of taps of the filter. The ability to reduce the complexity of the coefficient multipliers by combining the common subexpressions often outweighs the additional registers that are required [92].

Poly-phase filter architecture

The upsample filter as shown in Fig. 6.2 consists of an upsampler followed by a filter. In this architecture the filter operates at the high sample rate, $1/T_2$. At the input of the filter $N-1$ out of each N samples are equal to zero, which results in many redundant operations in the filter. A more efficient realization of the filter can be achieved by using a poly-phase structure, as shown in Fig. 6.8. The proof of the equivalence between the two representations is given in [85].

By using this architecture the N filters operate at the low sample rate, $1/T_1$. For each input sample, $x[nT_1]$, each of the N branches of the poly-phase net-

work contributes one non-zero output, which corresponds to one of the N outputs of the upsampler. A commutator, sampling at T_2, selects an output of each sub filter. The impulse response of the filters correspond to the by a factor N decimated versions of the original impulse response. The lengths of the decimated filters are equal to M/N, where M is the length of the original impulse response. To balance the computations in each branch, it is often advantageous to choose M to be a multiple of N.

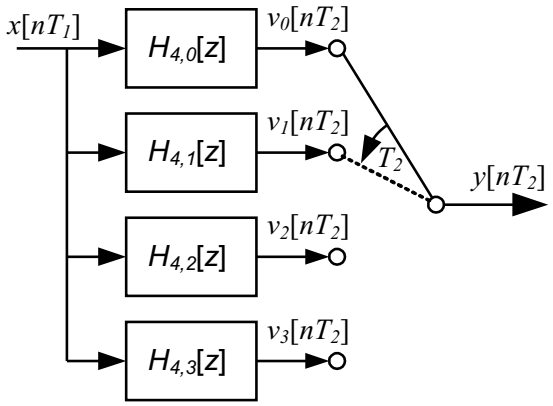


Figure 6.8: The principle schematic of a poly-phase upsampler by a factor 4.

The individual branches of the poly-phase FIR filter can be implemented in the direct form or in the transposed form. However, exploiting the symmetry of the filters coefficients is more difficult in this poly-phase structure, since at most one of the sub-filters is symmetric. This is due to the splitting of the original symmetric FIR filter into N part, where the first filter consists of the 1st, 5th, 9th,.... coefficient. The second filter consists of the 2nd, 6th, 10th,... coefficient. These are not symmetric around the center of the filter, only the last subfilter is symmetric in case the original filter is symmetric. Therefore, the transposed form implementation is preferred.

Halfband filters

A particularly efficient filter for an upsample ratio of two is called the halfband filter. Halfband filters are implemented efficiently in polyphase form, because

almost half $(N/2-1)$ of the filter coefficients equal zero. Halfband filters have two important restrictive characteristics: the passband and the stopband ripple are equal and the passband edge and stopband edge are equidistant from the halfband frequency $\pi/2$.

Halfband filters are specified with only three parameters: the order N, the stopband attenuation and the transition bandwidth. Halfband filters are often used in decimators and interpolators with sampling rate changes of two. In these systems the reduction of the computation of almost a factor of two is quite significant. The most important drawback of the halfband filters is the requirement that the stopband ripple is equal to the passband ripple. For most practical systems the requirements are such that the stopband ripple is much smaller than the passband ripple. However, since the required filter order is relative insensitive to the ripple specification, the computational price paid for designing a filter with an over designed passband ripple is small and almost always much less than the 2-to-1 reduction achieved by these filters [93].

The required order for a Kaiser window halfband FIR filter can be estimated by the empirical formula [22]

$$N = \left\lceil \frac{2(A_{stop} - 7.95)}{4.57\pi TW} \right\rceil, \tag{6.5}$$

where A_{stop} is the stopband attenuation and TW is the transition bandwidth. To reach a level for the A_{stop} of at least $80dB$, the minimum order, N, is equal to 15.

By cascading multiple upsampling stages followed by halfband filters to filter the unwanted signal components, the upsample rate can be set to an arbitrary power of two. Every upsample stage operates at a double clock frequency as the stage preceding it. When the halfband filter is implemented in the poly-phase form, the calculations occur at the input clock rate, which is half the output clock rate, followed by a commutator selecting the output samples of the two branches.

Because the calculations are performed at the low sample rate, the available period for doing the calculations is the longest. The time that is required for

calculating the coefficient multiplications and additions depends on several aspects, such as the multiplier architecture, the word length of the coefficients and the data, etc. When the sample rate is increased and therefore the clock period is reduced to a point that the time required for the calculations is larger than the clock period, the speed of the circuit has to be increased. A method to increase the speed is to select fast architectures for adders/substractors. However, when the clock speed is higher than possible with these fast architectures, pipelining has to be applied to the circuit and to reduce the number of calculations required within each clock period.

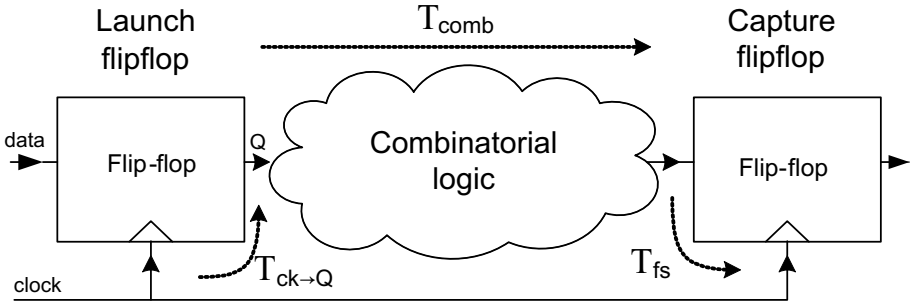


Figure 6.9: The timing of a sequential circuit.

The number of calculations that can be performed within a single clock cycle depends on the speed of the circuit and the setup and hold time of the flip-flops that clock the input and the output of the combinational logic block, see Fig. 6.9. The setup and hold time are independent of the clock period and are determined by the architecture of the latches and the process technology. The *hold time* is defined as the minimum amount of time after the clocks active edge during which the data must be stable. Any violation in these required times causes incorrect data to be latched and is known as a setup/hold violation. The *setup time* in a design determines the maximum frequency at which the chip can run without any timing failures. The effective time that the combinational logic has to reach a stable output condition is given by the clock period and the setup and hold times. The *setup time* is defined as the minimum amount of time before the clocks active edge by which the data must be stable for it to be latched correctly. Factors affecting the setup analysis are the clock period T_{clk}, clock to Q propagation delay of the launch flop $T_{ck \rightarrow Q}$, negative clock

skew T_{skew}, required setup time of the capture flop T_{fs} and combinational logic delay T_{comb} between the two flops being timed, see Fig.6.9. The following condition must be satisfied.

$$T_{clk} \geq T_{fs} + T_{ck \rightarrow q} + T_{skew} + T_{comb} \tag{6.6}$$

Using this equation the maximum frequency of a combinatorial circuit can be calculated. When the clock rate is increased more the effective time becomes less, and therefore the number of operations that can be performed in between the flip-flops becomes less.

For example, in the CMOS 90nm LP process standard cell library D-flip-flop, the following values are given: $T_{fs} = 80ps$ and $T_{ck \rightarrow q} = 300ps$. For a NAND gate the transition time is given as $T_{NAND} = 180ps$ under typical load conditions. Assuming the same clock is used to launch the data and to capture the data, i.e. zero time-skew between the input and output flip-flop and a single NAND-gate between them, the minimum clock period is given as

$$\begin{aligned} T_{clk} &\geq T_{fs} + T_{ck \rightarrow q} + T_{skew} + T_{comb} \\ &\geq 80ps + 300ps + 0ps + 180ps \\ &\geq 560ps \end{aligned} \tag{6.7}$$

The minimum clock period when a single NAND gate is used as combinatorial logic is in this example equal to 560ps, which is about 1.78GS/s, of which the majority of the time is used for the flip-flops.

The poly-phase halfband filters have the advantage of their relatively low complexity, but for every consecutive stage the clock rate doubles. Therefore, the required number of pipeline stages increases for every following filter. This pipelining increases the power consumption and complexity of the stages. As a result, the halfband filter becomes less efficient for the later stages.

To avoid the need of an excessive amount of pipelining for the stages running at the high sample rates, other architectures can be implemented. Instead of using

two cascaded upsample filters with each an upsample ratio of two, for the final stages, poly-phase upsample FIR filter can be used that has an upsample ratio of 4. The time that is available for the combinatorial logic, T_{comb}, is increased by more than a factor of two. Given the target sample rate of $2744.6MS/s$ and the numbers given in the example above, using a upsampler with a factor two, results in a time for the combinatorial logic of

$$\begin{aligned} T_{comb} &= 2 \cdot T_{clk} - T_{fs} - T_{ck \rightarrow q} \\ &= 728.7ps - 80ps - 300ps \\ &= 349ps \end{aligned} \tag{6.8}$$

Using a final upsampler with a factor 4, results in a time for the combinatorial logic of

$$\begin{aligned} T_{comb} &= 4 \cdot T_{clk} - T_{fs} - T_{ck \rightarrow q} \\ &= 1457ps - 80ps - 300ps \\ &= 1077ps \end{aligned} \tag{6.9}$$

However, increasing the upsample rate, increases the complexity of the filter, because for every doubling of the upsample ratio the required transition bandwidth is reduced by a factor two, assuming a similar effective bandwidth. Depending on the technology an optimum can be found.

In order to reduce the required order of the 4 times upsample polyphase FIR filter as much as possible, several optimizations have been applied:

- Reducing the usable passband
- Allowing more ripple in the passband

Since in an upsample filter the locations of the wanted signal band and the unwanted signal bands are known, some aliasing can be allowed in the passband

of the filter. This aliasing does not result in a reduction of the signal quality, in case the input signal bands that fold into the passband do not contain a signal. The transition width specification of the filter can be relaxed, and thereby the order of the filter. This increase in the transition width results in a reduced usable bandwidth. When the applied signal has a higher bandwidth than is allowed by the aliasing, the suppression of the images will be insufficient and they will appear in the output spectrum.

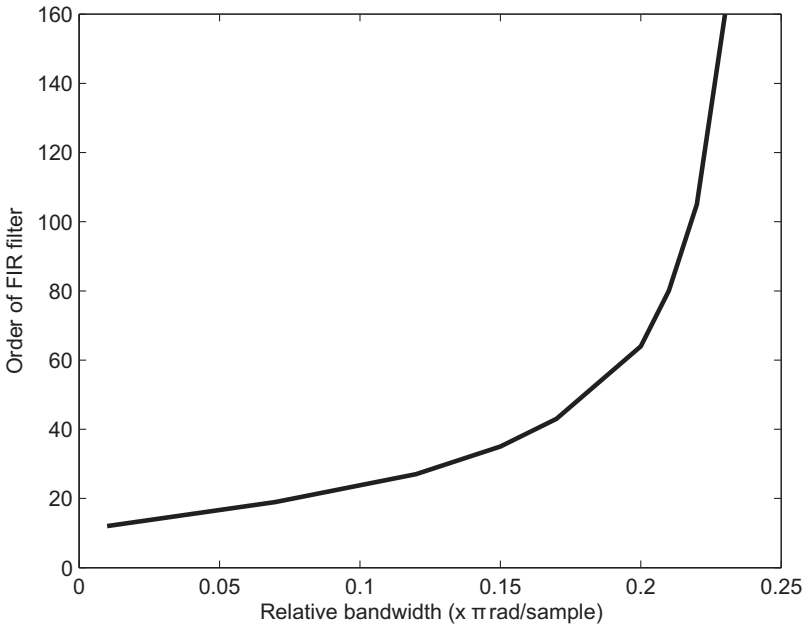


Figure 6.10: The order of a poly-phase upsampler by a factor 4 with a $A_{stop} = 80dB$ *and* $A_{pass} = 0.0017dB$ *as a function of the usable bandwidth.*

Fig 6.10 shows how the required order of the 4 times upsample filter with a $A_{stop} = 80dB$ and $A_{pass} = 0.0017dB$, depends on the usable bandwidth. Above a relative usable bandwidth of 0.2, the required filter order increased rapidly. For a relative bandwidth of 0.25 a ideal brick wall filter with an infinite order would be required.

The peak deviation in the passband is given as δ_p and the peak deviation in

the stopband is given as δ_s. The passband ripple also can be specified in terms of the maximum difference in the power level transmitted through the filter in the passband. By this definition the peak-to-peak passband ripple A_{pass} is given by

$$A_{pass} = 10\log_{10}\left(\frac{(1+\delta_p)^2}{(1-\delta_p)^2}\right) \ [dB] \tag{6.10}$$

The stopband ripple, A_{stop}, is the power difference between the nominal passband transmission level and the level of the highest ripple in the stopband. For filters that have the nominal passband transmission levels normalized at unity, the stopband attenuation is given by

$$A_{stop} = 20\log_{10}(\delta_s) \ [dB], \tag{6.11}$$

While in the halfband filter the passband ripple is by definition equal to the stopband ripple, i.e. $\delta_s = \delta_p$, it can be optimized for the polyphase FIR filter.

To reach the desired $80dB$ stopband attenuation in the case of the halfband filter it can be calculated that the passband ripple is equal to $0.0017dB$. When the polyphase upsample FIR filter would use the same stopband attenuation and passband ripple, the required order for the filter would be 46. By allowing $0.2dB$ ripple in the passband, which is with in the requirements set by the DOCSIS standard [3], the order can be reduced to 36.

The realized filter, as shown in Fig. 6.11, has a relative usable bandwidth of 0.15. Since the filter is part of a complex filter for both I and Q the total bandwidth with a sample rate of $2744MS/s$ is equal to about $2\ x\ 210MHz = 420MHz$, the stopband starts at $2\ x\ 470MHz = 940MHz$. The 36 coefficients of the filter are quantized to 14 bits and the A_{stop} after quantization of the coefficients is $\geq 75dB$ and the $A_{pass} = 0.2dB$.

In Appendix A.3, the power consumption for the final 4 times upsampling using two complex halfband FIR filters implemented in CMOS technology is estimated to be about $320mW$, while for the realized complex poly phase FIR

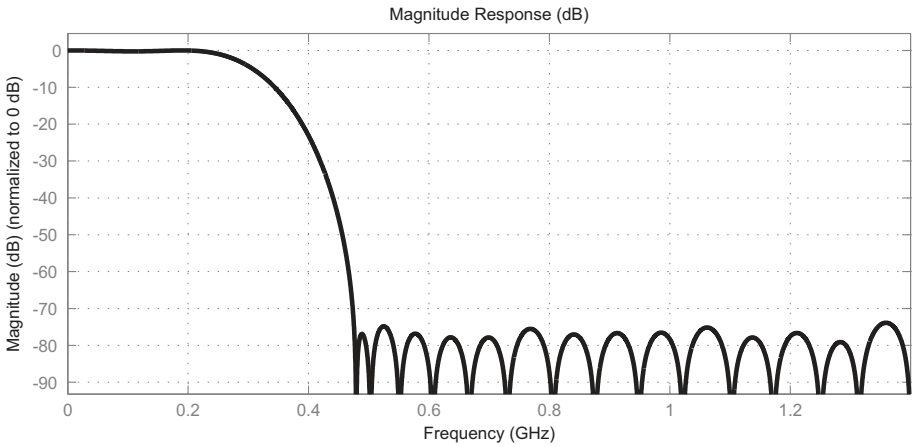


Figure 6.11: The frequency response of the realized poly-phase upsampler by a factor 4.

upsample filter as shown in Fig. 6.11, the power consumption is estimated to be about $270mW$, see Appendix A.2.

CIC filters

An alternative efficient filter structure for performing interpolation and decimation was introduced in [94], called the Cascade Integrator Comb filter. This filter uses no multipliers, but only adders and delays. The complexity of this filter is therefore low, compared to the FIR filter. The filter can handle arbitrary integer sample rate changes. The structure of the filter is shown in Figure 6.12. The filter upsample ratio used is independent of the structure of the filter. When the upsample ratio is changed, only the interpolator is required to change. The other parts of the system can be kept the same. The number of stages (R) in series determines the ability to attenuate the signal outside the band of interest. The shape of the filter is given by the order (R), the delay in the comb stages (M) and the upsample ratio (N).

The filter consists of two types of building blocks: Combs and integrators. The

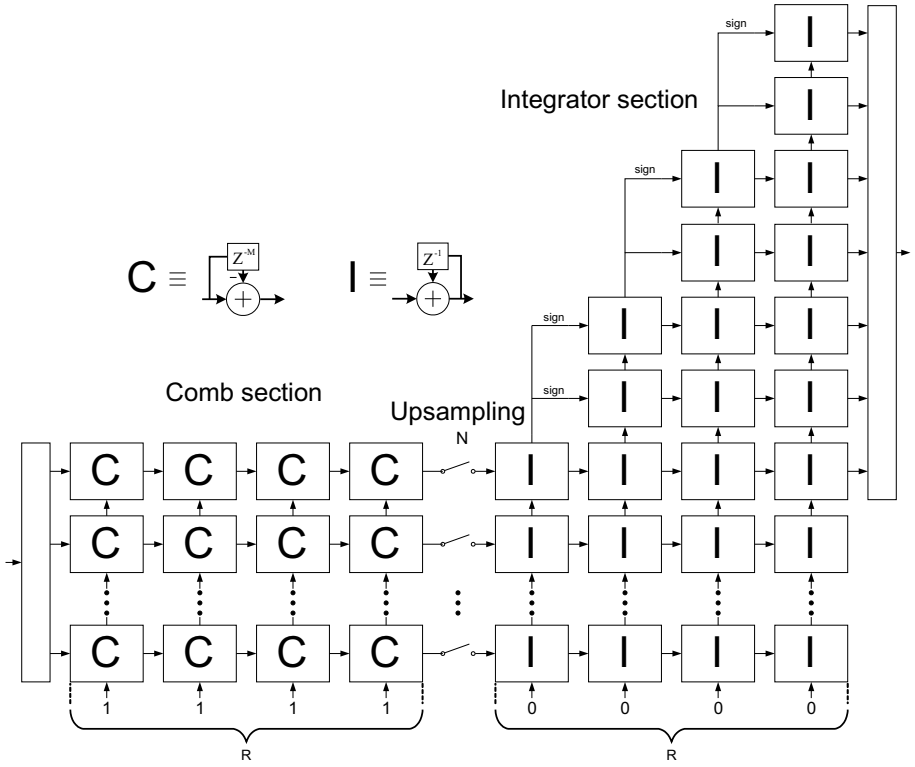


Figure 6.12: CIC filter structure

transfer function of the comb filter is given by

$$H_C(z) = 1 - z^{-M}. \tag{6.12}$$

The comb sections are running at a lower speed of $\frac{f_s}{N}$, where f_s is the sample rate at the output. The comb sections act as a high pass filters with a $20dB$ gain per decade. The comb section is given by

$$y[n] = x[n] - x[n - M], \tag{6.13}$$

where M is the differential delay. M is an arbitrary positive integer, but is usually equal to one or two.

The integrator is a simple filter with a unity feedback coefficient.

$$y[n] = y[n-1] + x[n]. \tag{6.14}$$

The transfer function for the integrator is thus given by

$$H_I(z) = \frac{1}{1 - z^{-1}}. \tag{6.15}$$

Due to its single pole at $z = 1$ the integrator by itself is unstable. The integrator works like a low pass filter with a $20dB$ per decade roll off.

The complete transfer function of the CIC filter, with T_s normalized, is given by

$$H(z) = H_I^R(z)H_C^R(z) = \frac{(1 - z^{-NM})^R}{(1 - z^{-1})^R} = \left(\sum_{k=0}^{NM-1} z^{-k} \right)^R. \tag{6.16}$$

The frequency response is given by Eqn. 6.16, evaluated at

$$z = e^{j2\pi f/N}, \tag{6.17}$$

where f is the frequency relative to the low sampling rate f/N. The magnitude response of the filter is given by

$$|H(f)| = \left| \frac{\sin(\pi M f)}{\sin\left(\frac{\pi f}{N}\right)} \right|^R, \tag{6.18}$$

which can be simplified by using the relation $\sin(x) \approx x$ when x is small. The response becomes then

$$|H(f)| \approx \left| NM \frac{\sin(\pi M f)}{\pi M f} \right|^R, \qquad for\ 0 \leq f < \frac{1}{N}. \tag{6.19}$$

In Figure 6.13 the output response is drawn for a filter with an upsample ratio of $N = 6$, $M = 1$ and $R = 2$. As the figure shows, the output spectrum has nulls at multiples of $f = \frac{1}{M}$. Around these locations aliasing occurs. If we

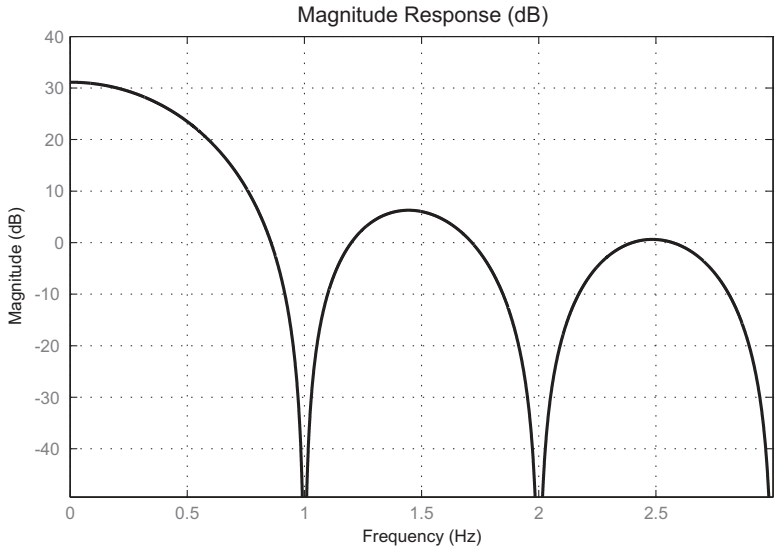


Figure 6.13: CIC filter response for $N = 2$, $M = 1$ and $R = 6$

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define f_c as the usable passband of the filter, then the aliasing regions are at

$$(i - f_c) \leq f \leq (i + f_c), \tag{6.20}$$

for $f \leq \frac{1}{2}$ and $i = 1, 2, \ldots, \lfloor \frac{R}{2} \rfloor$.

CIC filter with pre-correction Increasing the order N will improve the aliasing rejection, but it will also increase the passband droop. The CIC filter as described before can not meet the specifications required for the system, due to the pass-band droop, see Fig. 6.13 and Fig. 6.14. A possible solution for this passband droop is to use precorrection. This precorrection can be done by using a FIR filter. The FIR filter can be used at the low sample rate. The phase response of the CIC filter is linear, the group delay is therefore constant. The gain of the filter depends on the upsample rate. To compensate for this variable gain the output of the filter should contain a shift register to select the correct bits from the output word.

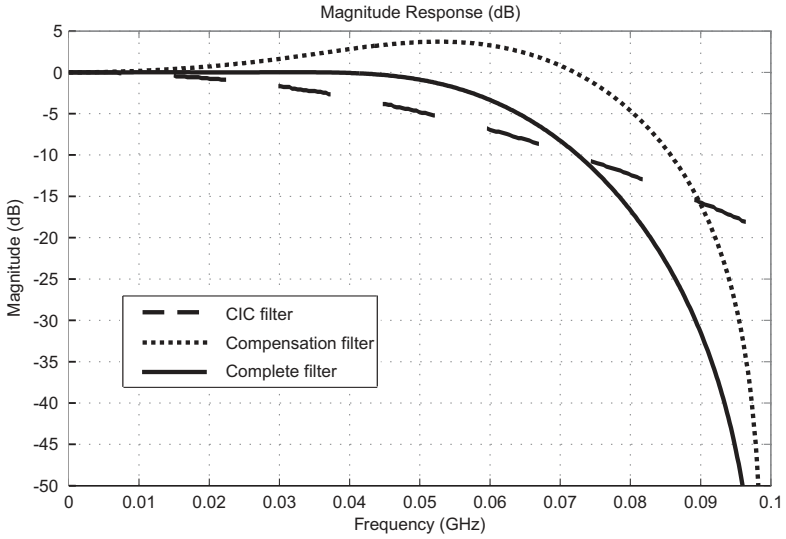

Figure 6.14: CIC filter passband response with $R = 15$, $M = 1$ and $N = 5$ and compensation filter

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The CIC filter is implemented in the CML version of the IC. The filter is implemented in custom made Current Mode Logic (CML), see Chapter 5.6.2. A advantage of this CIC filter compared with a polyphase upsample FIR filter, is its regular structure. The CIC upsample filter requires two cells, the comb and the integrator. This allows easy design and optimization of especially the integrator cell, which is used at the high sample rate. The upsample rate of the CIC upsample filter can be changed easily by changing the divider ratio between the high sample rate and the low sample rate and selecting with a scaler the appropriate bits at the output of the CIC filter, because the gain of the CIC filter depends on the upsample ratio. The implemented CIC filter, see Fig. 6.14 and Fig. 6.15, has 5 comb stages and 5 integrator stages, with a delay of one in the comb stage. Including the pre-compensation filter the usable bandwidth for the complex upsample filter is equal to $100MHz$. To simplify the design of the divider between the high sampling section and the low sampling section, the possible upsample ratios are limited to factors that are powers of two.

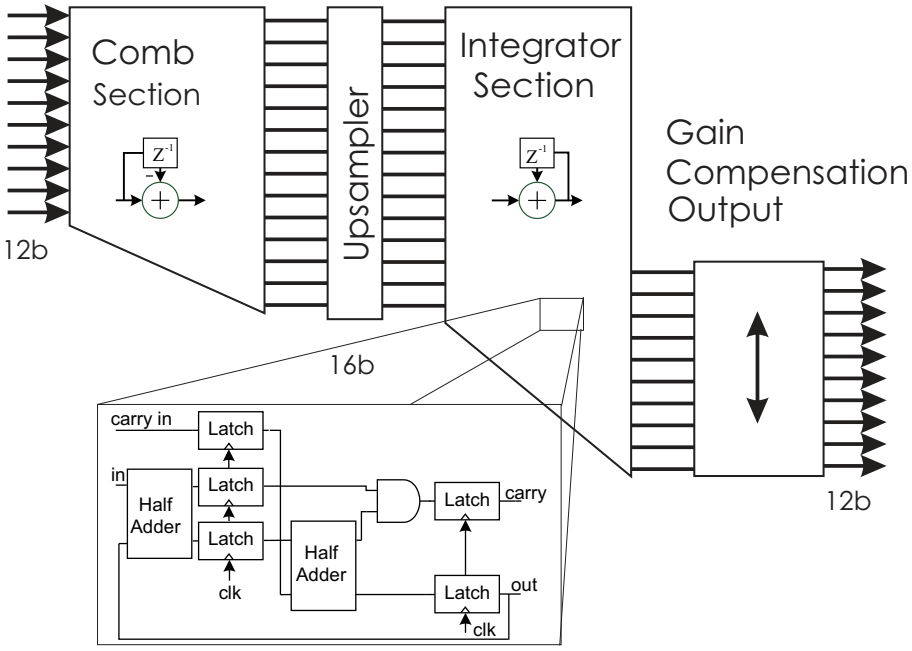

Figure 6.15: CIC filter implementation for $R = 15$, $M = 1$ and $N = 5$. With the circuit details of an integrator bit.

The number of bits needed for each comb stage and each integrator stage is given by [94]

$$\begin{aligned} W_{comb}(s) &= \lceil \log_2 (2^s) \rceil \\ W_{integrator}(s) &= \left\lceil \log_2 \left(\frac{2^{N-s}(RM)^s}{R} \right) \right\rceil \end{aligned} \tag{6.21}$$

The number of bits at the input is 12. Given a maximum upsample ratio of 16, the comb stages require 12, 13, 14, 15, 16 bits, respectively. For the integrator stages the number of bits are equal to 16, 19, 22, 25, 28, respectively. The bit growth for an upsample ratio of 16 is equal to 16 bit, for an upsample ratio of 2 the bit growth is equal to 4 bits. At the output of the CIC filter a scaler has been implemented to select the correct output bit depending on the upsample

ratio.

The power consumption of the CIC upsample filter, implemented in CML is estimated in Appendix A.4, to be about $250mW$.

6.2.4 Numerically controlled oscillator

The upconversion of the signal in the digital domain, is similar to the upconversion in the analog domain. It involves the multiplication of the signal with a periodic signal, commonly a sinusoid. There are many methods of generating this sinusoidal signal. Most algorithms use the architecture that is shown in Fig. 6.16. It consists of an accumulator that is incremented by the frequency control word, followed by a phase-to-amplitude converter which creates the sinewave shape. The phase-to-amplitude converter can be implemented using different methods. Common techniques are Lookup Table (LUT), a trigonometric identity, the Nicholas method, the use of Taylor series and the CORDIC algorithm.

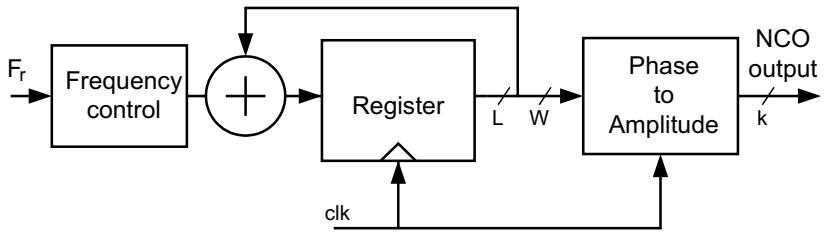

Figure 6.16: The general NCO architecture

Phase accumulator

Most algorithms are composed of a phase accumulator followed by a phase-to-amplitude converter, see Fig. 6.16 and Fig. 6.17. The phase accumulator calculates the phase by adding a phase increment in an accumulator every clock cycle. The overflow rate of this accumulator gives the output frequency

$$f_{out} = \frac{F_r}{2^L} f_{clk}, \tag{6.22}$$

where F_r is the phase increment or frequency control and L is accumulator word length. The frequency resolution is given by

$$\Delta f = \frac{f_{clk}}{2^L}, \tag{6.23}$$

Often the accumulator word length is longer than the word length used in phase-to-amplitude converter. This truncation of the length causes spurs in the output spectrum of the modulator. The effects of this phase truncation have been analyzed in [95, 96, 97].

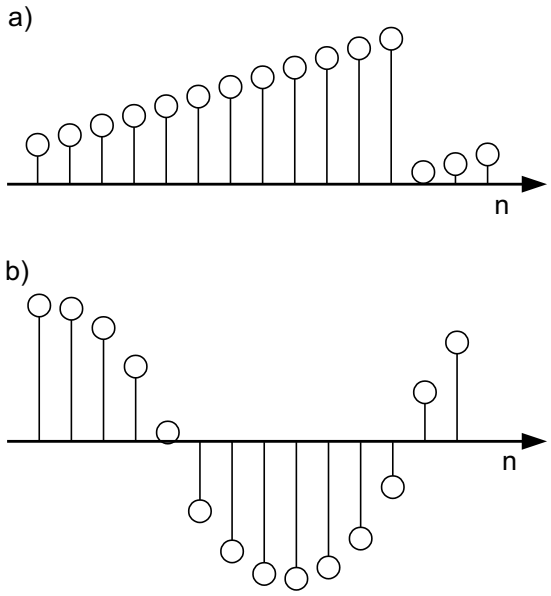

Figure 6.17: The signals in the NCO, a. the phase accumulator output, b. the NCO output

Delay equalization

At the required sample rates and the long word length of the phase accumulator, the phase accumulator can not complete the multi-bit addition within one clock period, because of the carry bits that ripple through the adder. In order to reach to required operation speeds a pipelined implementation is required. To reduce the number of gate delays per clock period, the adder can be split into smaller segments which are reclocked in each segment. This way the operation speed of the system is not limited by the speed of the accumulator. However, at the output of the accumulator all the bits need to arrive at the same moment. This is done by adding flip-flops to delay equalize the accumulator. At the input also the frequency control word needs delay equalization, to ensure correct operation when the frequency control word is changed. The delay equalization circuitry is thus large. The total number of flip-flops in the delay equalization is given by

$$\#DFFs = \frac{L(L-S) + W(W-S)}{2S}, \tag{6.24}$$

where S is the size of the segment and L is the length of the accumulator and W is the truncated word length of the accumulator. When a 32-bit accumulator is used with a segment size of 4-bit and the output word length is equal to 16-bit. Then the number of flip-flops required for the delay equalization alone is equal to 136.

Phase-to-amplitude conversion

For the conversion of the phase to sine many methods exist, examples are ROM look-up, Taylor series and CORDIC algorithm.

ROM look-up table The conventional method of generating a sinusoidal signal from the phase is the use of a ROM look-up table (LUT). The read only memory (ROM) is programmed with a sine-wave. The phase is connected to the address input and the data output returns the amplitude corresponding to this

phase input. The values that are stored in the ideal case without quantization of the phase and amplitude are given by

$$s(n) = \sin\left(2\pi \frac{\Delta F(n)}{2^W}\right), \tag{6.25}$$

where $\Delta F(n)$ is the phase register value with a length of W bits. The size of the ROM is $(2^W \cdot k)$, where W is the truncated phase address, and k is the word length of the amplitude. The number of words in the LUT determines the amplitude and phase quantization, which determines the spectral performance of the NCO. However, a larger ROM results in a higher power consumption, lower speed and larger size of the circuit.

A well known technique to reduce the size of the ROM is to exploit the symmetries of the sine-wave and store only a quarter of the period. The reduced memory size is traded for additional logic to calculate the complements of the accumulator and lookup table output. The size of the ROM is reduced by a factor of 4 and the two most significant digits of the phase are used to decode the correct quadrant.

Look-up table compression Other techniques to reduce the size of the ROM further are examined in [84] at the cost of increased logic. Multiple algorithms are compared to the uncompressed memory size of the ROM LUT. The compression ratios of the algorithms can be significantly, especially when the desired signal quality is high, and therefore the ROM size is large. An example is given for a spectral purity better than $85dBc$. The uncompressed memory size of the ROM is taken as a reference and is equal to $2^{14}\ x\ 12\ bits \simeq 200\ kbit$. With the modified Sunderland architecture [98, 99, 100] a compression ratio of 59:1 is achieved for the size of the ROM, at the cost of an adder. For the Nicholas architecture [95] a compression ratio of 128:1 is achieved with an additional adder/substractor.

However, the main disadvantage of a memory based NCO is its relative large access time of the memory. This limits its use at high frequency operation. Since memories themselves are difficult to pipeline, other methods must be

used to compensate for this access time. Placing multiple instances of the memory, each operating at a different phase of the clock, can be used to achieve the required operation speed. However, this increases the total memory size. An alterative is the use of a method that does not require a ROM-table. A commonly used algorithm that does not require memory for its operation is the CORDIC algorithm.

CORDIC The CORDIC is an acronym for COordinate Rotation DIgital Computer. The algorithm was first introduced by Volder [101]. Later it was developed into an unified algorithm to compute a variety of transcendental functions [102]. The CORDIC algorithm has two basic modes, the rotation mode and the vectoring mode. Both methods of the algorithm are realized as an iterative sequence of additions, subtractions and shift operations. Due to the simple operations that are used, the CORDIC is well suited for VLSI realizations. For the NCO only the rotational mode is used and will be examined in more detail.

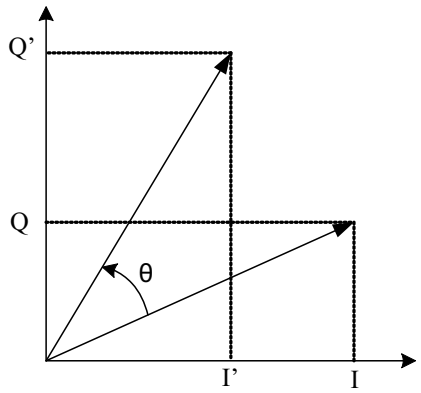

Figure 6.18: Vector rotation

The algorithm is derived from the general rotation transformation, see Fig. 6.18. Where the vector I, Q is rotated by the angle θ to I', Q'

$$\begin{aligned} I' &= I\cos(\theta) + Q\sin(\theta) \\ Q' &= Q\cos(\theta) - I\sin(\theta). \end{aligned} \tag{6.26}$$

This equation can be rearranged to

$$\begin{aligned} I' &= \cos(\theta)\left[I + Q\tan(\theta)\right] \\ Q' &= \cos(\theta)\left[Q - I\tan(\theta)\right]. \end{aligned} \tag{6.27}$$

When the rotation angles are restricted to $\tan(\theta) = \pm 2^{-i}$, where $i = 0$ to N, the multiplications of the tangent are reduced to shift operations. The CORDIC algorithm is graphically shown in Fig. 6.19. Arbitrary rotation angles can be achieved by performing iterations of successively smaller rotations. In every iteration a decreasing angle is added or subtracted. Because $\cos(\theta) = \cos(-\theta)$, the term $\cos(\theta)$ does not depend on the sign of the angle and therefore it becomes a constant. The rotation therefore can be expressed as

$$\begin{aligned} I_{i+1} &= k_i\left[I_i + Q_i d_i 2^{-i}\right] \\ Q_{i+1} &= k_i\left[Q_i - I_i d_i 2^{-i}\right], \end{aligned} \tag{6.28}$$

where $d_i = \pm 1$ and

$$\begin{aligned} k_i &= \cos(\tan^{-1}\left(2^{-i}\right)) \\ &= \frac{1}{\sqrt{1 + 2^{-2i}}}. \end{aligned} \tag{6.29}$$

The angle of the composite rotation is defined by the sequence of additions and subtractions of iterations of successively smaller angles. The resolution of the rotation angle is given by the binary arc-tangent. The angle is calculated for

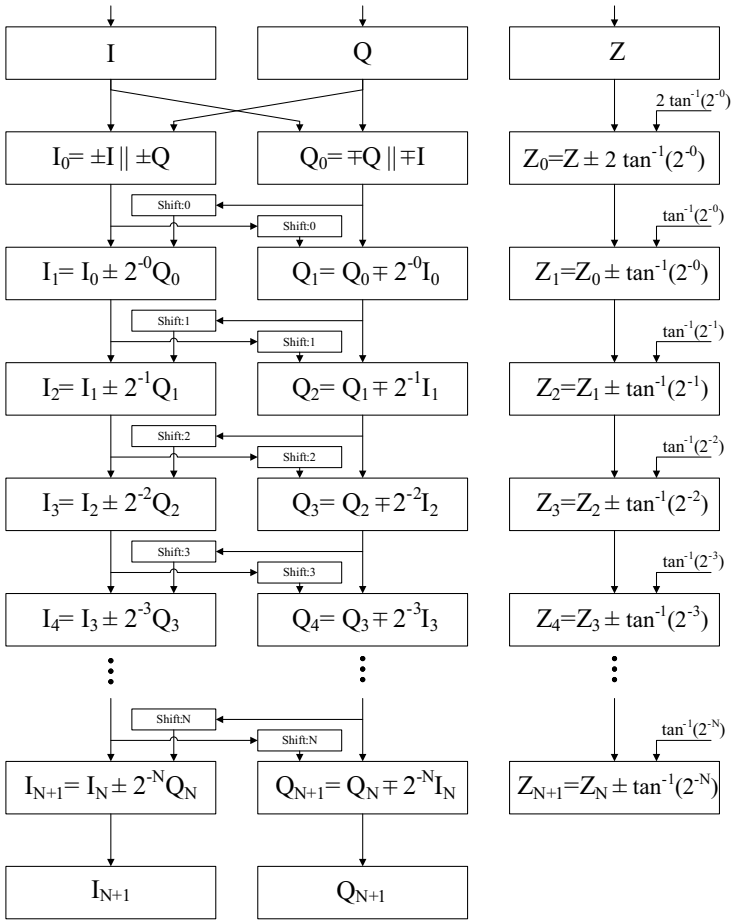

Figure 6.19: The CORDIC algorithm: Adding and subtracting iteratively

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each iteration, i, by

$$z_{i+1} = z_i - d_i \tan^{-1}\left(2^{-i}\right). \tag{6.30}$$

The CORDIC rotation algorithm only converges when the angle at the input is between $-\pi/2$ and $\pi/2$. Therefore, as a first stage an initialization rotation is required to ensure that the angle is within this convergence range. This first

stage is given by the following equations when the input angle is between $-\pi$ and π

$$\begin{aligned} I_0 =& d_{in} Q_{in} \\ Q_0 =& -d_{in} I_{in} \\ z_0 =& z_{in} - d_{in} 2 \tan^{-1} 2^0, \end{aligned} \tag{6.31}$$

where

$$d_{in} = \begin{cases} -1 & if\ z_{in} < 0 \\ 1 & otherwise. \end{cases} \tag{6.32}$$

Scaling of I and Q

To restore the signal levels to the expected levels, scaling has to be applied to the input or output signals. The gain depends on the number of iterations and is given by

$$G_N = \prod_{i=0}^{N-1} \sqrt{1 + 2^{-2i}}. \tag{6.33}$$

When the number of iterations approaches infinity the gain becomes approximately 1.647. When both the I and Q component at the input of the CORDIC have their maximum value the output value is equal to $\sqrt{2}$, together with the gain of the algorithm, the total gain is equal to 2.329.

The result from the CORDIC has to be corrected, because of this gain in the algorithm. Many articles have been written about this scaling issue and have suggested methods to implement the scaling at low complexity. Different methods are compared in [103]. Three different methods of correcting the scaling are commonly used:

- Multiplication of the output or input of the CORDIC by a constant, inversely proportional to the gain of the algorithm. This is the most straightforward method to compensate for the scaling, but at the cost of an additional multiplier.
- Compensate the scaling in every iteration by repeating the calculations, such that the scaling becomes a factor of two, which can be compensated by a shift operation.
- The CORDIC iterations can be merged with scaling factor compensations as performed in [104]

All these methods increase the complexity and the latency of the CORDIC. However, since the scaling factor is known and constant given the number of stages, the scaling can be compensated without cost in the polyphase FIR filter preceding it by adjusting its coefficients. Therefore this method is preferred and will be used.

Quantization errors

An accurate description of the quantization errors in the CORDIC algorithm is given in [105]. Two distinct sources of errors are identified. The first is the angle approximation, because of the finite number of stages. The second is the finite word length of the arithmetic. The error analysis in [105] is based on the assumption that the error reaches its maximum value at each quantization step. This results in pessimistic values, especially in a modulator where the input of the I and Q are random signals [106]. In [84] the quantization step is assumed to be uncorrelated with the input signal. With this assumption the signal-to-noise ration of the CORDIC is given by

$$\frac{S}{N} = \frac{2\delta^2}{0.1965n2^{-2(b-1)} + 2\delta^2 {G_N}^2 \left\{ \frac{(a_{n-1})^2}{3} + (n-2)\frac{\pi^2 2^{-2b}}{3} \right\}} \tag{6.34}$$

where δ^2 is the variance of the I_0 and Q_0 input signal and G_N is the gain of the CORDIC algorithm as given in Eqn. 6.33, b is the number of bits in

the arithmetic and a_{n-1} is the smallest elementary rotation angle and n is the number of stages.

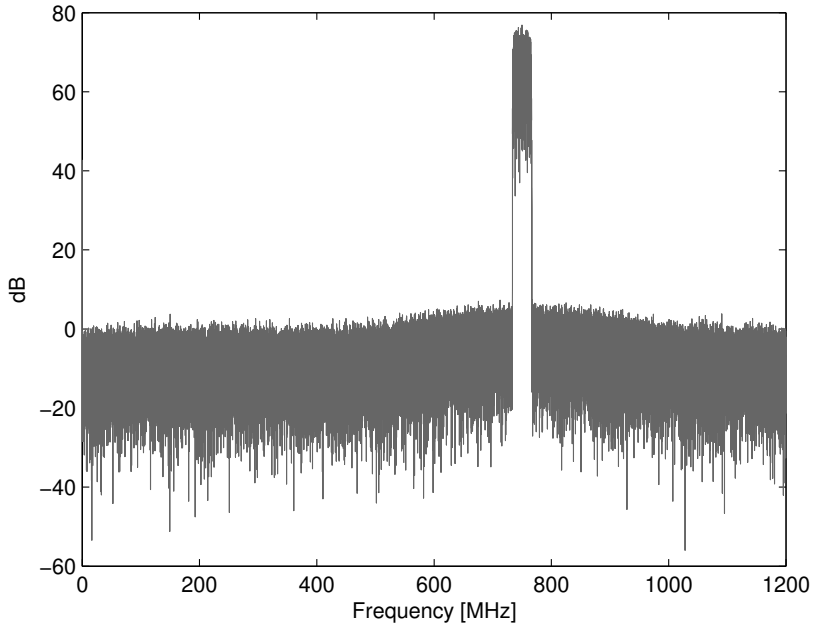


Figure 6.20: The output spectrum of the CORDIC algorithm.

From this equation the number of bits for the data path is determined to be 20 and 11 stages are used. The spectrum of a 5 carrier QAM signal is given in Fig. 6.20 and has a SNR equal to $69.7dB$.

6.3 Digital signal processing architecture

To proof the concept of the 'All-digital' transmitter, two ICs have been designed. Both ICs contain contain Digital Signal Processing (DSP) and a high speed DAC. The main difference between the two realizations is in the DSP. In the first version the DSP is implemented in CML, while in the second version the DSP is implemented in standard CMOS logic.

In the CML version the integrator section of the CIC upsample filter and the CORDIC run at the same clock rate as the DAC does, see Fig. 6.21. The implemented CIC filter supports an upsample rate of 2 to 16, which results in an input data rate of $171MS/s$ to $1372MS/s$ when the DAC clock rate is set to $2744MS/s$.

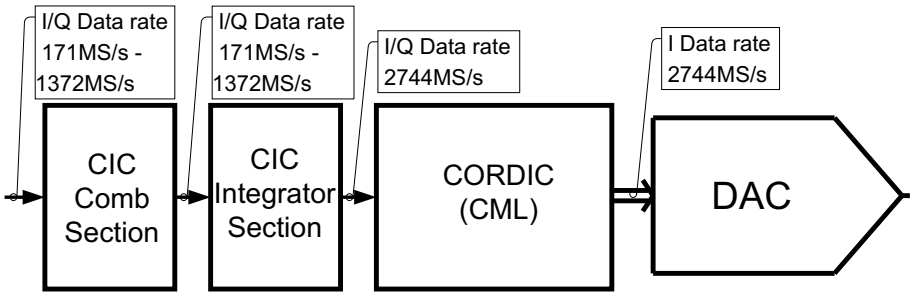


Figure 6.21: The architecture of the digital signal processing for the CML implementation

The CMOS implementation of the DSP consists of a poly-phase upsample FIR filter that has 4 phases, see Fig. 6.22. The upsample rate of the upsample filter is fixed to a factor 4, which results in an input data rate of $686MS/s$ when the DAC clock rate is set to $2744MS/s$. The poly-phase upsample filter is followed by 4 parallel CORDICs that have a synchronization mechanism to align the phases of the frequency tuning word and phase adders. Each of the four phases runs at a quarter of the DAC clock rate.

Commonly digital circuits are clocked by a single clock for all the circuits, see Fig. 6.23(a). This eases the design of the digital circuits because there are no clock boundaries that have to be crossed. Therefore the verification whether the circuits achieve the targeted operation frequency is easier. When multiple clocks are used, any communication between circuits that are clocked with different clocks can create problems to achieve correct timing.

The effect of the current consumption of a traditional static CMOS logic circuit is depicted in Fig. 6.23(a). It shows that the supply current is drawn in peaks that are synchronous with the digital clock frequency. At the rising edge of the digital clock, the clock network becomes active. The delay of the clock

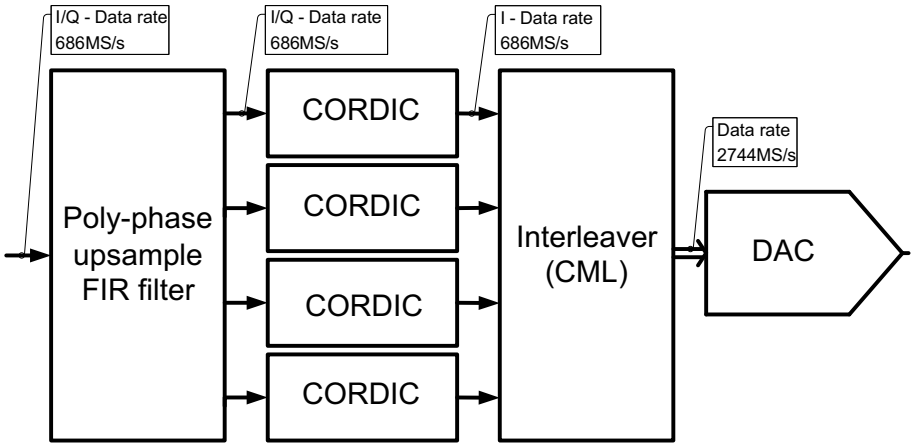
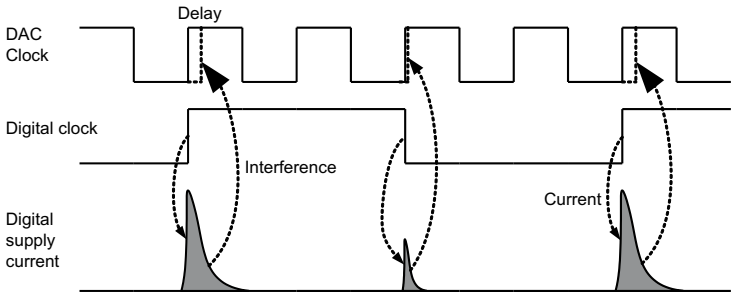


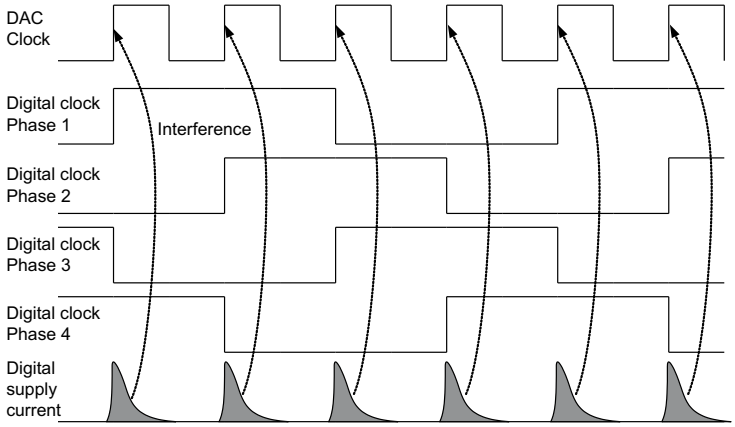
Figure 6.22: The architecture of the digital signal processing for the CMOS implementation

network is normally small, which results in a fast rising supply current. When the clock has completed the transition, the edge clocked flip-flops output their internal data value. The combinatorial logic will settle to a new stable state. The time this takes depends on the logic depth of the combinatorial circuit that is in between the flip-flops, but is commonly a large portion of the clock cycle. At the falling edge of the clock the clock network will change its level and a peak in the supply current is the result of it. Because the data at the input of the combinatorial logic does not change on this edge, this peak is smaller and shorter than at the rising edge. Before the next rising edge all the combinatorial circuits must be settled to their final value. For a properly designed circuit, therefore only a small amount of current is drawn from the supplies, which is mainly determined by the leakage current. The data is then clocked in by the next rising clock and the cycle starts again.

A part of this peak current is drawn from the local decoupling capacitors and the remaining is drawn through the supply pins of the package. The amount that is delivered through the external pins depends on the impedance that is present in the supply network. For these fast rising transients the inductance of the bondwires is commonly responsible for the main impedance. Reducing the bondwire inductance by placing more supply pads in parallel is not necessarily



(a) Interference from a single clock phase digital circuit



(b) Interference from a poly clock phase digital circuit

Figure 6.23: Interference coupling to analog blocks and clock

an improvement, because then more of the transient current will be supplied from the external capacitors and less from the local decoupling. This increases the peak current that flows through these bondwires and increases the coupling into bondwires that are nearby. The higher peak currents can also cause voltage fluctuations over any common impedance that is shared between the analog and digital supplies. A good grounding and supplying strategy is therefore essential. On the other hand, when the inductance of the supply is large, more current is drawn from the local decoupling, which results in a voltage dip in the IC. This voltage dip decreases the noise margin of the circuits and the voltage fluctuations can capacitively couple through the substrate to the analog circuits.

Designing an architecture with a single clock for all the digital logic could have some major drawbacks, because the clock of the DAC has, in this case, a four times higher frequency. Therefore, every fourth DAC clock cycle the digital circuits are clocked as well, the DAC clock is possibly to be influenced by it. When the DAC clock is delayed or advanced every fourth clock cycle, the resulting output spectrum will show modulation of the DAC input signal around the frequency $f_s/4$. Another possible coupling is the direct coupling of the $f_s/4$ clock frequency component through the substrate, supplies or common inductances to the output. At a DAC clock frequency of $2744MS/s$ the digital clock is equal to $686MS/s$, which falls in the bandwidth of interest. These possible interference issues must be minimized in order to comply to the required specifications.

To reduce the problems that are caused by the coupling, either capacitive or inductive, between the sensitive analog and the digital circuits, a poly clock phase solution could help, see Fig. 6.23(b). The clocks of the digital circuits are split into four phases, with every phase one DAC clock cycle delayed compared to the previous phase. In this manner, at every DAC clock cycle a part of the digital circuit is active. In addition, the peak currents are reduced by a factor 4 and when all phases are completely equal, every DAC clock cycle would be affected in a similar manner, eliminating all $f_s/4$ components. The direct coupling to the output would appears as a clock feedthrough that is synchronous with the DAC clock at the output of the DAC. Because the DAC clock frequency is much higher than the highest signal band that is of interest, it will not cause problems since these frequencies are filtered by the low-pass output filter.

In practice not all four phases are exactly equal to each other, therefore the reduction of the $f_s/4$ product will be finite. This imbalance of the phases is mainly caused by the poly-phase upsample FIR filter that has different coefficients for each of the four phases. The four clocks each have their own clock network. These networks differ from each other in the loading. Therefore, the delay of these networks will not exactly be equal. This will change the moment the current is drawn from the supplies. In addition, when the coupling through the substrate is the dominant source of interference, the distance between the aggressor and the victim is important. The phases that are physically closer in

the IC will have a larger coupling to the analog components, thereby reducing the cancelation of the $f_s/4$ component.

The expected reduction of the mixing products and the direct coupling products is 10 - 30dB according to some simulations. These numbers are hard to quantify, because of the many possible coupling paths between the digital and the analog components.

6.4 Power consumption in digital logic

Low-power designs have received a large amount of attention recently as portable applications gain market share. However, even in high performance designs, power has become an issue since the high frequencies that are attained can lead to power dissipations of multiple watts. Dissipation of this amount of power requires a special package and a heat sink, resulting in higher cost and potential reliability problems. Understanding and proper modeling of the power consumption is important to predict and optimize the system.

6.4.1 Power consumption in CMOS logic

Dynamic power is the largest component of the total circuit's power consumption. It is caused by the charging and discharging of capacitive loads at the output of gates. The dynamic power consumption of digital CMOS logic circuits is determined by the supply voltage V_{DD}, the clock frequency, f, the capacitance, C that has to be charged and discharged, and the activity factor α that indicates how probable it is that the circuit changes state:

$$P_{CMOS} = \alpha f C V_{DD}^2. \tag{6.35}$$

To estimate the power of a digital CMOS circuit, it was sufficient in the past to concentrate on the logic gates of the circuit and neglect the effects of the interconnect, as the delay and most of the capacitance was mainly determined

by the logic gates. In deep sub micron designs, this is no longer true, because the interconnect capacitance has not scaled down as much as the gate capacitance. The charging and discharging of the capacitive component is the dominant component of the total power dissipated in static CMOS circuits. Therefore, the relative increase of interconnect capacitance with respect to the gate capacitance results in an increased importance of interconnect loading for the power estimation [107].

Although the capacitive component is usually dominant, for some deep submicron circuits, mainly for low power circuits that are operating a large amount of time in standby mode, the leakage power can become the dominant energy consumption [83]. For circuits that are always active, such as these upsample circuits and NCO, the leakage power can be neglected.

Interconnect length

Since almost all designs are based on hierarchy, a relation was described in 1971 by Landman and Russo [108], that relates the number of pins (input or output), P, of a logic circuit to the number of blocks (cells or gates), G, in the circuit and the average number of pins per block, F. This equation also known as Rent's rule, which is stated as

$$P = F \cdot G^p, \tag{6.36}$$

where the superscript p in the equation is an empirical constant having a value in the range of $0 < p < 1$. Generally p varies from 0.4 for simple regular designs up to 0.8 for complex designs having a large amount of interconnect [109]. The parameter p is a measure of how many of the gates in a circuit communicate with the outside world. Most of the nodes inside a circuit need to interact with other internal gates of the circuit. Some, however, do need to interact with external connections.

The power of Rents rule is that it can be applied recursively on a circuit, resulting in an increasingly smaller logic block. Eventually, the logic block consists

of just a few gates. With the help of this recursion property, an estimation can be made of the interconnect distance between two blocks. In [110] the interconnect length is estimated on a two dimensional Manhattan grid. Almost all digital circuits use such a Manhattan grid style for the circuits and wires. Therefore, nearly all wire length estimation tools use this or a derivative of this model.

The model presented in [110] of the average wire length estimates the average interconnect in terms of gate pitches. A gate pitch is the distance from the middle of one logic gate the the middle of the next gate. The average wire length is given by

$$L_{avg} = P_g \cdot R_{avg}, \tag{6.37}$$

where P_g is the gate pitch in μm, which is determined by the process technology, and R_{avg} is given in [110] as

$$R_{avg} = \frac{2}{9}\left(7\frac{G^{p-0.5}-1}{4^{p-0.5}-1} - \frac{1-G^{p-1.5}}{1-4^{p-1.5}}\right)\frac{1-4^{p-1}}{1-G^{p-1}}, \tag{6.38}$$

in the case the $p = 0.5$ the equation becomes

$$R_{avg} = \frac{2}{9}\left(7\log_4 G - \frac{1-G^{-1}}{1-4^{-1}}\right)\frac{1-4^{-0.5}}{1-G^{-0.5}} \tag{6.39}$$

The gate pitch is traditionally determined by taking the square root of the chip area divided by the number of gates [111]. According to [112], the size of a logic cell is set by the metal pitch (MP) of the lower-level interconnect layers in a process. In [111] it is found that for basic gates such as a 2-input NAND gate that the size of this cell for most standard drive strengths is 4 MP across and 16 MP high. Other cells are either narrower or wider, depending on the number of inputs, transistor and drive strength of the cell. This results for a typical cell library in a average gate area of $64MP^2$.

In complex circuits the required interconnect between cells becomes more and more dominant. To fit the interconnect, cells are placed further apart. This

unused area is commonly filled by decap cells that help to supply the current peaks at the moment of switching. In [111] a constant called silicon efficiency, (SE) is introduced which in deep sub-micron technologies standard cell based ASICs typically is around 50 %. With this additional decap the average gate pitch increases and is given by

$$P_g = \frac{8 \cdot MP}{\sqrt{SE}}, \tag{6.40}$$

The average wire length within a module corresponds to a point-to-point connection with a fan-out of one. Part of the nets, however, require a larger fan-out, because it needs to drive multiple gates or gates at a larger distance. In [113] an empirical relationship is given that relates linearly the average point-to-point wire length to the fan-out (fo):

$$L_{avg}^{fo} = L_{avg}^{p-p} \left(1 + K(fo - 1)\right), \tag{6.41}$$

where $K = 0.4$. In [113] $K = 0.3$ was used, but in [111] this value has empirically determined to fit better with a value of 0.4. This relationship has seen to hold in deep sub-micron technology designs for fan-outs < 8. However, since most routing is local and therefore has reasonably small fan-outs, this limitation should not be significant.

Interconnect capacitance

For accurately estimating the interconnect capacitance in circuits, field solvers are commonly used. While they are accurate they are also slow and not capable to give estimations of the interconnect capacitance early in the design cycle when no layout is available.

Empirical models [114] are well regarded for their simplicity, speed and accuracy. However, often these models are in agreement with the actual capacitance only for a few specific configurations. In [114] three capacitance models are given to estimate the total capacitance on a wire. These are wire-to-ground,

wire-to-wire and cross over capacitances. For the estimation of the capacitance only the first two are used in this thesis. The cross over capacitance of two wires crossing each other at a angle of 90 degrees is ignored for simplicity reasons and because its addition to the total capacitance on the wire is small.

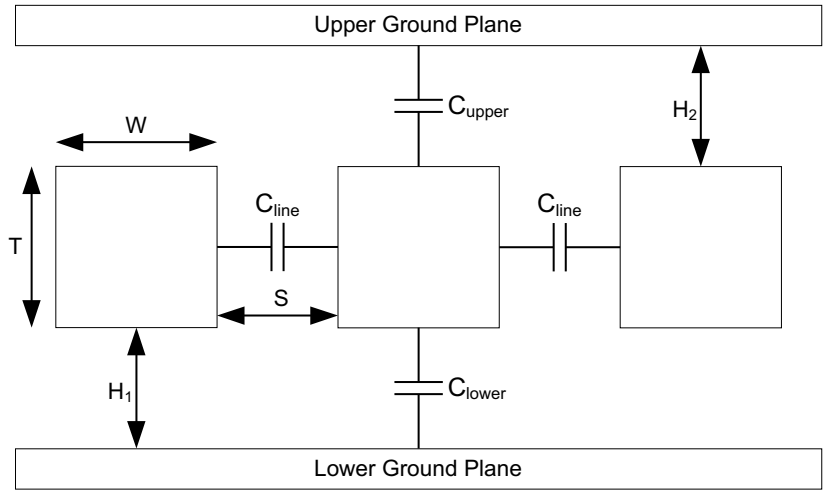


Figure 6.24: The physical definitions of the variables of the cross selection of a metal stack

With the following equations accuracies better than 10 % can be reached, see Fig. 6.24 for the definitions of the variables. The capacitance from wire-to-ground can be estimated by the following expressions [114]

$$\frac{C_{lower}}{\varepsilon} = \frac{W}{H_1} + 1.086\left(1 + 0.685e^{\frac{-T}{1.343S}} - 0.9964e^{\frac{-S}{1.421H_1}}\right) \cdot \left(\frac{S}{S+2H_1}\right)^{0.0476} \cdot \left(\frac{T}{H_1}\right)^{0.337}, \tag{6.42}$$

and

$$\begin{aligned}\frac{C_{upper}}{\varepsilon} =& \frac{W}{H_2} + 1.086\left(1 + 0.685e^{\frac{-T}{1.343S}} - 0.9964e^{\frac{-S}{1.421H_2}}\right) \\ & \cdot \left(\frac{S}{S+2H_2}\right)^{0.0476} \cdot \left(\frac{T}{H_2}\right)^{0.337}.\end{aligned} \tag{6.43}$$

The wire-to-wire capacitance is estimated by the following expression

$$\begin{aligned}\frac{C_{line}}{\varepsilon} =& \frac{T}{S}\left(1 - 1.897e^{\frac{-H}{0.31S} - \frac{-T}{2.474S}} + 1.302e^{\frac{-H}{0.082S}} - 0.1292e\frac{-T}{1.326S}\right) \\ & + 1.722\left(1 - 0.6548e^{\frac{-W}{0.3477H}}\right) \cdot e^{\frac{-S}{0.651H}},\end{aligned} \tag{6.44}$$

where

$$\begin{aligned}H &= \frac{H_1 + H_2}{2}. \\ \varepsilon &= \varepsilon_r \varepsilon_0\end{aligned} \tag{6.45}$$

The physical definitions for the variables in these equations are shown in Fig. 6.24. For the calculations of the capacitance it is assumed that the interconnect wiring is done in the lower level layers and with a minimum pitch between them. In addition, it is assumed that the metal above and below the wire are connected to a low impedance node. This results in a high capacitance, but is reasonably close to what is seen in local routing due to density requirements [111].

The total capacitance for the wire per unit of length can be estimated by

$$C_{wire} = C_{upper} + C_{lower} + 2C_{line} \tag{6.46}$$

Device capacitance

The capacitance of a device that is acting as a load to the driving gate consists of a gate oxide capacitance, overlap capacitance and junction capacitance. Since the last capacitance is commonly not dominant, it is ignored in the following calculations. The capacitance at the input of the gate is given by the following equation:

$$\begin{aligned} C_{device} &= C_{oxide} + C_{overlap} \\ &= \frac{\varepsilon_r \varepsilon_0 W L}{T_{ox}} + C_{gd_0} W \end{aligned} \tag{6.47}$$

The capacitance at one of the inputs for a 2 input NAND gate given by the following equation.

$$C_{NAND} = 4C_{oxide} + 4C_{overlap} \tag{6.48}$$

Total capacitance

The capacitance per unit of length, as given by Eqn. 6.46, times the average length of the interconnect, as given by Eqn. 6.37, gives the paracitic interconnect capacitance. Together with the device capacitance, as given in Eqn. 6.48, the load capacitance of the driving gate can be calculated. With these capacitances the dynamic power consumption of the static CMOS logic functions can be analyzed, using Eqn. 6.35.

In the following sections the dynamic power consumption of the building blocks described in Chapter 6.2 will be estimated.

6.4.2 Power consumption in CML logic

The estimation of the power consumption of CML logic is simpler than in the CMOS case, because every gate draws as a first order approximation a

constant amount of current independent of the activity and clock frequency. The variation of the tail current because of the activity on its input is normally less than 5% [81].

The effects such as the capacitive loading and the parasitics on the interconnect can be neglected for the calculation of the power consumption. These capacitances, however, do have an effect on the delay of the gate and therefore the maximum speed that can be reached. During the design of the circuit the capacitive loading of the gates must be taken into account and in case the delay is too large, a larger drive strength must be used.

Therefore, to estimate the total power consumption of a circuit, it is enough to know the number of gates that are used and their tail current. The total power consumption is then given by the total current of the gates times the power supply voltage. The power consumption of the CML DSP is estimated in Appendix A.4.

6.4.3 The power consumption estimation of the DSP

In this section the impact on the power of several implementation aspects will be analyzed for the CMOS architecture as described in Chapter 6.3 using the methods that are given in Chapter 6.4.1. In Appendix A the calculation methods for the CORDIC, poly-phase upsample FIR filter and the halfband upsample FIR filter are given.

The power consumption of the DSP is estimated for the most dominant circuits. These circuits are used in the data path of the system and have therefore a high data activity. Several other components are implemented in the DSP as well, such as configuration registers, temperature sensors and supply sensors. The configuration register is used to set frequencies, amplitudes and bias settings. The sensors are used to monitor the circuits' operation conditions. The sensor circuits are, however, not active during normal operation of the circuit and their power consumption can therefore be neglected. Other circuits that are used in the data path of the IC are circuits, such as the scaler at the output of the CORDIC, which enables the control of the signal gain, but they consume

only a small amount of power and are therefore neglected.

The power consumption numbers that are estimated are based on a typical process corner with the standard supply voltage for the technology and a temperature of 25 degrees Celsius. The spread on the power supply current as a result of the variation in the process, between the fast corner and the slow corner, can be as large as 50 % for 90nm CMOS process [115] and this number increases for more advanced technologies. In addition, the power consumption for conventional static CMOS logic is directly related to the activity factor of the circuit. This activity factor can vary depending on the signal that is applied at the input of the DSP and the frequency to which the CORDIC is tuned. The calculations that are used in this chapter assume a Gaussian input signal. This will give power numbers close to the worst case, but since the input signal of the DSP consists of a combination of many channels, the input signal can be approximated by it, see Chapter 2.4. Therefore, the calculated power consumption is only an estimation of the true power consumption. The true power is influenced by many factors that can differ chip-to-chip, such as process variation, supply voltage, ambient temperature, etc., or application-to-application, such as the modulation frequency, the applied signals, etc.

Power as a function of the sample rate

In Chapter 5.5 the required minimum sample rate was determined by the requirements on the output spectrum and the implementation complexity of the low-pass filter at the output of the DAC.

In Fig. 6.25 the estimated power consumption of the DSP is given as a function of the sample rate. The power consumption is estimated using the poly-phase upsample FIR filter that is given in Fig. 6.11 and the CORDIC of Fig. 6.20. The figure clearly shows distinctive steps in the power when the clock rate is increased. These steps are caused by the additional pipelining that is required to achieve the higher speed. When a circuit that is designed for a high clock rate, is used at a lower clock rate, it will consume more power than a circuit that is optimized for that lower clock rate, because of the additional flip-flops. The power consumption of a circuit that is optimized in 90nm CMOS at a clock

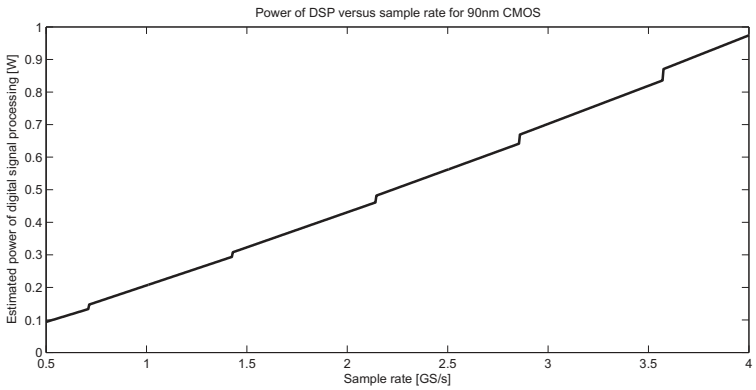


Figure 6.25: The power of the digital system as a function of the sample rate

rate of $2744MS/s$, as is determined in Chapter 5.5, is estimated to be $650mW$ and increases to almost $1W$ when the clock rate is increased to $4GS/s$.

Power as a function of the bandwidth

The designed poly-phase upsample FIR filter in Chapter 6.2.3 had a relative bandwidth of 0.15. Since this filter is implemented two times, as a complex filter, the combined relative bandwidth is equal to 0.30. With a sample rate of $2744MS/s$ this results in a usable bandwidth of about $420MHz$.

Fig. 6.10 showed the order of the filter as a function of the relative bandwidth. When the relative bandwidth of the single filter approaches 0.25 or 0.5 for the complex filter, the required order of the filter increases rapidly. This high order filter will consume more power. Therefore, it becomes more efficient at some relative bandwidth to implement two parallel filters with the corresponding CORDICs to mix these signals to different frequencies and sum the outputs. The power consumption as a function of the relative bandwidth of the complex DSP is shown in Fig. 6.26. The transition point at which two parallel implementations consume less power and become therefore more attractive is at a relative bandwidth of about 0.42, which is at about $580MHz$ signal bandwidth when the clock rate is $2744MS/s$. At a relative bandwidth of 0.78 three

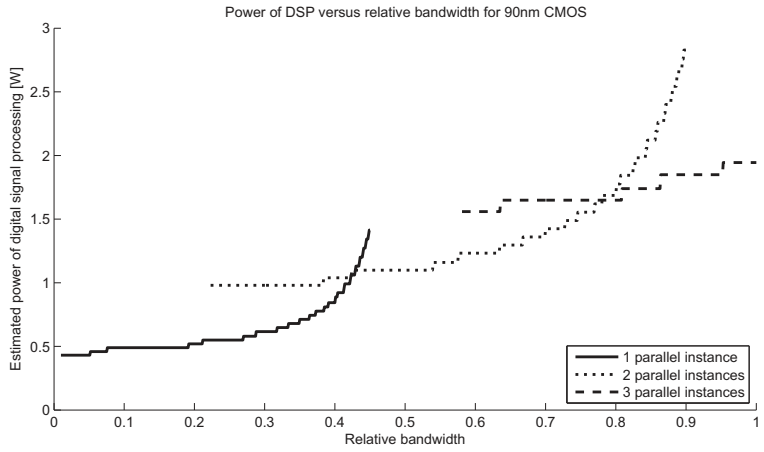


Figure 6.26: The power of the digital system as a function of the usable bandwidth

parallel implementations consume less power than two. However, this is at a signal bandwidth of $1070MHz$, which is higher than is required by the DOCSIS standard. With two parallel implementations the complete signal band from $50MHz$ to $1000MHz$ can be covered, assuming that the carriers can be placed anywhere in the band at the input of the DSP by the baseband processing.

Power as a function of the technology

Fig. 6.27 shows the power for the DSP with a signal bandwidth of $420MHz$, as determined in Chapter 6.2.3, as a function of the implementation technology, using the technology information from Table 5.2. The figure clearly shows the decreasing power when more advanced technologies are being used.

6.5 Conclusion

Compared to the conventional DOCSIS transmitter, the requirements for the clock source are reduced significantly: the large tuning range that was required

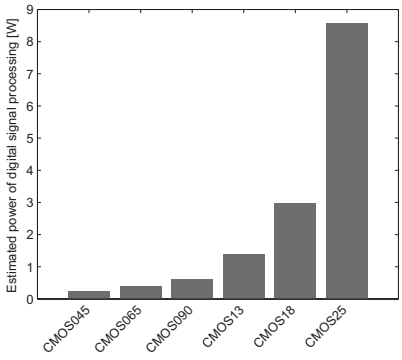


Figure 6.27: The power of the digital system for a bandwidth of $420MHz$ *as a function of the technology*

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in the conventional architecture is not needed, and the phase noise specification of the clock source is reduced by almost $9dB$.

The digital circuits that are implemented use a poly-phase upsample FIR filter to limit the clock rate at which the circuits have to operate in combination with a poly clock-phase to reduce the interference to the analog circuits as much as possible. The digital mixers are implemented as CORDICs and are also implemented in a poly-phase manner.

The expected power consumption of the DSP implemented in 90nm CMOS technology is about $650mW$ under typical conditions. The expected power consumption of the CML DSP is equal to about $1.6W$.

7

DAC analysis, design and implementation

In this chapter the functional, algorithmic and circuits aspects of a Digital-to-Analog Converter will be reviewed. Because of the many carriers that are combined in the digital domain, upconverted to the RF frequency and then converted into the analog domain with a single DAC, special emphasis will be given on the effects of the broadband signal on the signal quality reduction as a result of the physical limitations of the DAC.

7.1 DAC basics

In this chapter the subfunctions of a Digital-to-Analog Converter are given. In addition, the principle of the current steering DAC is described and the characterization methods and figures of the performance of digital-to-analog converters are defined.

7.1.1 Digital-to-Analog Converter subfunctions

Digital-to-Analog converters can be designed for applications ranging from low-speed high-resolution to high-speed low-resolution. There are many books

about this topic which describe a large variety of DAC architectures [116, 117]. For low-speed high-resolution converters commonly over-sampling converters are used, while for high-speed converters Nyquist-rate converters are often used.

The basic function of a Digital-to-Analog Converter (DAC) is to generate an analog output signal proportional to its digital input code. A basic functional diagram of a DAC is shown in figure 7.1. The digital input code consists of a number of bits.

The digital input, $d(n)$, is a discrete-time and discrete-amplitude signal. The DAC converts this signal into a discrete amplitude continues time-signal.

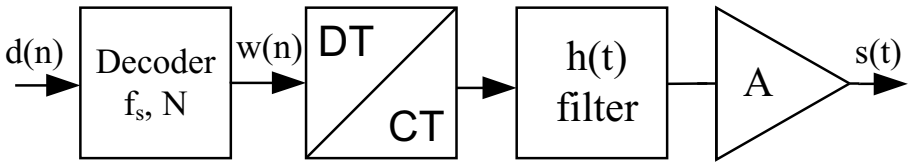


Figure 7.1: The functional block diagram of a Digital-to-Analog converter

In the time domain, the output of the DT/CT appears as a series of modulated rectangular pulses whose widths are equal to the reciprocal of the sampling (update) rate $f_s = \frac{1}{T_s}$.

$$s(t) = A \cdot h(t) \otimes \sum w(n)\delta(t - nT_s), \tag{7.1}$$

where $w(n)$ is the decoded input, $\delta(t)$ is the delta pulse, $\otimes$ stands for convolution, $h(t)$ is the pulse shaping impulse response and A is the gain. Due to the use of rectangular pulses the frequency spectrum is now modified by the sinc roll-off response $sin(x)/x$, in which zeros or nulls, appear at the sampling-rate multiples [117]. This sinc response acts as a filter that modifies the amplitude of the fundamental reconstructed signal.

DACs can be implemented in several different architectures. All the different architectures are based on the electrical quantities used: charge, voltage and current. In this thesis a current steering architecture is used, because this ar-

chitecture is fast compared to other architectures, such as resistor ladder or capacitor architectures, and does not require an output buffer, which typically limits the sample-rate and bandwidth of the latter two architectures. Some switched-capacitor DACs leave out the output buffer to increase the performance of the DAC. However, in such a configuration the output signal power becomes sample rate dependent. Hence, this requires that the DAC is designed and used at a specific sample rate which limits the flexibility.

7.1.2 Current steering D/A Converter

The basic principle of current steering DACs is the summation of currents proportional to the input word. The special case of a binary current steering converter is shown in figure 7.2. The current sources are connected in parallel. These current sources are connected to switches; the switches control whether the current can flow to the output node. The switches are controlled by the bits of the binary input code of the DAC. The output current of the DAC is therefore proportional to the input code word. The output node of the DAC is connected to a resistor. This resistor converts the output current of the DAC into a voltage.

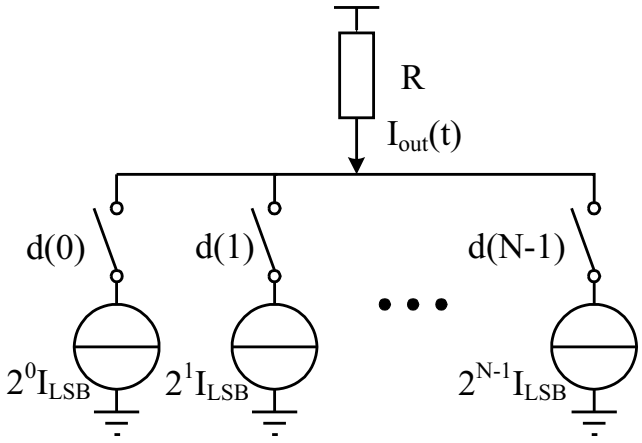


Figure 7.2: Circuit diagram of a basic binary current steering Digital-to-Analog converter

The topology of the DAC can be classified into several types

- Binary partitioned
- Thermometer partitioned
- Segmented partitioned

Other specialized topologies exist, such as sine-weighted partitioning that can be used in Direct Digital Synthesis (DDS) applications. These are outside the scope of this thesis and will not be analyzed further.

Binary partitioning

In the binary weighted current steering DAC the current sources, as shown in Fig. 7.2, are scaled according to the binary principle. This means that output current of the i^{th} current source is equal to $2^i \cdot I_{LSB}$, where I_{LSB} is the current of the Least-Significant Bit (LSB). The output of an ideal N-bit binary weighted current steering DAC is given by

$$\begin{aligned} I_{out(D)} &= 2^{(N-1)} I_{LSB} \cdot d_{N-1} + \cdots + 2 I_{LSB} \cdot d_1 + I_{LSB} \cdot d_0 \\ &= I_{LSB} \cdot D, \end{aligned} \tag{7.2}$$

where D is the digital input code given by

$$D = 2^{(N-1)} \cdot d_{N-1} + \cdots + 2 \cdot d_1 + d_0 = \sum_{m=0}^{N-1} 2^m \cdot d_m. \tag{7.3}$$

The advantage of this topology is that it is simple, for an N-bit converter there are only N current sources needed and an equal number of switches. In addition there is no need for decoding logic, all switches can be controlled directly by the input bits.

However, there are a number of disadvantages in using this topology [116]. A disadvantage is the required matching for a binary scaled converter, the Most-Significant Bit (MSB) has to be matched within $\frac{1}{2}$ Least-Significant Bit

(LSB) to the sum of all other bits. This is difficult to achieve, because of the process spread. For high resolutions, such as for 10 bits converters and beyond, these matching requirements are difficult to be guaranteed. Higher resolutions require laser trimming or self-calibration techniques [117]. Another disadvantage is because due to the large ratio between the LSB and the MSB, it is difficult to synchronize the moment of switching, especially at the mid-scale transition where all bits are being switched. Matching is an issue for all bit transitions, but the severity of the problem is proportional to the weight of the bit. This is in particular a problem for broadband signals where the probability of being close to this mid-scale is larger than for sine-wave signals, as analyzed in Chapter 2.4. Therefore the binary weighted DAC can create glitches that can severely limit the performance.

Thermometer partitioning

Another topology is the thermometer coded DAC. In this topology all the current sources have the same value. In this topology, the binary input code is first converted into a thermometer code. The thermometer code then controls the switches of the current sources.

This topology has several advantages compared with the binary weighted topology. One of the advantages is that the converter is guaranteed monotonic, because, assuming that all current sources are positive, the analog output is always increased when the digital input increases. Another advantage is that glitches are non existent. At all code steps a single 1-LSB bit transition occurs.

Thermometer code topology also has several disadvantages. For a N-bit converter $2^N - 1$ current sources are needed. This results for a high resolution converter in a lot of switches that have to be synchronized. Since the area and the power consumption of the decoder and switches increase exponentially, a full thermometer code DAC topology is seldom used for more than 10-bit resolution.

Segmented partitioning

In most DAC designs a combination of binary and thermometer code weighted elements are used. The thermometer code is used for the MSBs and the binary code for the LSBs. This is called segmentation. 0% segmentation is defined as a fully binary converter and 100% segmentation is defined as a full thermometer-code converter. An important question is the optimum point for the number of binary bits and the number of thermometer code bits. The advantages of the binary and the thermometer code DAC can be combined by choosing the segmentation. The DAC can then be optimized with respect to the performance, area, power and other aspects.

7.1.3 Performance characterization

In this work a number of static and dynamic characteristics are used to determine the performance of the DAC. A number of these characterizations are given below [118].

Static Performance

The static properties are given by the settled output values, and are often too optimistic to determine the true performance of the converter. Static performance is normally specified with four parameters; offset error, gain error, Integral Non-Linearity and Differential Non-Linearity. There are many books which define these parameters [117, 116].

The *INL and DNL* express the deviation from the straight line as shown in figure 7.3. DNL expresses how much the difference in output level between two adjacent codes deviates from the ideal LSB step Δ. The INL expresses the total deviation of an analog value from the ideal value. The ideal line is the line corrected for gain and offset errors. Several methods are used to determine this line. The first definition is the line that goes through the first and the last point. The second definition is the line that has the smallest mean square error (MSE) and the third definition is the line that results in the smallest maximum

deviation (minimax). In this thesis the straight line that goes through the first and last point will be used to determine the INL. The DNL and INL at step k

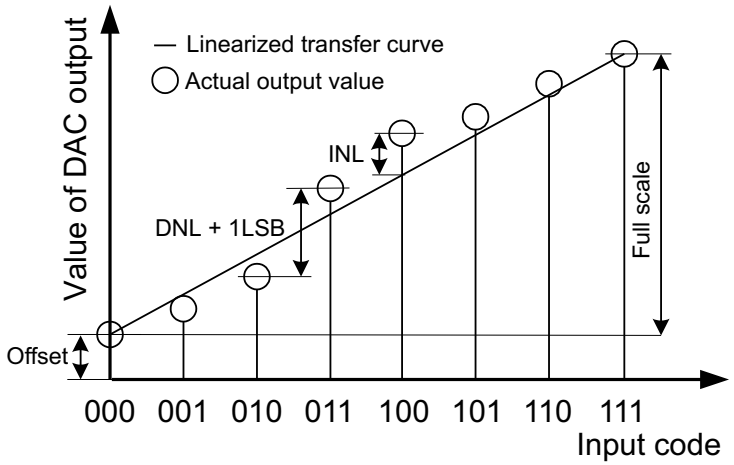


Figure 7.3: Non ideal characteristic of a DAC showing the INL and DNL for a 3 bits DAC

are defined by [118]

$$DNL_k = \frac{A_k - A_{k-1}}{a \cdot \Delta}, \tag{7.4}$$

$$INL_k = \frac{A_k}{a \cdot \Delta}, \tag{7.5}$$

where A_k is the value at step k, Δ is the LSB step and a is the input value corrected for offset and gain error.
Usually the worst case DNL and INL are given by

$$DNL = \max_{k \in 1 \ldots 2^N - 1} \{|DNL_k|\}, \tag{7.6}$$

$$INL = \max_{k \in 1 \ldots 2^N - 1} \{|INL_k|\}, \tag{7.7}$$

Single tone dynamic performance

For DACs that are used in communications systems, metrics such as INL and DNL are not sufficient to characterize the performance [119]. For DACs often

frequency domain metrics such as SFDR, THD are used. The dynamic performance is usually determined by measuring the performance while applying quantized single-tone sinusoidal inputs at several different frequencies.

A circuit implementation of a converter will suffer from non-idealities e.g. component mismatch, parasitics, limited output impedances, noise, etc. These non-idealities will distort the signal and will have an impact on the quality of the signal. In this section a number of different metrics to evaluate the quality of the signal will be given. The focus will be on performance metrics that are important for communication systems.

Spurious Free Dynamic Range (SFDR) The spurious-free dynamic range (SFDR) is the ratio between the power of the wanted signal and the power of the largest spurious (unwanted) tone within a certain frequency band, as shown in figure 7.4. SFDR is usually expressed in dB as

$$SFDR = 10 \log_{10} \left(\frac{P_s}{P_x} \right), \tag{7.8}$$

where P_s is the power of the wanted signal and P_x is the power of the largest spurious component within the considered frequency band.

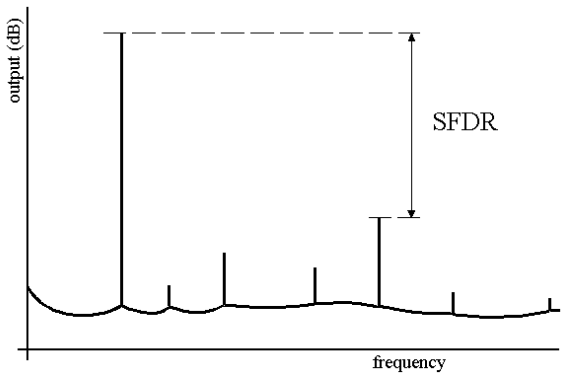


Figure 7.4: Definition of SFDR

Total Harmonic Distortion (THD) The total harmonic distortion (THD) is the ratio of the total harmonic distortion power and the power of the fundamental, i.e.

$$THD = 10 \cdot \log_{10}\left(\frac{1}{P_s}\sum_{k=2}^{\infty} P_k\right), \tag{7.9}$$

where P_k is the power of the k-th harmonic, and P_s is the power of the fundamental frequency component.

Multi-tone dynamic performance

For communication systems these single-tone metrics are also often not sufficient for the characterization of the performance. Other performance metrics are required that resemble the signals that are used in communication systems in a better way.

Intermodulation Distortion Intermodulation distortion appears when at the input a multi-tone signal is applied. The intermodulation distortion is the result of multiple signals interacting with each other in a device with a non-linear transfer function. The transfer function of a non-ideal device can be approximated by a polynomial of the order M, see Eqn. 7.10. The order determines the accuracy with which the non-linearity is modeled.

$$V_{out} = \sum_{i=0}^{M} \alpha_i V_{in}^i, \tag{7.10}$$

where α_i is the relative strength of the i-th order distortion. Often two tones are used for the input signal. Although more tones could be used to approximate the signal properties of a broadband signal better.

Second order intermodulation distortion If f_1 and f_2 are the frequencies of the two tones with both an amplitude equal to A and we assume that only

α_1 and α_2 are significant, we obtain

$$\begin{aligned} V_{out} &= \alpha_1 \left(A\sin\left(\omega_1 t\right) + A\sin\left(\omega_2 t\right)\right) + \\ &\quad \alpha_2 \left(A\sin\left(\omega_1 t\right) + A\sin\left(\omega_2 t\right)\right)^2 \qquad (7.11) \\ &= \alpha_1 A\sin\left(\omega_1 t\right) + \alpha_1 A\sin\left(\omega_2 t\right) + \\ &\quad \alpha_2 A^2 \left\{1 - \frac{1}{2}\cos\left(2\omega_1 t\right) - \frac{1}{2}\cos\left(2\omega_2 t\right) + \right. \\ &\quad \left. \cos\left((\omega_1 - \omega_2)t\right) - \cos\left((\omega_1 + \omega_2)t\right)\right\}, \qquad (7.12) \end{aligned}$$

the second order distortion products occur at

- DC
- $2f_1$,
- $2f_2$,
- $f_2 + f_1$,
- $f_2 - f_1$

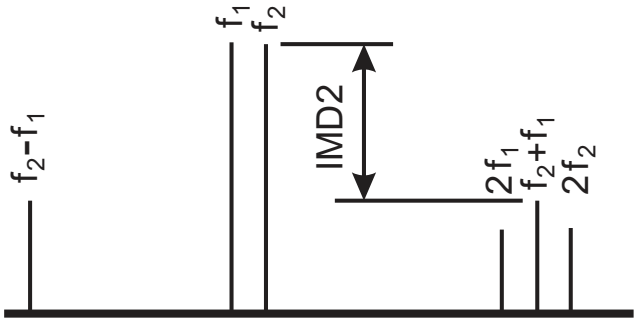


Figure 7.5: Definition of IMD2

The $IMD2$ is the difference between the power of one of the two fundamental

signals and one of the the second order $f_2 \pm f_1$ products

$$\begin{aligned} IMD2 =& 10\log_{10}\left(\frac{P_{f_2+f_1}}{P_s}\right) \\ =& 10\log_{10}\left(A^2\frac{\alpha_2}{\alpha_1}\right) \end{aligned} \tag{7.13}$$

where $P_{f_2+f_1}$ is the power level of one of the second order products and P_s is the power of one of the fundamental signals at the output. As can be observed from the last equation, when the power of the input is increased by one dB the $IMD2$ component increases by two dB.

Third-order intermodulation distortion If f_1 and f_2 are the frequencies of the two tones with amplitude A and we assume that the first three terms α_1, α_2 and α_3 are significant.

$$V_{out} = \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3, \tag{7.14}$$

$$\begin{aligned} V_{out} =& \alpha_1 A\left(\sin\omega_1 t + \sin\omega_2 t\right) + \\ & \alpha_2 A^2\left(\sin\omega_1 t + \sin\omega_2 t\right)^2 + \\ & \alpha_3 A^3\left(\sin\omega_1 t + \sin\omega_2 t\right)^3 \end{aligned} \tag{7.15}$$

Then the third order distortion products occur at

- $2f_2 - f_1$,
- $2f_1 - f_2$,
- $2f_1 + f_2$,
- $2f_2 + f_1$,
- $3f_1$,
- $3f_2$

When the two tones are spaced closely together, then especially the first two components are of importance because unlike the 2^{nd} order distortion these

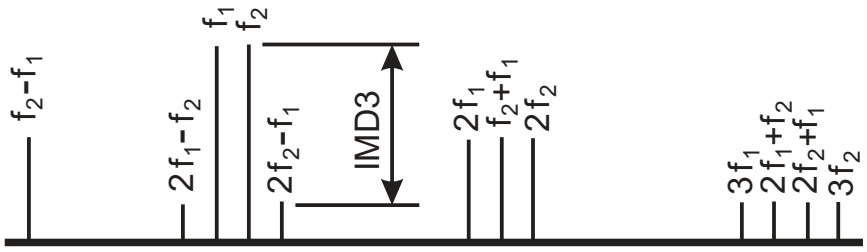


Figure 7.6: Definition of IMD3

components are in close proximity of the original signals. When we assume that the power of the two signals is equal than the IMD3 is the difference between the power of one of the two fundamental signals and one of the the third order $2f_2 - f_1$ and $2f_1 - f_2$ products

$$\begin{aligned} IMD3 =& 10\log_{10}\left(\frac{P_{3x}}{P_s}\right), \\ =& 10\log_{10}\left(\frac{\frac{3}{4}A^3\alpha_3}{A\alpha_1 + \frac{9}{4}A^3\alpha_3}\right) \end{aligned} \tag{7.16}$$

where P_{3x} is the power level of one of the third order products and P_s is the power of one of the fundamental signals at the output. When the distortion is mild then $\alpha_3 \ll \alpha_1$, which results in a three dB rise of the IMD3 when the power of the signal is increased by one dB.

Composite Second Order (CSO) and Composite Triple Beat (CTB) When more than two tones interact with each other in a non-linear system, Composite Second Order (CSO) and Composite Triple Beat (CTB), describe the intermodulation performance. These parameter take into account the fact that the distortion generation process with a large number of signals create multiple contributors to the second order and third order impairments. This is especially true in cable television systems where the carriers are placed at regular distance from each other e.g. $6MHz$.

With such a regular spaced input signal, the CSO is the vector sum of all the 2^{nd} order intermodulation products at a certain location in the band of inter-

est. The same applies to CTB but instead for the 3^{rd} order intermodulation products. The number of CSO and CTB products increases fast with the number of signals that are combined. For the case of equally spaced carriers, a simple expression can be used to estimate the number of third order beats on any channel [120].

$$\#beats = (N-1)^2/4 + (N-M)(M-1)/2 - (N/4), \tag{7.17}$$

where N is the number of carriers and M is the carrier being measured. The number of beats at the band edges, $M = 1$ and $M = N$, is 2/3 of the number of beats in the middle, $M = N/2$ of the band. This number is independent of the number of channels.

Adjacent Channel Leakage Ratio ACLR [1] is an important parameter in transmitter specifications. It is defined as the ratio of the power in the adjacent channel to the power in the wanted channel,

$$ACLR = 10log_{10}\left(\frac{P_{adjacent}}{P_{wanted}}\right). \tag{7.18}$$

Intermodulation products, such as adjacent channel power ratio (ACLR) and error vector magnitude (EVM) are important figures of merit for linearity. The adjacent channel leakage is harmful for the system, because it disturbs neighboring channels, causing reduced SNR in those channels which makes retrieving the information more difficult. Since two neighboring channels have no correlation, the interference from the neighbor channel can be assumed to be stochastic in nature.

EVM can be considered as a FOM for its own transmitted fundamental signal. The EVM describes the distortion of the channel caused by the components involved.

From the transmitter point of view EVM is usually an easier metric to handle than ACLR. In most systems in which the ACLR requirements are met the

[1] also called Adjacent Channel Power Ratio (ACPR)

EVM specifications are fulfilled if the transmitter meets those requirements. In systems where many constellation points lie close to the maximum amplitude, however, the ACLR can be met but the EVM does not comply to the required specifications [121]. An example of such a system is GSM-EDGE. However, in the DOCSIS transmitter the constellation points are distributed evenly; therefore, this approximation can be used.

The DOCSIS standard defines the ACLR up to a distance of four channels, see Chapter 3.2.2 and the specification stays constant beyond the four channels.

Although for the DOCSIS standard, and many others, the ACLR is the main specification for the performance of the transmitter, it is difficult to perform circuit simulations to estimate this specification with sufficient accuracy. The biggest obstacle is the length of the test pattern that is required, in order to have reliable results. This is caused by the wide band properties of the input signal of which the performance is being characterized. It has a near Gaussian characteristic which results in a large peak-to-average power ratio. However, those peaks are only occurring occasionally, resulting in long test patterns. In order to achieve realistic properties of the input signal, the test patterns should be several 1000's of symbols long, with symbol rates of 5.36MSym/s this results in test pattern times of 100's of μs, while 100's of ns are possible with reasonable simulation times[2].

Digital-to-analog converters are typically characterized using single or two tone signals. The main reason for these sinewave signals is the ease to analyze these signals. They also provide a standard test method that can be used to characterize and compare devices among each other. However, these sinewave signals often do not represent the 'real world' modulated signals that are converted in a DAC when used in the application.

Sinewave signals and modulated signals have some important differences that affect the behavior of the DAC. Because sinewave signals consist of single tones, the signal has no bandwidth, whereas modulated signals have their signal energy spread over a frequency range. When the DAC adds distortion to the signal in the form of harmonics, the lack of bandwidth in the sinewave signal

[2] 100's of ns with a C-extracted model of the DAC core takes about one to two days of simulation time depending on the level of details on a 3GHz Intel Xeon processor

results in harmonics that are placed at distinct frequency locations, whereas for modulated signals the second order distortion has a bandwidth of twice that of the original signal and the third order distortion has triple this bandwidth etc. This spreading in bandwidth reduces the level of the harmonics.

In addition, these modulated signals often have variations in their amplitude level. To prevent clipping of the signal the average amplitude level must be reduced as described in Chapter 2. In general, the distortion of the signal increases when the signal power is increased. For a general RF device the third order harmonic products increase three times as much as the signal power increases. Therefore, the lower average signal level of the modulated signal results in a reduction of the average distortion. However, for a DAC this relation does not always hold. For DACs that are full binary or DACs that have a low number of thermometer bits, the INL/DNL at the mid-code transition can be large. When a sinewave is being converted into an analog signal, this mid-code transition occurs twice per period. A broadband signal signal, however, is most of its time around this mid-scale code and crossings of this value happens often. Reducing the amplitude of the signal does not reduce the likelihood of crossing this value. Therefore the energy in the distortion products stays constant, but the signal amplitude is reduced, thereby increasing the relative distortion metrics.

7.2 Signal quality in case of DAC imperfections

In this chapter a number of imperfections of a Digital-to-Analog Converter will be discussed. DAC limitations stem from various causes. The number of error mechanisms that are present is very high. These mechanisms cause reduced performance at the output of the Digital-to-Analog Converter, such as reduced linearity, interference and reduced signal frequencies.

The performance that is required is determined by the application. Depending on the application some error mechanisms have more impact than others. For example, video DACs require excellent performance in the time domain, in or-

der to achieve high quality images, whereas for communication DACs linearity in the frequency domain is often the most important specification.

The architecture and topology of the DAC has a large influence on which error mechanisms are important and dominant. For example, the level of segmentation of the binary and thermometer coded DAC have an influence on the static differential non-linearity.

The DAC is designed such that it complies with specifications which are defined by the application. Examples of specifications for a DAC are resolution, accuracy, conversion rate, dynamic range and operating conditions.

7.2.1 Noise by quantization

Although quantization noise is not an imperfection of the DAC itself, as the signal is already quantized at the input of the DAC, it does affect the signal quality. The SNR of a full-scale sinusoid is given by the well known equation

$$SQNR = 6.02b + 1.76 \ \ [dB] \tag{7.19}$$

where b is the number of bits. When the signal is not a full-scale signal, as is often required to prevent clipping of the broadband signal, the SQNR becomes

$$SQNR = 6.02b + 1.76 - 10\log_{10}(PAPR) \ \ [dB] \tag{7.20}$$

where $PAPR$ is the peak-to-average power ratio as defined in Chapter 2.4. Increasing the sample rate of the signal while keeping the bandwidth of the signal constant improves the SNR by

$$10\log_{10}\left(\frac{f_s}{2f_{BW}}\right) \ \ [dB] \tag{7.21}$$

where f_s is the sample rate and f_{BW} is the bandwidth of the signal.

In the DOCSIS standard the ACLR is given as main specification. When we assume that the noise spectral density (nsd) is flat over the frequency range, the ACLR due to the quantization can be calculated by

$$ACLR = 6.02b + 1.76 + 10\log_{10}\left(\frac{f_s}{f_{BW}}\right) - 10\log_{10}\left\{PAPR(N)\right\} \ \ [dB] \quad (7.22)$$

The ACLR requirements, as described in Chapter 3.2.2, is given as

$$ACLR_{req}(N) > 73 - 10\log_{10}(N) \ \ [dB] \quad (7.23)$$

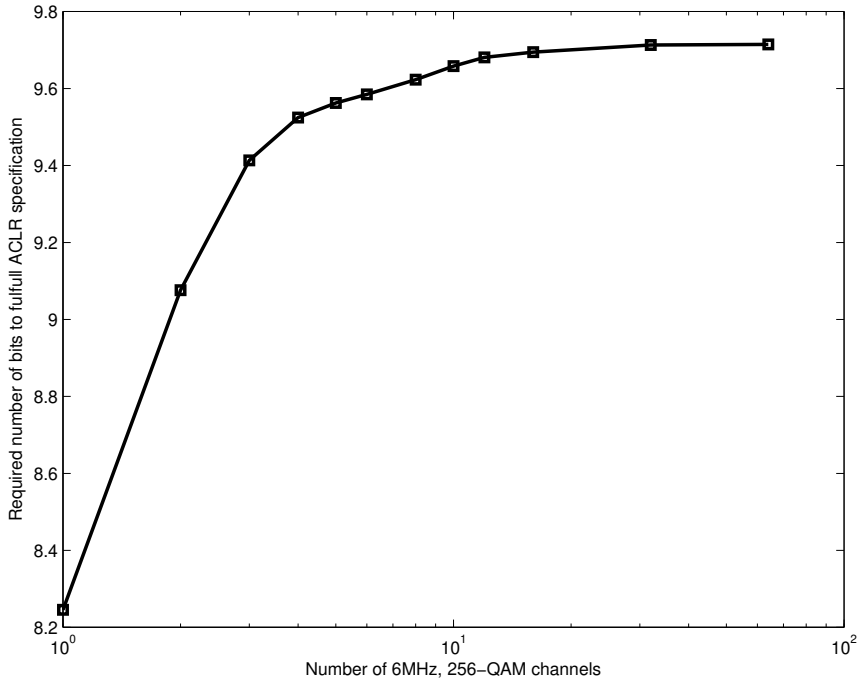


Figure 7.7: Simulation of the required number of bits due to quantization noise as a function of the number of channels

Because the requirements for the ACLR decreases proportionally to the increase of the ACLR due to the increasing number of carriers, the number of bits that

are required is independent of the number of carriers. However, the PAPR does depend on the number of carriers, especially for a low number of carriers. In Fig. 7.7, the required number of bits is shown as a function of the number of carriers. Taking into account the sample rate of $2744MS/s$ as defined before. As can be observed, from about 10 carriers the required resolution does not increase anymore with the number of carriers.

7.2.2 Amplitude error by output impedance

The finite impedance of the current sources causes code dependent variation of the output impedance of the DAC. The signal dependent variation introduces non-linear distortion in the current steering DAC. Non-linearities caused by output impedance variations have been analyzed previously in [122, 123, 124, 125].

To meet signal quality requirements, the output impedance should be larger than a certain minimum value. Since for the single-ended DAC, the INL curve, due to the finite output impedance, is even, the even harmonics will dominate. For the differential circuit the third harmonic will dominate. The output impedance requirements for a fully differential DAC are reduced by over an order of magnitude relative to the requirements for a single-ended DAC [125]. However, any imbalance in the circuit will cause a second harmonic. This imbalance can be caused by design imperfections or due to mismatch of the components involved. Here we will consider only differential DACs, because these are commonly used for high performance applications.

Single tone SFDR consequences

The single tone performance can be derived by considering a simple model of a DAC, as shown in Fig. 7.8. Each current source of the DAC with N elements has a certain output impedance z_o. Let a single unit of a full thermometer coded DAC have impedance Z_{on} when the switch is conducting and impedance Z_{off} when the switch is open. As Z_{on} and Z_{off} will be different, the impedance at the output of the DAC will vary depending on the code applied to the DAC.

Non linear distortion is generated, because this output impedance is signal dependent.

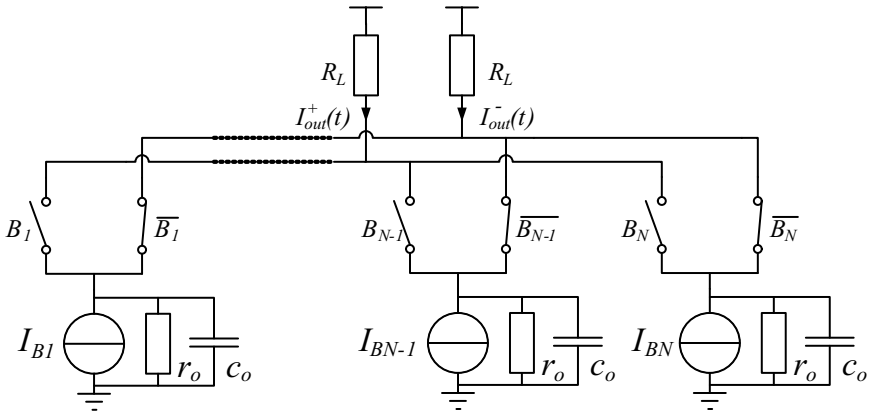


Figure 7.8: Digital to Analog Converter with non-ideal current sources

Equations can be derived for the harmonic distortion HD2 and HD3. In this section it is assumed that the third harmonic is dominant for the SFDR for the differential DAC and the HD2 is being canceled by the differential nature of the DAC.

Fig. 7.8 shows the unit current cell with the output impedance r_o and c_o indicated. The impedance Z_{imp} can be calculated as

$$Z_{imp} = r_o(1 + g_o(r_o//c_o)) \tag{7.24}$$

$$= r_o(1 + g_o r_o)\left[\frac{1 + \frac{j\omega c_o}{g_o}}{1 + j\omega c_o r_o}\right] \tag{7.25}$$

The number of switches that conduct at a certain time when a full scale sinewave signal is applied is given by

$$S(t) = N\left[\frac{1 + \sin(\omega t)}{2}\right], \tag{7.26}$$

where N equals the total number of switches. The output impedance of the DAC is then given by the load resistor in parallel with the output impedances of the current sources that are turned on at a certain moment. The single ended output voltage will then be

$$V_{out}(t) = \frac{N(1+\sin(\omega t))I_{LSB}}{2g_L + g_{imp}N(1+\sin(\omega t))}, \tag{7.27}$$

The single-ended SFDR requirements are given as [124]

$$Z_{imp,req} = \frac{1}{4}NR_L 20\log_{10}(SFDR). \tag{7.28}$$

A similar analysis can be made for the differential output of a current steering DAC. The output voltage of the differential DAC is given by

$$V_{out,diff} = \frac{4NIo\,x g_l}{(2\,g_l + g_o\,Nx + g_o\,N)\,(-2\,g_l - g_o\,N + g_o\,Nx)} \tag{7.29}$$

where $g_o = 1/Z_{imp}$, $g_l = 1/R_L$ and I is the unit cell current. The Taylor expansion of the above equation gives

$$V_{out} = \alpha_0 + \alpha_1\,\sin(\omega\,t) + \alpha_2\,(\sin(\omega\,t))^2 + \alpha_3\,(\sin(\omega\,t))^3 + \cdots \tag{7.30}$$

Applying goniometric relations and combining the corresponding terms gives [124]

$$\begin{aligned} V_{out} &= \alpha_1 + \frac{1}{2}\alpha_2 + \frac{3}{8}\alpha_4 \\ &+ \left(\alpha_2 + \frac{3}{4}\alpha_3\right)\sin(\omega\,t) \\ &- \left(\frac{1}{2}\alpha_2 + \frac{1}{2}\alpha_4\right)\cos(2\omega\,t) \\ &+ \left(\frac{1}{4}\alpha_3\right)\sin(3\omega\,t), \end{aligned} \tag{7.31}$$

where

$$\alpha_1 = -4\,\frac{N\,Io\,g_l}{(2\,g_l + g_o\,N)\,(-2\,g_l - g_o\,N)}, \tag{7.32}$$

$$\alpha_2 = 0, \tag{7.33}$$

$$\alpha_3 = -4\,\frac{N^3\,Io\,g_l\,{g_o}^2}{(2\,g_l + g_o\,N)^3\,(-2\,g_l - g_o\,N)}, \tag{7.34}$$

$$\alpha_4 = 0. \tag{7.35}$$

The SFDR of the differential DAC, assuming that the third order distortion is dominant for the differential DAC, is given by the ratio of the coefficients $\sin(\omega\,t)$ and $\sin(3\omega\,t)$.

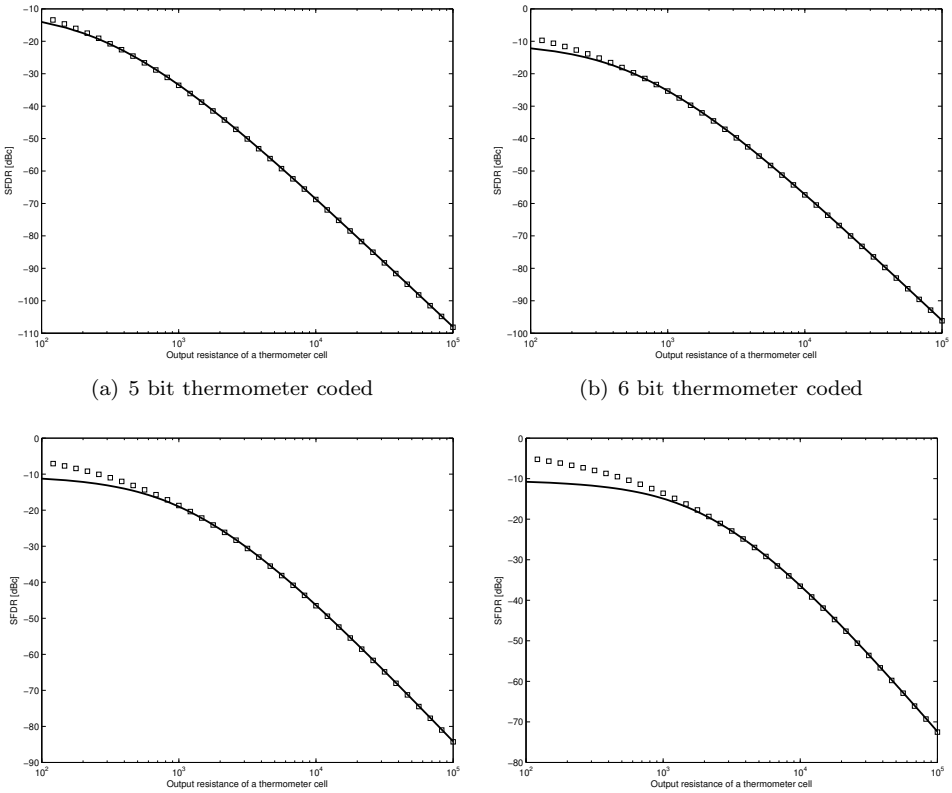
$$SFDR_{diff} = 20\log_{10}\left(\frac{N^2{R_L}^2}{16\,{Z_{imp}}^2 + 16\,Z_{imp}\,N R_L + 7\,N^2{R_L}^2}\right) \tag{7.36}$$

The required impedance for a given resolution can be easily determined from above equation. The SFDR is plotted in Fig. 7.9 for different levels of segmentation as a function of the current source resistance, with a load resistor of 25Ω. As can be observed from the figure, when many thermometer sources are used and the current source resistor is low, the assumption that the third order products are the only contributors to the SFDR does not hold anymore. For these conditions higher order products should be taken into account, although for normal operation conditions these higher order products are not significant.

Two tone IMD3 consequences

In narrow band communication systems, IMD3 is often the only significant spurious component that will fall inband. The IMD3 is therefore an important FOM for a DAC.

The impedance requirement for the IMD3 can be derived similar to the analysis given for the SFDR in the previous section. The signal has two tones of equal amplitude instead of the single tone that is used for the SFDR and is given by



(a) 5 bit thermometer coded

(b) 6 bit thermometer coded

(c) 7 bit thermometer coded

(d) 8 bit thermometer coded

Figure 7.9: The calculated (solid line) and simulated (squares) results of the SFDR for several levels of segmentation

$$x(t) = \sin(\omega_1 t) + \sin(\omega_2 t) \tag{7.37}$$

Using the same Taylor expansion Eqn. 7.30 as in the previous section, where the coefficients are given in Eqn. 7.32 - 7.35, the fundamental and third order component have an amplitude [11]

$$\begin{aligned} Fundamental &= \alpha_1 + \frac{9}{4}\alpha_3, \\ Third\ order\ distortion &= \frac{3}{4}\alpha_3. \end{aligned} \tag{7.38}$$

The ratio between these two gives the third order distortion component IMD3 [125].

$$IMD3 = 1/3\,\frac{16\,{g_l}^2 + 16\,g_l\,g_o\,N + 13\,N^2{g_o}^2}{N^2{g_o}^2} \tag{7.39}$$

The required impedance for a given resolution and IMD3 can be easily determined from above equation.

Wideband ACLR consequences

While the IMD3 is often the most important linearity specification for narrow band signals, for wideband signals the ACLR is often the most leading specification. The relation between the IMD3 and the ACLR is given in Chapter 7.1.3. The two most important differences are the spectral widening of the harmonics and the changes in the probability density function of the multi-carrier signal.

To take into account the reduced average amplitude of the wideband signal, the variable A is added to Eqn. 7.24

$$S(t) = N\left[\frac{1 + Ax(t)}{2}\right], \tag{7.40}$$

where N equals the total number of thermometer sources and $x(t)$ is the wideband signal. The output impedance of the DAC is then given by the load resistance in parallel with the number of thermometer sources that are turned on at a certain moment in time. The differential output voltage becomes equal to

$$V_{out,diff} = -4\,\frac{N\,Io\,Ax\,(t)\,g_l}{(2\,g_l + go\,N\,Ax\,(t) + g_o\,N)\,(-2\,g_l - g_o\,N + g_o\,N\,Ax\,(t))} \quad (7.41)$$

where $g_o = 1/r_o$, $g_l = 1/R_L$ and I is the unit cell current. The Taylor expansion of the above equation and applying goniometric relations and combining the corresponding terms gives the factors for Eqn. 7.30 as

$$\begin{aligned}
\alpha_1 &= -4\,\frac{N\,Io\,A g_l}{(2\,g_l + g_o\,N)\,(-2\,g_l - g_o\,N)}, && (7.42)\\
\alpha_2 &= 0, && (7.43)\\
\alpha_3 &= -4\,\frac{N^3\,Io\,A^3 g_l\,{g_o}^2}{(2\,g_l + g_o\,N)^3\,(-2\,g_l - g_o\,N)}, && (7.44)\\
\alpha_4 &= 0. && (7.45)
\end{aligned}$$

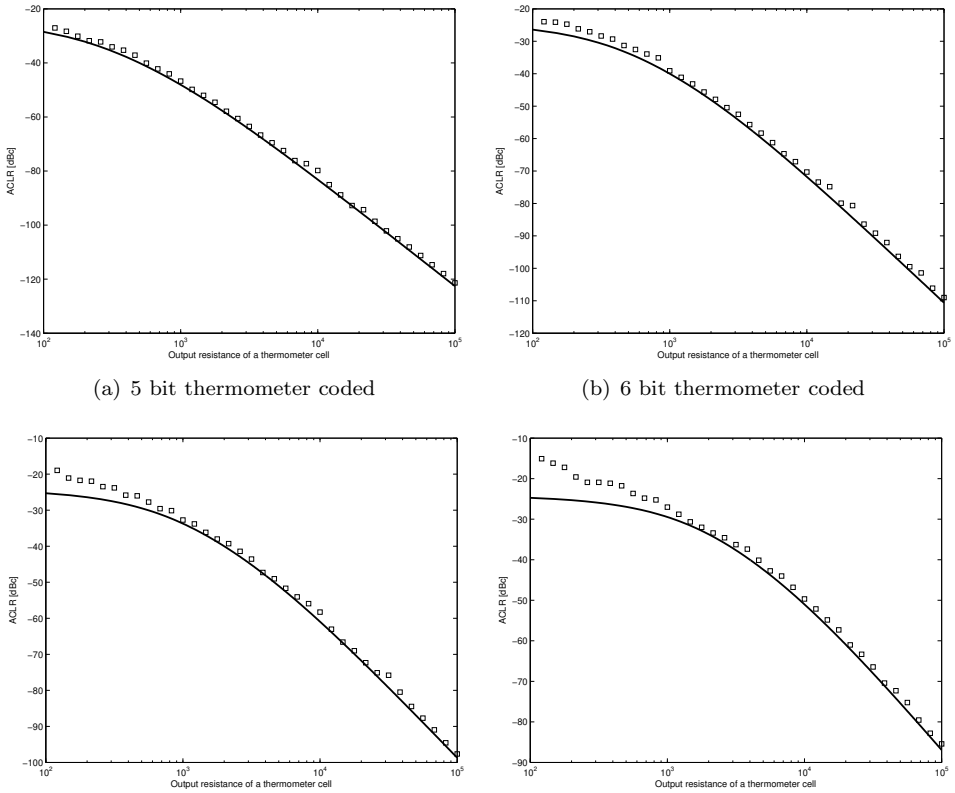
Assuming that the third order distortion is dominant for the ACLR, the ACLR is given by the ratio of the third order component and the fundamental as Eqn. 7.38.

$$ACLR = \int_{-A_{clip}}^{A_{clip}} D(x) pdf(x) dx, \quad (7.46)$$

where $D(x)$ is the third order distortion at the amplitude x. Assuming a large number of carriers, the probability density function (pdf) of the amplitude is approximated by the Gaussian distribution as is shown in Chapter 2.4.5. When the clip level is normalized to unity and symmetric around zero, the ACLR is given by

$$ACLR(g_o) = \frac{3\sqrt{2}}{\sqrt{\pi\,\sigma^2}} \int_0^1 \frac{N^2 x^2 {g_o}^2 e^{-\frac{x^2}{2\sigma^2}}}{16\,{g_l}^2 + 16\,g_l\,g_o\,N + 4\,{g_o}^2 N^2 + 9\,N^2 x^2 {g_o}^2} dx \quad (7.47)$$

In Fig. 7.10 the ACLR as a function of the resistance of the current source is



(a) 5 bit thermometer coded

(b) 6 bit thermometer coded

(c) 7 bit thermometer coded

(d) 8 bit thermometer coded

Figure 7.10: The calculated (solid line) and simulated (squares) results of the ACLR for several levels of segmentation for a 12-bits converter

drawn for a number of segmentations. Taking into account the Gaussian pdf of the wideband signal and a clipping level of $12dB$ above the rms level of the signal, which results in occasional clipping of the signal, as shown in Chapter 2.4.2, the σ becomes equal to about 0.25. The solid line is the calculated results using the equation above and the squares are the simulated results.

As can be observed when comparing the results of the narrowband performance and the wideband performance graphs, when the DAC performance is affected by output conductance, a higher output conductance is allowed to achieve a similar performance for wideband signals than for a narrowband signal.

At low resistance the simulations show worse results than than the calculated results, this is mainly caused by the restriction in the calculation that only the third order distortion is taken into account. At such high level of distortion also the higher order distortion products, such as the fifth, should be taken into account. However, for normal operating conditions these higher order distortion products are not significant.

7.2.3 Amplitude error by current source mismatch

In an actual implementation of a DAC the current sources will differ from their designed values due to the mismatch errors. In current steering DACs current source mismatch based errors tend to be dominant at relatively low signal frequencies.

Since every bit has its designed amplitude and its mismatch, the output signal amplitude depends on which bits are being turned on at a certain moment. This will result in a signal dependent output error.

The matching errors of a current source can be modeled as an additional current source, δI, in parallel with the nominal current source, $\tilde{I}$, as shown in Fig. 7.11.

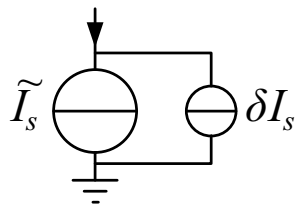
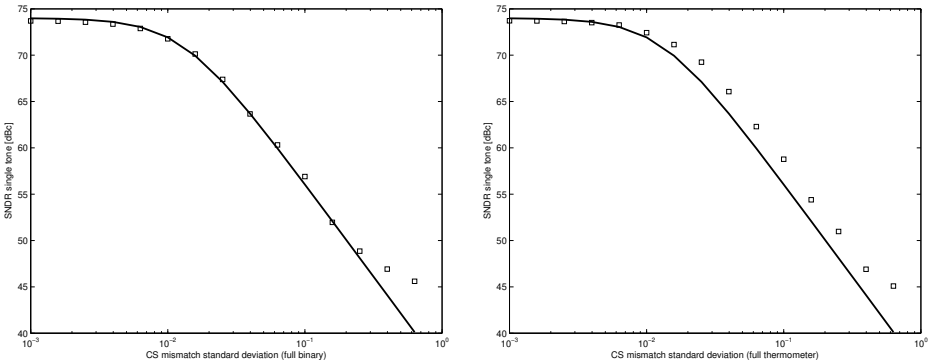


Figure 7.11: Model for the mismatch of the current source

Single tone SNDR consequences

Mismatch in the current sources amplitudes creates distortion in the output signal of the DAC. An ideal N-bit DAC will have $2^N - 1$ identical current



(a) Full binary coded DAC (b) Full thermometer coded DAC

Figure 7.12: The calculated (solid line) and simulated (squares) results of the SNDR for the full binary coded DAC and the thermometer coded DAC

sources grouped according to its coding. In a non-ideal DAC there will be mismatch between equally designed current sources caused by process spread. This mismatch between those current sources will result in signal dependent distortion. The analysis for sinusoidal signals is given in [126]. When the mismatch is assumed to be uncorrelated and Gaussian distributed, then the SNDR of an N-bit binary converter for a full scale sinusoidal signal can be shown to be [126]

$$SNDR \approx 6N + 1.76 - 10\log\left(1 + 6\sigma_{\Delta I/I}^2 2^N\right), \tag{7.48}$$

where $\sigma_{\Delta I/I}$ is the spread of the normalized current source error. The calculated (line) and simulated (squares) SNDR of a single tone for a 12 bits converter as a function of the current source mismatch is shown in Fig. 7.12

Wideband ACLR consequences

The SNDR for a wideband signal can be calculated by using a similar analysis as is given in [126] for sinusoidal signals.

The assumption is made that the ideal output current is given by $\overline{I_s}$, as shown

in Fig. 7.11, and each current source has a matching error of δI_s. The actual output current for each unit current source becomes

$$I_s = \tilde{I_s} + \delta I_s, \tag{7.49}$$

the relative matching of the current source is equal to

$$\varepsilon_s = \frac{\delta I_s}{\overline{I_s}}. \tag{7.50}$$

The matching errors are assumed to be Gaussian distributed with zero mean. The variance of the thermometer bit is

$${\sigma_s}^2 = E_\delta \left\{ {\delta I_s}^2 \right\} = {I_s}^2 \cdot {\sigma_s}^2. \tag{7.51}$$

The absolute error for the thermometer bit is δI_s. The total output current is given by the contribution of all bits

$$\begin{aligned} I(X) &= \sum_{s=0}^{2^N-1} I_s \cdot b_s && (7.52)\\ &= \sum_{s=0}^{2^N-1} \left(\tilde{I_s} + \delta I_s \right) \cdot b_s && (7.53)\\ &= \tilde{I_T} \cdot X + \sum_{s=0}^{2^N-1} \delta I_s \cdot b_s && (7.54) \end{aligned}$$

The absolute error current is equal to

$$\Delta I(X) = \sum_{s=0}^{2^N-1} \delta I_s \cdot b_s \tag{7.55}$$

The variance of the error current is

$$\sigma_{\Delta I(X)}{}^2 = E_\delta \left\{ |\Delta I(X)|^2 \right\} \tag{7.56}$$

$$= E_\delta \left\{ \left| \sum_{s=0}^{2^N-1} \delta I_s \cdot b_s \right|^2 \right\} \tag{7.57}$$

$$= \sum_{s=0}^{2^N-1} E_\delta \left\{ [\delta I_s \cdot b_s]^2 \right\} \tag{7.58}$$

Since b_s is 0 or 1, we have that $b_s^2 = b_s$

$$\sigma_{\Delta I(X)}{}^2 = \sum_{s=0}^{2^N-1} E_\delta \left\{ |\delta I_s|^2 \right\} \cdot b_s \tag{7.59}$$

$$= \overline{I_s}^2 \cdot \sigma_s{}^2 \cdot \sum_{s=0}^{2^N-1} b_s \tag{7.60}$$

$$= \overline{I_s}^2 \cdot \sigma_s{}^2 \cdot X \tag{7.61}$$

The mismatch errors are assumed to be uncorrelated, the average value of the squared current is

$$E_\delta \left\{ [I(X)]^2 \right\} = [I_s \cdot X]^2 + E_\delta \left\{ [\Delta I(X)]^2 \right\} \tag{7.62}$$

using equation 7.56

$$E_\delta \left\{ [I(X)]^2 \right\} = [I_s \cdot X]^2 + I_s{}^2 \cdot \sigma_s{}^2 \cdot X \tag{7.63}$$

The code averaged squared value for the expression in 7.63 is

$$\overline{E_\delta \left\{ |I(X)|^2 \right\}} = I_s^2 \cdot \overline{X^2} + I_s{}^2 \cdot \sigma_s{}^2 \cdot \overline{X} = I_s^2 \cdot \overline{X^2} + I_s{}^2 \cdot \sigma_s{}^2 \cdot X_{DC} \tag{7.64}$$

where $\overline{X} = X_{DC} = 2^{N-1}$ is the average input value and is set to the mid scale value. The average error power is equal to

$$P_e = \overline{I_s}^2 \cdot \sigma_s^2 \cdot 2^{N-1} \tag{7.65}$$

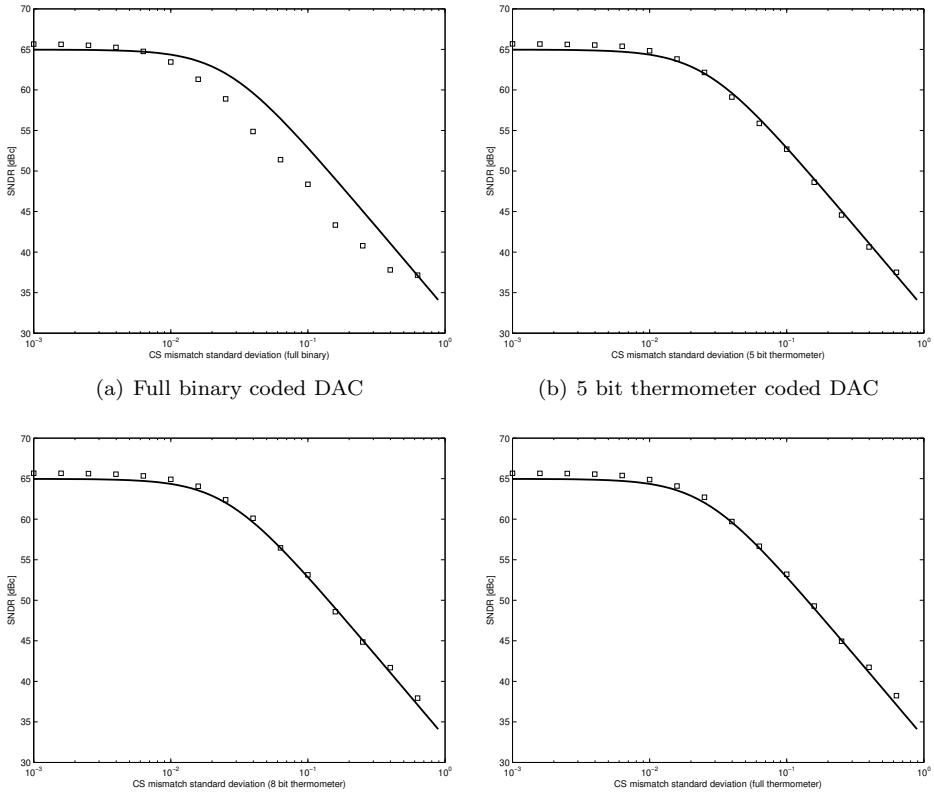
Assume that the input signal is given by $Ax(t)$, where A is the amplitude of the ac signal. The signal power is then equal to

$$\begin{aligned} P_s &= \overline{I_s}^2 \cdot \overline{X^2} = I_s^2 \cdot \overline{(2^{N-1} + Ax(t))^2} && (7.66) \\ &= \overline{I_s}^2 \cdot \left(2^{2N-2} + A^2\overline{x(t)^2}\right) && (7.67) \end{aligned}$$

The SNDR can be found by taking the ratio of the signal power and the matching plus noise error power. Assuming a large number of carriers, the pdf of the amplitude is approximated by the Gaussian distribution as is shown in Chapter 2.4.5. When the clip level is normalized to unity, the SNDR is given by

$$SNDR(\sigma) = \int_0^1 \frac{3x^2 2^{2N-1}}{1 + 3\sigma_s^2 2^{N-1}} \frac{e^{-\frac{x^2}{2\sigma_{pdf}^2}}}{\sqrt{2\pi\sigma_{pdf}^2}}\, dx \qquad (7.68)$$

Because of the large peak amplitude levels that are possible when many carriers are combined, clipping has to be taken into account. In Fig. 7.13 the result of Eqn. 7.68 is shown with a clipping level of $12dB$ above the rms level of the signal, i.e. $\sigma_{pdf} \approx 0.25$, which results in occasional clipping of the signal, as shown in Chapter 2.4.2. The figure shows that the above equation does not accurately predict the SNDR for low levels of segmentation, e.g. < 4 bit thermometer coded. For DACs that are full binary or DACs that have a low number of thermometer bit, the INL/DNL at the binary/thermometer bit transitions can be large. When a sinewave is being converted into an analog signal, the mid-code transition occurs twice per period. However, a broadband signal signal is the most of its time around the mid-scale code and the crossings of this value occurs often. The relative low average amplitude of the signal does not reduce the likelihood of crossing this value. When a higher segmentation is used the binary/thermometer bit transition glitch decreases and are more uniformly distributed over the code range. Thereby reducing the impact of these transitions on the performance.



(a) Full binary coded DAC

(b) 5 bit thermometer coded DAC

(c) 8 bit thermometer coded DAC

(d) Full thermometer coded DAC

Figure 7.13: The calculated (solid line) and simulated (squares) results of the SNDR for various levels of segmentation

7.2.4 Timing error by relative timing precision

The moment the current of a unit element is switched from one output to the other output is synchronized by a global clock and this moment should match to the moment of switching of the other units. However, due to mismatch in the switches, latches or buffers, the switching moment of a unit can differ with respect to the expected moment. In Fig. 7.14a a DAC output with and without a timing error is shown. These timing errors result in a charge error in the output, as is shown in Fig. 7.14b. The magnitude of the timing error pulse is determined by the number of bits that change state at a certain moment,

which is given by the difference between successive input codes

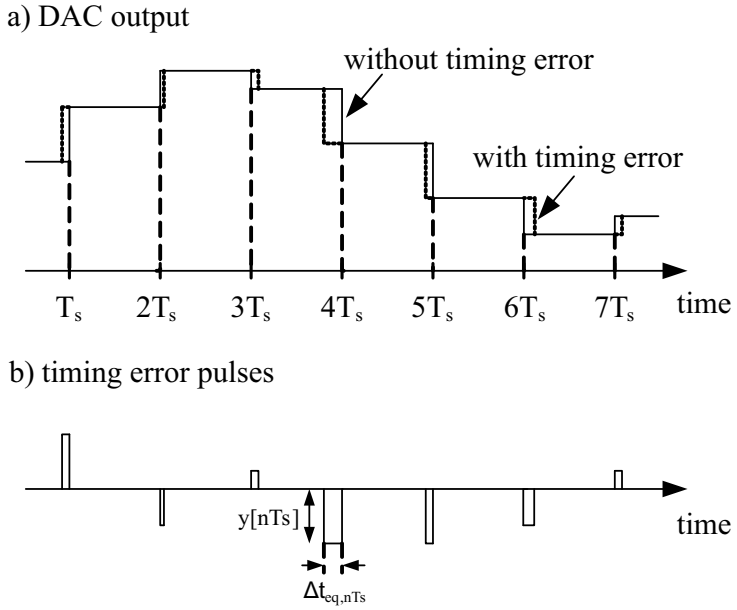


Figure 7.14: The DAC output with and without timing error and the corresponding timing error pulses

$$\Delta w[nT_s] = w[nT_s] - w[(n-1)T_s], \tag{7.69}$$

where $w[\cdot]$ is the input data of the DAC and T_s is the clock period. The duration of the timing error pulse, which is called equivalent timing error, is given by the mean value of the timing errors of the elements that change state as

$$\Delta t_{eq,nT_s} = \frac{1}{\Delta w[nT_s]} \sum_{k=w[(n-1)T_s]}^{w[nT_s]} \Delta t_k \tag{7.70}$$

where Δt_k is the timing error of unit element k. Each unit of the DAC is assumed to have a timing error which follows a normal distribution with a zero mean and a variance σ^2. The variance of the equivalent timing error is then

given by

$$\sigma_{T_E}{}^2 = \frac{\sigma^2}{|w[nT_s] - w[(n-1)T_s]|^2} \tag{7.71}$$

When many units change state, the equivalent timing error converges to its mean value, which is zero in this case. Therefore, the equivalent timing error improves when the number of unit elements increases, assuming that the distribution of the timing error per unit element does not change.

In [127], the SDR is calculated for these timing errors as follows. The error per transition is given by

$$e(m) = \frac{\Delta t_{eq,m}}{T_s} \Delta w(m) \tag{7.72}$$

where $w(m)$ is the output of the DAC expressed as a current. The autocorrelation $R_e(m,n)$ of $e(m)$ with respect to the timing error of the unit elements Δt_k is given by

$$\begin{aligned} R_e(m,n) =& E\left\{e(m)e(m+n)\right\} \\ =& \frac{1}{T_s^2} \Delta w(m) \Delta w(m+n) R_{T_E}(m,n) \end{aligned} \tag{7.73}$$

where the autocorrelation of T_E is given by

$$R_{T_E}(m,n) = \frac{\sigma^2}{|\Delta w(m)|\,|\Delta w(m+n)|} min\left(|\Delta w(m)|, |\Delta w(m+n)|\right) \tag{7.74}$$

The expected signal error power $R_e(m,0)$ is equal to

$$\begin{aligned} R_e(m,0) =& \sigma_{t_{eq}}^2 \frac{\Delta w(m)^2}{T_s^2} \\ =& \frac{\sigma^2}{{T_s}^2} |\Delta w(m)| \end{aligned} \tag{7.75}$$

the time average value of $R_e(m,0)$ is given by

$$P_e = \langle R_e(m,0) \rangle = \frac{\sigma^2}{T_s^2} \langle |\Delta w(m)| \rangle, \tag{7.76}$$

which gives the average power of the error signal due to timing errors of the unit elements. When the input signal is expressed as a Fourier series as follows

$$w(m) = \Re \left\{ \sum_{p=1}^{P} A_p e^{j2\pi m f T_s p} \right\}, \tag{7.77}$$

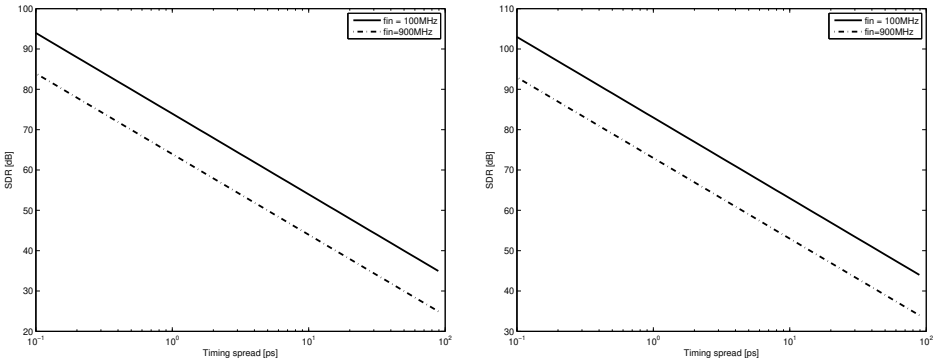
where A_p is the amplitude of frequency bin p. The term $|\Delta w(m)|$ is given as [127]

$$|\Delta w(m)| = \sum_{p=1}^{P} 2A_p \left| \sin(\pi f_p T_s) \sin\left(2\pi f_p T_s \left(m - \frac{1}{2}\right)\right) \right|. \tag{7.78}$$

Because the signal frequencies are bound to the Nyquist range the average power of the error signal as given in Eqn. 7.76 is found by

$$P_e = \frac{\sigma^2}{T_s^2} \sum_{p=1}^{P} \frac{4}{\pi} \sin(\pi f_p T_s) A_p \tag{7.79}$$

The signal to distortion ratio is then calculated as [127]



(a) 5 bit thermometer coded DAC (b) 8 bit thermometer coded DAC

Figure 7.15: The calculated results of the SNDR for various levels of segmentation @ 2744MS/s

$$SDR = \frac{P_s}{P_e} = \frac{\sum_{p=1}^{P} \frac{A_p^2}{2} sinc^2\left(\pi f_p T_s\right)}{\frac{4\sigma^2}{\pi T_s} \sum_{p=1}^{P} A_p \sin\left(\pi f_p T_s\right)} \tag{7.80}$$

For a full scale sinusoid the SDR can be simplified to [127]

$$SDR = 3.01(N-1) - 10\log_{10}\left(\sigma^2 f_1 f_s\right) - 9.03 \tag{7.81}$$

The result of Eqn. 7.80 is plotted in Fig. 7.15 for two levels of segmentation and two signal frequencies as a function of the timing spread at a sample frequency f_s of $2744MS/s$.

7.3 DAC specification

The target specifications for the DAC are based on the DOCSIS specifications as are summarized in Chapter 3.

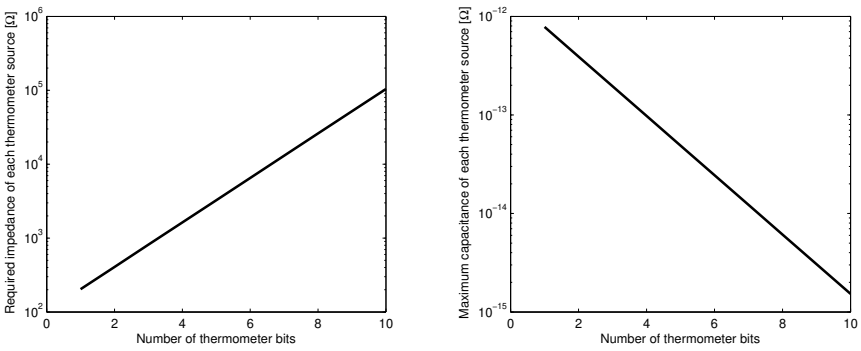
The sample rate of the DAC was determined in Chapter 5.5 to be at least $2400MS/s$ to be able to filter the Nyquist images with a realistic filter, to reduce the required analog filter. To ease the design of the upsampling to an integer ratio that can be factorized in small prime numbers, a sample rate of $2744MS/s$ is selected for the clock rate of the DAC, which is 512 times the data rate of the $5.36MS/s$ of a single carrier.

The jitter/phase noise requirements for the clock were analyzed in Chapter 6.2.1 to be better than $-95dBc/Hz$ at $10kHz$ offset for each carrier. Taking into account the frequency division ratio between the DAC clock and the highest carrier the requirements on the system clock is reduced to $-86dBc/Hz$ at $10kHz$ offset.

The required performance is determined by the ACLR specifications given in Table 3.3 and the amplitude levels as defined in Table 3.4. Using these specifications the requirements on the various aspects of the DAC will be defined.

An important specification of the DAC is the level of segmentation, i.e. the number of bits that are thermometer coded. When the segmentation is increased, the DNL of the DAC decreases, which results in less distortion to the output signal, especially around the mid-scale transition point where, typically for the full binary DAC, the DNL has its maximum. For segmented converters the maximum DNL typically occurs at the transitions where the binary bits are turned off and a thermometer source is turned on. For a two bit thermometer encoded DAC these points are at 1/4, 1/2 and 3/4 of the code range of the DAC, etc.. For segmentation levels higher than 4 bit, simulations show that the improvement to the signal quality because of current source mismatch becomes minor, as shown in Fig. 7.13.

Increasing the segmentation does also have an effect on the required output impedance of a thermometer source. Assuming that the DAC converts 16 carriers simultaneously, the required ACLR is $-62dBc$ as was calculated before. Taking into account a margin of at least $3dB$, the ACLR specification becomes equal to $-65dB$. Using Eqn. 7.47, the required impedance for a thermometer current source can be calculated. In Fig. 7.16(a), the result is plotted as a function of the number of thermometer sources. Assuming that the capacitive



(a) Impedance required

(b) Maximum capacitance of the current source

Figure 7.16: The required impedance and maximum capacitance of the cascoded current source for a signal frequency of 1000MHz

part of the impedance at higher frequencies is dominant over the resistive part, and using the highest signal frequency of $1000MHz$, the maximum capacitance of the cascoded current source is shown in Fig. 7.16(b). Especially for higher levels of segmentation the allowed capacitance becomes extremely small and is no longer realizable in the current process technology.

For the effect of the local timing variation on the performance of the DAC it is beneficial to increase the segmentation according to Eqn. 7.80 and Eqn. 7.81. This is mainly caused by the averaging effect when more thermometer sources are switched simultaneously. However, this equation only takes into account the thermometer coded part of the converter. Increasing the segmentation will often increase the area of the DAC, which could affect the mismatch that causes the local timing variation and thereby the performance of the DAC [127]. Increasing the segmentation by one bit will almost double the power consumption of the DAC, when the power for every thermometer bit synchronization stays constant. Often, this increase in power consumption is unwanted, and the power consumption for the re-synchronization per bit is decreased by a factor two. This increases the spread in the local timing variation. In order to make an accurate decision on the best segmentation for the local timing variation, a full layout implementation is required, which can be used to extract the para-

sitic capacitances in combination with a monte-carlo analysis. However, doing such a thorough analysis requires full optimization of each of these designs, which requires an excessive amount of time to make and analyze. Therefore, this analysis has not been executed.

A low segmentation results in a small binary-to-thermometer decoder, in favor of low complexity and low power consumption and especially to avoid disturbances caused by an otherwise large and complex digital circuit that operates at GHz frequencies. For clock frequencies of several GHz it is important to minimize the digital logic that has to operate at those high frequencies, since these circuits consume a lot of power and can generate interference. The decoder is made with current mode logic to minimize the distortion generated by the digital circuits, which could couple to the DAC and output signal.

Taking into account the output conductance, amplitude matching and the local timing variation and the operation speed required, a segmentation of 5 bit thermometer and 7 bit binary was selected. This relative low segmentation allows for a relative high power consumption in every bit for clocking and resynchronization and reduced complexity and power consumption in the binary-to-thermometer decoder.

Using Eqn. 7.68, it can be calculated that the spread in the mismatch of the current sources should be smaller than 0.01% to be limited by the quantization noise. This would result in an INL of 0.55 LSB. Since this results in an unrealistic low current source spread without amplitude calibration, the targeted INL is set to about 1 LSB which is about the maximum feasible for a 12-bits converter without calibration.

7.4 Architecture and circuit design

This section discusses the architecture of the DAC. Special focus is given to the sub functions that determine the performance at high signal and sampling frequencies.

7.4.1 Architecture

Fig. 7.17 shows the architecture of the designed DAC. It consists of a pipelined decoder for the thermometer bits, a delay for the binary bits which is equal to the latency of the thermometer decoder and an array of unit elements. Each unit element, denoted by Therm 0 to 30, of Fig. 7.17 consists of a combination of a master-slave latch, driver and output switches, see Fig. 7.18. The binary elements, denoted by Bin 0 to 6, use the same master-slave latch and driver, but use a scaled number of switches and current in the output stage.

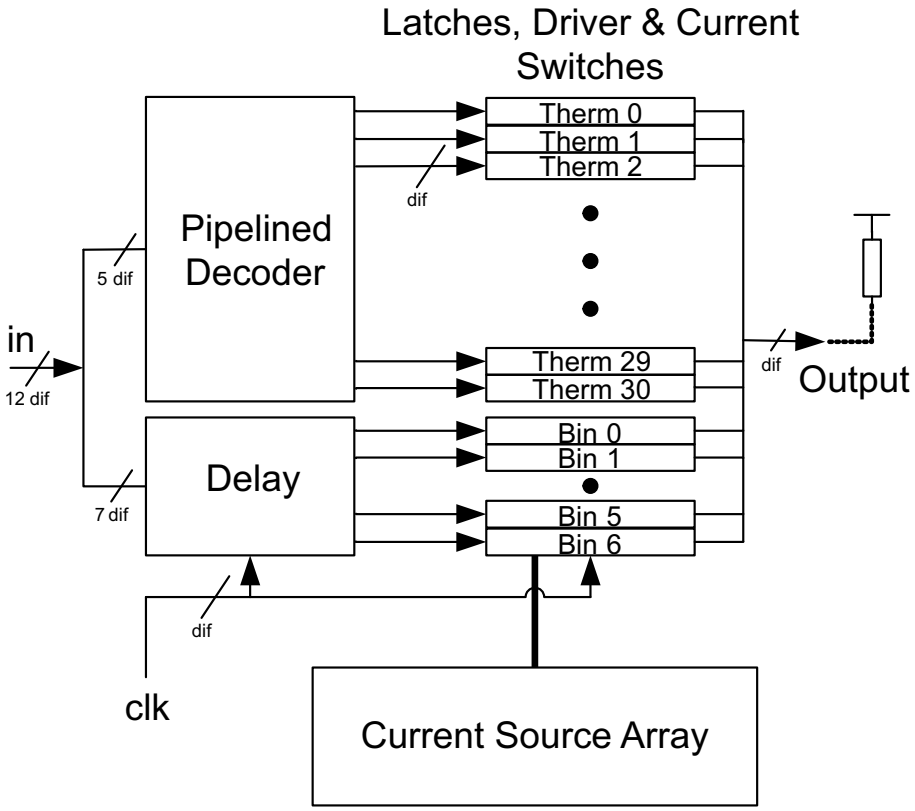


Figure 7.17: The fully differential DAC Architecture

The current steering DAC consists of many instances of the same unit that are connected in parallel for every thermometer bit. This unit contains a double latch and driver that drives the switches which steer the current of the unit

either to the positive or to the negative output terminal. The latches are used to synchronize the moment of switching with an accurate clock. The driver ensures that the switches have the optimal driving levels during the on and off conditions of the output switches.

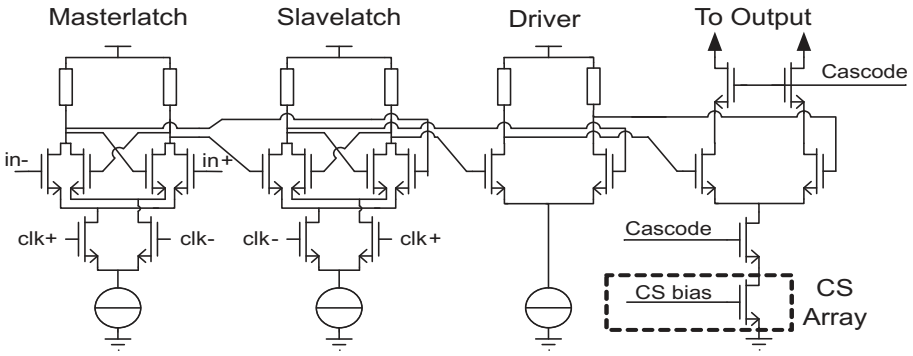


Figure 7.18: The master-latch, slave-latch, driver and switches that are placed in the unit array

The high frequency performance of DACs is critically dependent on the switching dynamics of each unit element, and also on the way the switching of one element affects the other. Ideally, all elements should switch in the same way, and should not interfere with each other. The intention is to achieve clock frequencies up to $2.8GHz$ while simultaneously maintaining an overall high linearity at high signal frequencies.

The segmentation is 5 bits thermometer and 7 bits binary. As said before, this segmentation allows a small binary-to-thermometer decoder. The architecture adopted for the decoder is fully differential, and is based on Current Mode Logic (CML) circuits, and uses internal pipelining; such an implementation offers higher immunity towards noise injected into common nodes such as the common substrate, power and ground rails. This is important, because the DAC will be part of a highly active digital circuit. Further steps have been taken to reduce the coupling between circuit nodes as much as possible as will be explained in more detail later.

The segmentation is 5 bits thermometer and 7 bits binary. One of the reasons for this choice was to be able to use a small binary-to-thermometer decoder,

in favor of low complexity and low power consumption and especially to avoid disturbances caused by an otherwise large and complex digital circuit that operates at GHz frequencies. For clock frequencies of several GHz it is important to minimize the digital logic that has to operate at those high frequencies, since these circuits consume a lot of power and can generate interference. The decoder is made with current mode logic to minimize the distortion generated by the digital circuits, which could couple to the DAC and output signal.

DAC topology

A common topology for a DAC is the matrix structure as was introduced by Miki [128], as illustrated in Fig. 7.19, or a derivative of it. This topology offers the benefit of being compact. However, it has some drawbacks that makes it less suitable for high frequency operation. At those high frequencies the synchronization between the different units of the DAC is critical. Any systematic timing difference between the units will create harmonic distortion in the output signal.

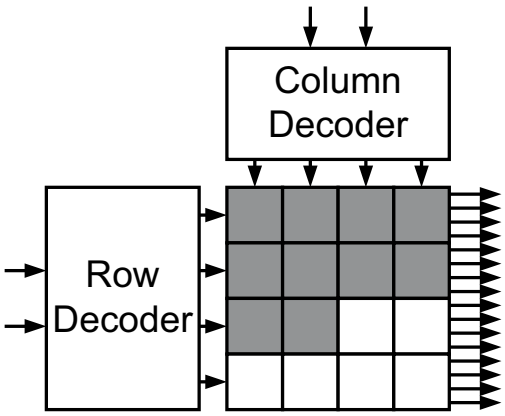


Figure 7.19: The traditional matrix topology of a current steering DAC

In the matrix topology it is difficult to achieve decent synchronization between the units. The clock and output network must be balanced and have the same length to every unit. In addition, the capacitive loading and the interconnect resistance in the network should match to the network of the other elements.

Otherwise the clock signal will not arrive at the same moment at all units or the output signals from the units will not arrive at the output pin at the same moment, thereby distorting the signal.

A method of balancing the interconnections of the clock and of the output network is to use a tree structure. When the units are layouted in a matrix, ensuring balanced trees is difficult. It requires a large space between the units to place the trees and coupling between those trees is hard to prevent. Because of the additional area the parasitic capacitance increases, which requires more power to ensure that the data and clock signals arrive in time over this increased distance.

Because the distance from the row and column decoder to the unit cells is different for all the elements, optimization of the drive strength is difficult.

An alternative topology is to place the units in a single row, thereby easing the design of the trees to connect the clock and output, see Fig. 7.20. This topology is selected in this design.

The current sources are placed at an separate location in the DAC. The current of the current sources relies on intrinsic matching instead of calibration methods. There are many papers published [129, 67, 130, 131] which use some form of calibration to ensure the matching of the current sources. While these papers often show excellent static INL and DNL performances, they often fail at higher signal frequencies because most of the calibration algorithms rely on modifying the circuit in the analog domain. This often increases the parasitic capacitance on nodes that are sensitive to their parasitic capacitance. This larger parasitic capacitance affects the dynamic performance of the DAC in a negative manner, since the improvement of the INL and the DNL characteristic of the DAC is commonly only dominant at relatively low signal frequencies. Having current source calibration is not expected to improve the performance of the DAC as the signal band of interest starts at $50MHz$ and most likely the static calibration will hamper the performance at higher signal frequencies.

Another calibration method [132] that uses reordering of the units according to their mismatch error seems better fitted given the high dynamic range that is required at high signal frequencies, because no extra circuits, except a low

frequency measurement circuit, are required in the analog domain. The main disadvantage of this calibration method is the need for a fast mapping decoder, which depending on the technology, number of thermometer bits and the operation speed, can consume more power than a standard fixed decoder.

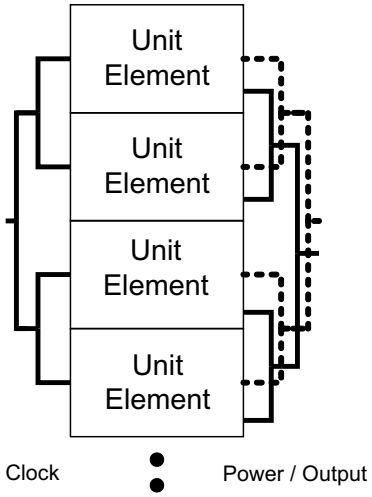


Figure 7.20: The placement of the elements with on both sides the trees to connect the clock, supply and output

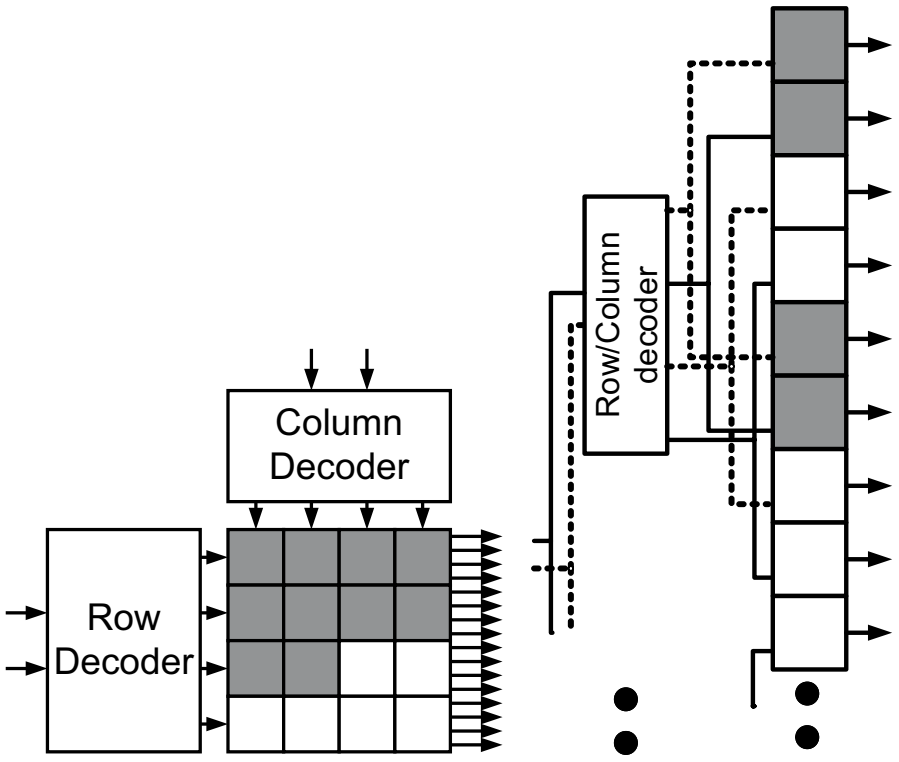
Decoder

Many DAC designs use the row/column decoder, that was introduced by Miki [128], to decode the binary MSBs into thermometer encoded bits. However, as said before, nowadays most designs do not place the current sources, switches and synchronization logic in the matrix anymore, but place them at a separate place. The conventional binary-to-thermometer decoder consists of three parts, the row decoder, column decoder and the array of decoding cells. The LSBs of the bits that are decoded are converted in the column decoder into intermediate thermometer codes, while the MSBs are decoded in the row decoder. The final unary code is generated in the decoding array that receives its inputs from both the row and column decoder. The rows are consecutively turned on while the column decoder determines the cells that are turned on in the last row that is

addressed by the row decoder. The decoding cell in the array can be realized by the function

$$T_{ij} = (C_j + R_{i+1})R_i, \tag{7.82}$$

which can be implemented by a simple OR/AND gate combination.



(a) Traditional decoder topology (b) Implemented decoder topology

Figure 7.21: The traditional and the used decoder topology

The decoder that is implemented in this DAC is designed as a standard row/column decoder architecture, however the decoding cells are not put into a matrix in the layout, but into a single row, see Fig. 7.21. The row and column decoder is distributed in five parts along this row. In this way, long wires to connect the unit elements with the row/column decoders are not required, resulting in

a lower wiring capacitance. The wires to the unit elements all have the same length, which reduces the timing differences of the moment at which the data arrives at the unit elements. This, in combination with the internal pipelining, in contrast to [133], further enables high speed operation.

Local timing variation

An advantage of the 5-7 partitioning is, that only 38 (31+7) elements require synchronization instead of 63+6=69 elements as in [133] or 127+15+5=147 as in [134]. Spread in the moment at which different elements change state results in a reduction of the performance [127]. Timing errors can be classified into deterministic errors and stochastic errors. The effect of stochastic timing errors on the signal quality is discussed in Chapter 7.2.4. The deterministic timing errors are primarily caused by length differences in the clock and in the output lines and supply voltage differences between the elements and thus should be taken care of.

The low number of elements enables reduced complexity of clocking and simplifies the layout of interconnects. For example, when the elements are laid out in a single row, this makes the clock and output wiring easier to manage. Because of a simpler layout the systematic timing errors originating from the clock and output wiring are easier to reduce. To minimize those deterministic differences, a shielded tree structure is used for the clock network. Despite that CML substantially reduces the timing sensitivity to supply variations (here: IR drops between different units) there still is some remaining sensitivity, especially with respect to the CML current source transistor. To further reduce this timing error mechanism, a full power supply tree was realized to guarantee the same Vss/Vdd for each element by design. This results in a better control of deterministic timing errors, but comes at the cost of less averaging of stochastic errors related to mismatch [127]. This has to be dealt with by other means as will be discussed in the next section.

The stochastic component of timing errors is caused by the mismatch between the different elements. Increase of the gate area of the switching transistor results in better matching, but does not necessarily lead to a lower timing er-

ror [127]. The timing error is determined by a combination of switch threshold mismatch and the slope of the signal driving the switch, the latter being dependent on switch gate capacitance, interconnect capacitance and driver output capacitances. Because the gate capacitance increases faster than mismatch reduces when the gate area increases there is an optimum to be found, for a given interconnect and parasitic capacitances. This optimization approach has been applied to each and every relevant internal node to achieve an overall timing error of <1ps after carefully considering extracted information from layouts for a complete element as is shown in Fig. 7.18. Another contribution to the timing uncertainty comes from the decoder. The moment that the output of the decoder changes, depends on the combination of the input value and the previous states of the decoder. This results in transition time variations even after re-clocking with latches inside the decoder. These variations can be reduced by putting multiple latches in cascade.

Monte Carlo simulations indicate that an rms timing error of 1.5ps, including all afore mentioned effects, was achieved by design for all 38 elements.

The current sources were placed as a separate array. No calibration was used for the current sources. Therefore, other methods are used to achieve the required matching. It consists of a combination of three methods. First, the current source array is split into four equal parts and a common centroid technique is used. Second, each of those four quadrants have their own bias voltage, reducing the potential gradients [127]. Third, a switching sequence is used which 'randomizes' the order of each current source in the quadrant, such that the total error does not accumulate. The methods used to optimize the current source array are described in Chapter 7.4.2.

In each element the current source is cascoded by a transistor to reduce the capacitance of the large current source transistor and its interconnection wiring seen at the output of the current switches, to achieve a high impedance at high frequencies. A second cascode transistor is placed between the switching transistor and the output node to reduce the coupling between the switching transistor and the output node, thereby limiting the impact of charge injection from the gate of the switches to the output and limiting the modulation of the switch junction capacitances by the large signal swing. This results in more

identical behavior of the switching over the complete input range.

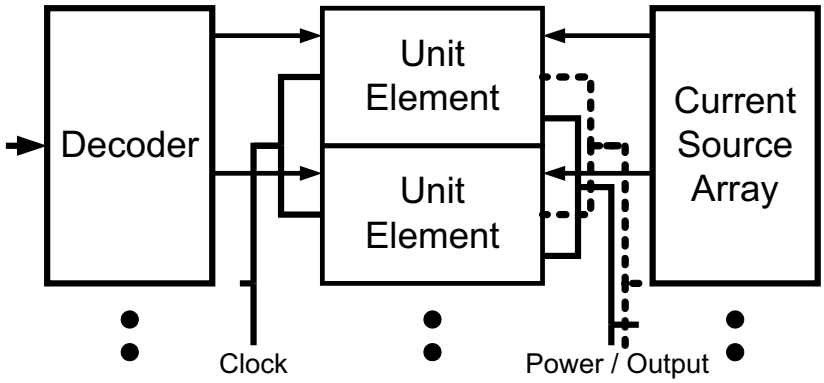


Figure 7.22: Tree structures placed at opposite sides to prevent coupling and interference

Another important consideration at GHz frequencies is the coupling between the different wires and coupling through substrate. One of the most critical points relates to the clock lines. These should not be distorted by the output signal and visa versa. In case this coupling is present, the clocking of all elements becomes data dependent, which will further distort the output signal. Moreover, the digital input signals should not couple to the output wires and clock lines. For those reasons the output wires and clock wires are at opposite sides of the elements, see Fig. 7.22. The data input is connected to the same side as the clock lines are, but to reduce the coupling between them a metal shield is used. The power tree is connected to the same side as the output tree is. Coupling between them is less of a problem because the power lines have low impedance and the differential circuitry results in low fluctuations or current glitches on them.

7.4.2 DAC circuits

In this section the implementation aspects of the DAC will be addressed using the previously described architecture.

Output current switches

Besides the aforementioned synchronization issues, also the equality of the current pulse shape between the binary and thermometer weighted current pulses is important, especially for DACs that have only a few thermometer bits, e.g. 5. The chosen segmentation results in a scaling ratio of 1:128 between the LSB and the thermometer bits for a 12 bit converter. A method to reduce the difference in size of the switches and of the upper cascode transistors in the binary part is to use multiple smaller switches and upper cascodes in parallel. In this design the transistors of the thermometer bits are split into 16 parallel transistors. The main advantage is the better scaling of the binary sources compared to the thermometer sources and the reduction of the capacitance that has to be driven. For example, for the most significant binary bit only half of the switches are used to steer the current of the source to the output nodes. The remaining switches of a binary unit are connected to a dummy current source. This dummy current is dumped into the power supply. This ensures that the behavior of all the switches is similar. This same method is used for the other binary bits, except for the three least significant sources. For those sources the switches are near minimum size and are not scaled anymore. The same master-slave latch and driver combination is used for all elements, including the binary elements to avoid synchronization errors due to different loading [127].

Output stage

The schematic of the output stage is shown in Fig. 7.23. It consists of a cascoded current source, a differential pair and two switch cascode transistors. The current source transistor, shown in the dashed box in the figure, is physically located at an other location as will be discussed in more detail later.

Current source cascode The current source transistor is large in order to ensure decent matching of the amplitude of each unit. The area of the current source transistor is determined to be $24\mu m^2$ for the LSB bit and $3072\mu m^2$ for the thermometer bit in the following section. This large transistor results in a

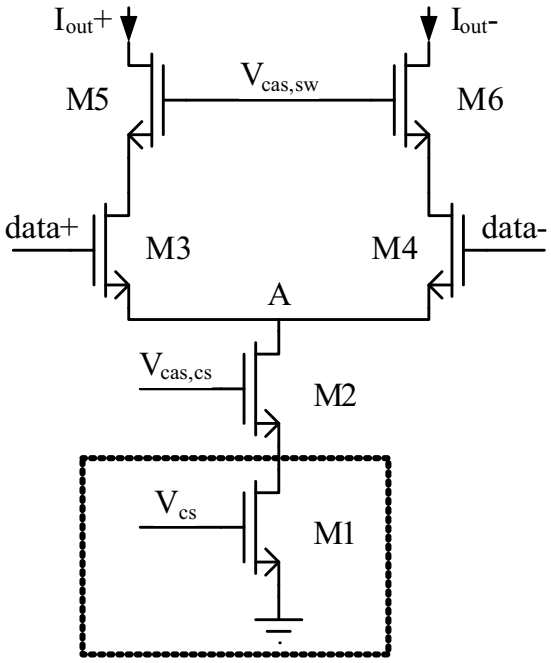


Figure 7.23: The output stage of a single unit

large parasitic capacitance. In addition, the current source transistor is split into four parts which are layouted using a common centroid methodology to avoid performance degradation due to a gradient that can exist in the IC. The four parts are connected together using relative long copper wires which add to the parasitic capacitance. To shield this large parasitic capacitance from the switches and to increase the output impedance of the CS a current source cascode transistor is added.

During the switching of a unit the common sources can have a small dip, which is caused by both switches being turned off momentarily. This dip in the common sources voltage can cause, when the switches are directly connected to the CS transistor or the dip is large, that the CS transistor goes out of saturation momentarily. When this happens, the output impedance drops significantly and because of the large capacitance on the drain of the CS transistor it will take a long time before the CS transistor is back to its normal operation condition. The current source cascode transistor, which is added between the CS

transistor and the common source node of the switch transistor, prevents this from happening. This cascode transistor is much smaller than the CS transistor and it is placed close to the switches, thereby reducing the parasitic capacitance. The disadvantage of this cascode transistor is its V_{ds} which reduces the headroom for the other transistors.

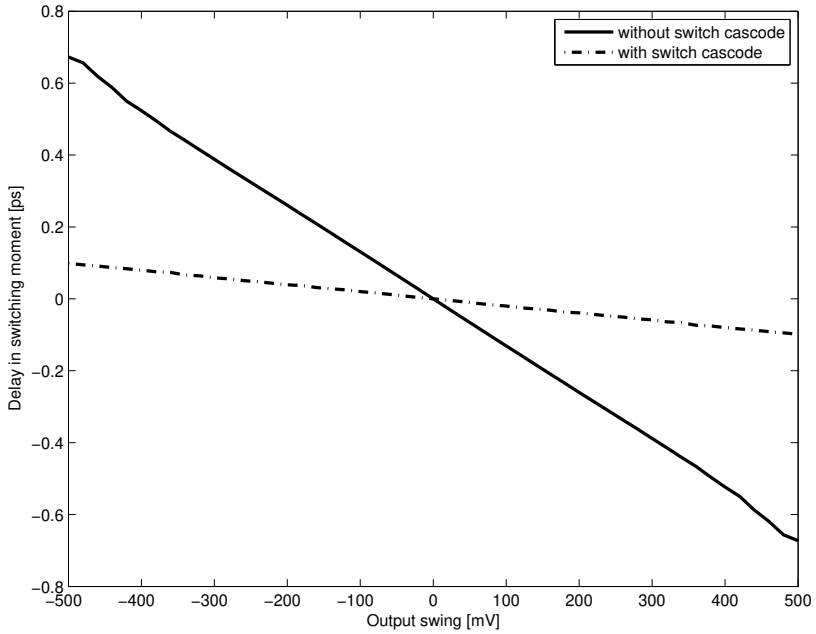


Figure 7.24: The variation in switching moment caused by the amplitude on the output of the DAC with and without a switch cascode transistor

Switch cascodes At the drain side of the switches another cascode transistor is added, which reduces the coupling between the output nodes and the switches. The moment of switching is influenced by the voltage on the drain of the switches, as shown in Fig. 7.24. Without the switch cascode transistor the drain voltage is directly connected to the output, which results in a data dependent moment of switching and therefore a distortion of the output signal. With the cascode transistors the swing on the drain as a result of the output swing is reduced, which reduces the variation in the moment of the switching by about a factor 7.

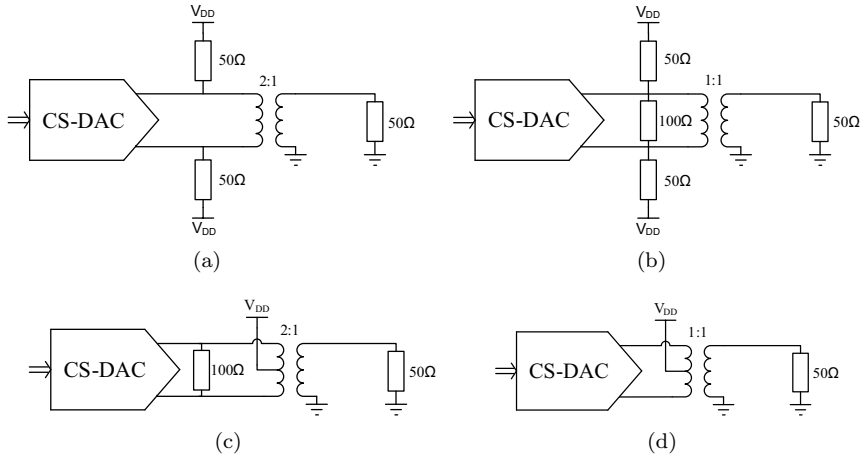


Figure 7.25: Several configurations to convert the differential output signal into a single-ended output signal

The capacitance variation between the on-state and the off-state of a unit is also reduced by placing a switch cascode transistor [135]. To reduce the capacitance on the drains of the switch and at the output, these cascode transistors are thin oxide transistors. In order to prevent breakdown of the transistors, the voltage difference between the gate-drain and gate-source terminals is therefore limited to the maximum thin oxide transistor supply voltage.

Output termination The differential output of the DAC is commonly converted into a single ended output with a high frequency transformer. Many configurations are possible to connect the output of the DAC and the single-ended output; a number of options is shown in Fig. 7.25. These configurations set the DC operation point of the output of the DAC and the effective AC impedance seen from the DAC. The configurations as shown in Fig. 7.25(a) and Fig. 7.25(b) do not use a center tap in the transformer. The DC operation point of the output is set by resistors that are connected to the V_{DD}. When the DC point is set too low, the CS transistor is pushed out of saturation and the performance is degraded significantly. The voltage drop over the resistors can be compensated for by applying a higher voltage to the termination resistors. However, when the current of the DAC is switched off, the DC operation point

becomes equal to this high supply voltage. Since the DC operation point of the output is limited to a normal operation voltage, such that the thin-oxide cascode transistors are not stressed beyond their maximum gate-drain voltage levels, these configurations are not preferred.

Since the output frequency range of the DAC extends up to $1000MHz$, it is important that the signal is properly terminated in order to prevent reflections in the output transmission lines. The output of a current steering DAC is high ohmic while the impedance of the PCB trace and termination is commonly 50 Ω[3]. When the signal frequencies are relatively low and the length of this connection is short, the effect is limited. However, at high signal frequencies the influence of these reflections increases. Therefore, the PCB trace is often terminated close to the DAC with a 50 Ω resistor to the V_{dd} at both outputs, see Fig. 7.25(a) or 100 Ω differential between the two outputs, see Fig. 7.25(c). Therefore, the configuration that is shown in Fig. 7.25(d) is not preferred and the configuration as shown in Fig. 7.25(c) is selected. The disadvantage of this 100 Ω resistor is the attenuation of the signal amplitude, which has to be compensated for by increasing the signal amplitude in the DAC.

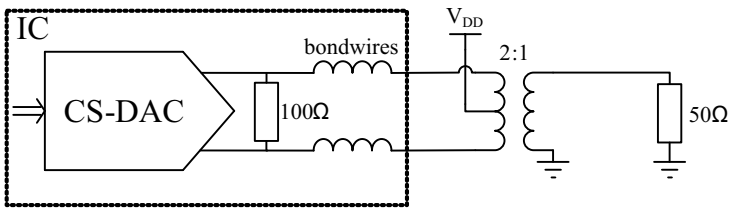


Figure 7.26: The implemented DAC output configuration

The selected output configuration is shown in Fig. 7.26. The termination resistor is placed inside the DAC, to damp the effect the bondwires have on the signal. The DC operation point is set by the center tap of the transformer, which has a 2:1 ratio.

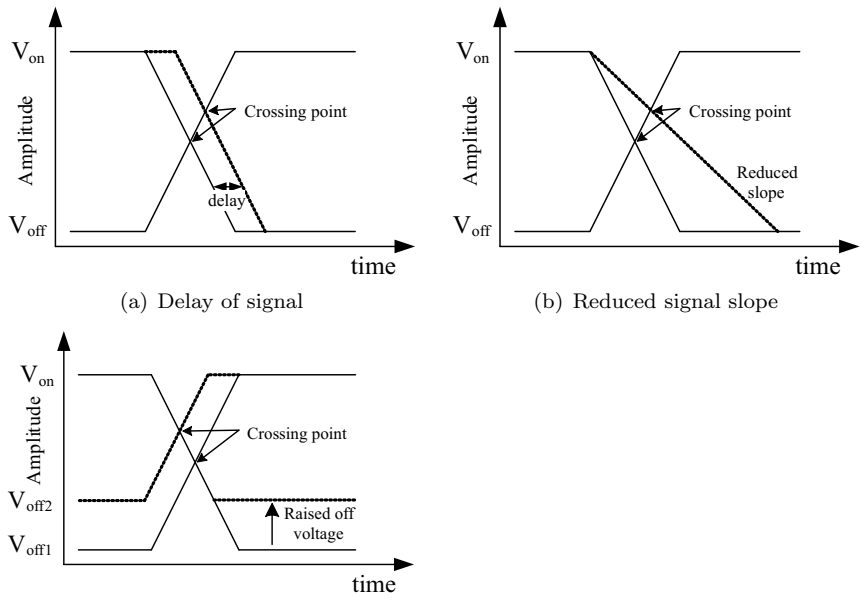
The supply voltage at the center tap of the transformer is set to a level of 1.5 V. This increases the voltage headroom in the DAC output stage. Since the drain

[3]The output configurations shown and used here have 50 Ω instead of the 75 Ω that is commonly used in the cable television environment, because the available measurement equipment is terminated with 50 Ω. In the application the impedance levels have to be adjusted or an impedance conversion circuit has to be added.

of the thin oxide cascode transistor is connected to 1.5 V DC, it is important for reliability reasons that the gate-drain voltage or the gate-source voltage does not go beyond the nominal maximum of 1.2 V. Since the drain is connected to the output and the source is connected to the drain of the switches which is well above ground this higher voltage does not impose a reliability problem. Since the voltage of 1.5 V is within the absolute maximum ratings of the process technology, this configuration will not result in problems even when the DAC is turned off while the termination voltage is still present on the output.

Switches and driver The gate voltage of the switches is defined by the driver. The high voltage of the output of the driver is equal to the supply voltage at the driver. The high voltage on the gate of the switches turns on the current to its output. The size of the switch in combination with the current through it determines the voltage at the common source terminal. This voltage determines the headroom for the current source transistor and the cascode transistor. Reducing the voltage decreases mainly the overdrive voltage V_{gt} of the current source transistor, which affects the matching behavior and the thermal noise at the output of the DAC. Increasing the voltage at the common source terminal requires larger switch transistors. This larger transistor increases the charge feedthrough to the output at the switching moment and increases the load on the driver, which then requires more power to reach the same settling time and slope of the signal. Reducing the signal slope increases the spread in the moment the output changes state due to the mismatch, or inter-symbol interference will increase as shown later. Therefore a steep slope is desired.

The effective crossing point of the driving signal determines the moment when the output current is steered in the complementary output. When the crossing point is too low, the switch that has to go off turns off faster than the complementary switch turns on. As a result the current in the current source will reduce momentarily, which will result in a glitch in the common source terminal of the switches. In case this glitch becomes too large the voltage on the drain of the current source transistor will drop too much and the transistor will go out of saturation. Because the current source transistor is a large transistor with a big parasitic capacitance, it can take a long time to recover.



(a) Delay of signal

(b) Reduced signal slope

(c) Raised off voltage

Figure 7.27: Several methods to raise the effective crossing point of the driving signals to the output switches

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With control signals at the gate of the switches, varying between 0 V and V_{DD}, the cross point of the two control voltages equals to $V_X = V_{DD}/2$. In this case the voltage variation on the drain of the current source can be as large as [136]

$$\begin{aligned} \Delta V &= -\frac{V_{DD}}{2} + \left(\sqrt{\frac{2I}{\beta}} - \sqrt{\frac{I}{\beta}} \right) \\ &\approx 0.4V. \end{aligned} \tag{7.83}$$

where $\beta = (W/L)_{sw}\, KP$, and KP is the gain of the transistor. I is the current of the current source. In this equation, the effect of the capacitance is not taken into account. The voltage calculated is therefore larger than it would be in reality.

There are a number of methods to ensure that the voltage change at the common node of the unit current cell remains constant. Three methods are described below, and shown in Fig. 7.27. These methods all achieve the same

effect: the crossing point of the drive signals is raised in such away that the switches are never both off at the same time.

- The first method is to delay the drive signals, see Fig. 7.27(a). There are several structures published in the literature that perform this function. However, all of these structures have the disadvantage that the delaying of the control signal limits the use at high clock frequencies.
- The second method is the delay of the rising or the falling drive signal, see Fig. 7.27(b). The falling of the control signal is for example delayed for some time, while the rising of the control signal is not delayed. This method of different rise fall time has the disadvantage of a reduced operation speed and increased jitter in the switching moment.
- The third method is to raise the crossing point of the drive signals by changing the output voltage span of the driver, see Fig. 7.27(c). The output voltage of the driver is changed in such a way that the lower output voltage is higher than zero. If the lower output voltage is increased, the switching point of the output switches is also increased.

An additional advantage of the last method is the reduced voltage swing the driver needs to drive. The driver will be faster and also the charge feedthrough of the output switches is reduced. The preferred effective crossing point is at about 2/3rd of the swing.

The swing that is required at the output of the driver is determined by the allowable current through the switch transistor that is in the off-state. When the swing is too small the off-state voltage at the gate of the switch is too high and leakage current will continue to flow through it. When this current will only attenuate the differential output voltage it would not be problematic. However, this off-state current is sensitive to mismatch of the switch transistors and the driver swing. Since both the switch transistors and the driver transistors are small for speed reasons, they have a large spread. Therefore, the current at the output depends on which cells are turned on and off, thereby creating distortion. When the swing is increased too much, the charge injection at the switching transistors is larger than required, which reduces the performance.

In addition the output swing of the driver is larger which requires an increased load resistance in the driver which increases the time constant of the driving signal of the output switches. This increases the sensitivity for timing variations due to the mismatch of the switches. Alternatively the tail current of the driver can be increased at the cost of a higher power consumption. As compromise the driver swing is set such that the off-state current is less than 1/1000 of the on-state current.

As said before, in order to reduce the difference between the thermometer units and the binary units the switches and cascodes are split into 16 parts. Using this method the four most significant binary bits can be scaled ideally and show the same behavior as the thermometer sources. For the remaining binary bits the switch and the switch cascode transistor are not scaled further down, while the current source and the current source transistor are scaled down according to the required current for these bits. The reason for not scaling down the switch and its cascode transistor is the minimum size that is allowed by the design rules. Because of this unscaled switch the delay for the smallest LSB units is larger (the capacitance on the nodes is constant while the current is smaller), than for the thermometer bits.

Output stage circuit Between all those previously mentioned conditions a compromise has to be found. The process that is used does unfortunately not support low V_t transistors which would ease the limited voltage headroom. The implemented sizes and nominal operating voltages of the output stage are given in Fig. 7.28.

Tail current in CML stages

The minimum power in a latch or buffer stage can be determined by the power that is required to suppress the inter-symbol interference (ISI) below a certain level. In Fig. 7.29 the effect of the ISI on the moment a bit changes state is shown.

To prevent ISI the bit must settle well within a single clock cycle. When the transition is not settled before the next clock cycle the signal transition starts

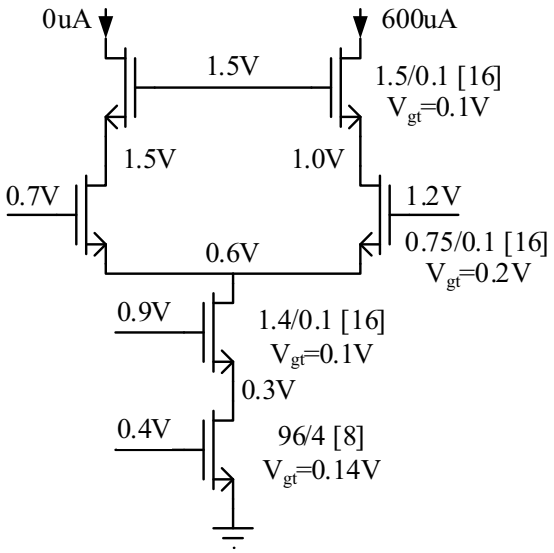


Figure 7.28: The sizes and operation points of the output stage

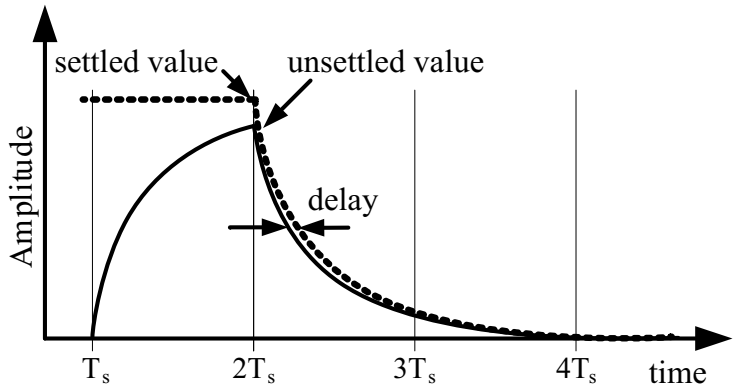


Figure 7.29: Illustration of inter-symbol interference of a single-ended signal at the output of a digital circuit

from a lower starting value, thereby crossing the mid amplitude value earlier than bits that are in the previous state for an extended amount of time.

The allowed amount of ISI can be calculated by assuming exponential settling of the driving signal of a CML gate. As derived in Chapter 5.6.2, the delay time τ_d is given by

$$\tau_d = 0.69 R_D \left(C_{par} + C_L \right), \tag{7.84}$$

where R_D is the load resistance, C_{par} is the parasitic capacitance and C_L is the load capacitance. The output voltage of the single-ended equivalent circuit is given by

$$V_{out}(t) = \left(V_0 - \Delta V \right) e^{-\frac{t}{RC}} + \Delta V. \tag{7.85}$$

When we assume the transition point of the circuit that is driven by this stage is at the mid value of the output $V_{out} = \frac{1}{2}\Delta V$ then the time to reach this value is given by

$$t = \ln \left(\frac{V_0 - \Delta V}{V_0 - \frac{1}{2}\Delta V}. \right). \tag{7.86}$$

As shown in Fig. 7.29, in case the signal is fully settled the initial condition is given by $V_0 = \Delta V$. When the signal is not fully settled, V_0 is given by

$$V_0 = \Delta V \left(1 - e^{-\frac{t}{RC}} \right). \tag{7.87}$$

The moment the output crosses the transition point is given by

$$t_{unsettled} = \ln \left(2 \left(1 - e^{-\frac{t}{RC}} \right). \right) \tag{7.88}$$

The difference in switching moment is given by

$$\Delta t = t_{unsettled} - t_{settled} = RC \ln \left(1 - e^{-\frac{T_s}{RC}} \right), \tag{7.89}$$

R defines the ΔV given the I_{tail} of the differential CML gate as shown in Fig. 5.11(a). As discussed in Chapter 5.6.2 the single-ended swing for a high speed CML circuit is typically close to the V_t of the process. The C is given by the

combination of the load capacitance and the parasitic capacitance of the wiring and the transistors.

As an example of this method of calculating the minimal required tail current the driver of the output switches is taken. The estimated capacitance C, consisting of the transistor capacitances and the parasitic capacitances is estimated to be about 40fF. The swing on the output of the driver is determined in Chapter 5.6.2 to be 0.5 V. Therefore, the tail current, I_{tail} is given by

$$I_{tail} = \frac{\Delta V}{R} = \frac{0.5}{R} \tag{7.90}$$

with a sample frequency of $2744MS/s$, T_s is equal to about $360ps$. A tail current of $300\mu A$ gives a $\Delta t \approx 300fs$, while a tail current of $400\mu A$ gives a $\Delta t \approx 40fs$. The final circuit uses a current of $450\mu A$ which results in a $\Delta t \approx 15fs$, which ensures that the ISI does not affect the performance.

Bias network and supply network

All the components in the unit cell, such as master latch, slave latch, driver and cascodes, require biasing from an accurate reference. To ensure high performance the differences in moment that units switch or the differences in the amplitude value of each unit cell should be small.

In Fig. 7.30 the variation in the unit cell output amplitude is shown when a single bias current is varied. The mismatch in the amplitude is given for variations of the nominal current for the master latch, slave latch, driver and current source cascode transistor. The figure shows that even a variation of 10 % of the bias currents in the unit cell does not have a big impact on the amplitude of the signal, i.e. less than one LSB.

In Fig. 7.31 the variation of the timing due to a variation of the bias current is shown. From this figure it can be concluded that the slave latch is dominant in the variation of the switching moment. To keep the variation of the switching moment due to the biasing of the slave latch alone less then 0.5ps, the variation of its bias current should be less than 3.5%.

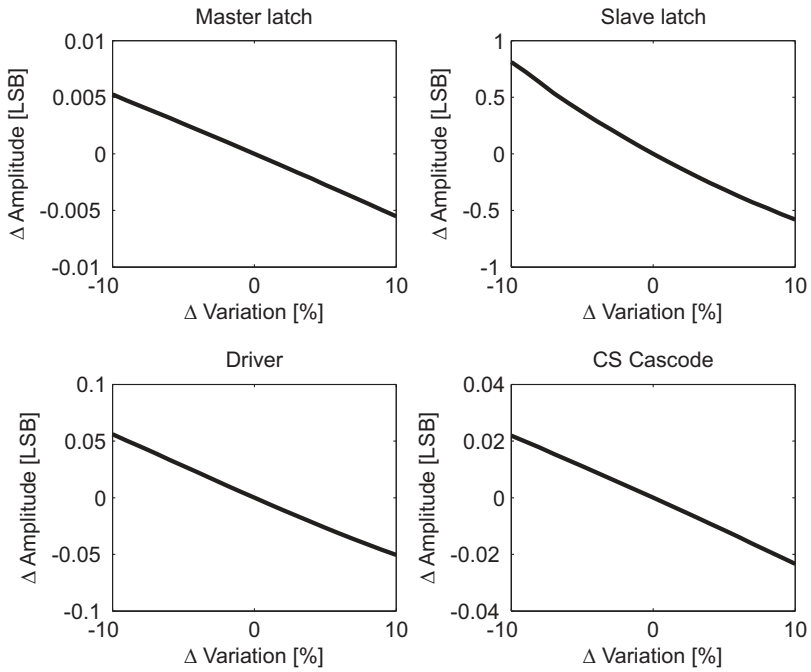


Figure 7.30: Variation of the output amplitude of the DAC as a function of the variation of the bias currents of the master latch, slave latch, driver and current source cascode transistor

To distribute the bias to all the units two options are available. Current biasing and voltage biasing respectively. When current biasing is used, see Fig. 7.32(a), the mirrored current at the target is in first order independent of any voltage difference between the units. The transistors in the dashed box, $M1$, $M2$ and $M7$, are commonly placed at a central location and $M3/M4$ and $M5/M6$, etc. are placed in every unit cell. The currents I_A and I_B should be equal to each other. However, due to mismatch these currents will differ. The current biasing method involves three transistors that should match to each other in every unit cell, $M2$, $M3$ and $M4$ should match $M7$, $M6$ and $M5$ respectively.

With current biasing the power consumption of the DAC increases, because for every element a separate bias current is required. The matching of this bias distribution current that involves $M2$ and $M3$ is determined by the size

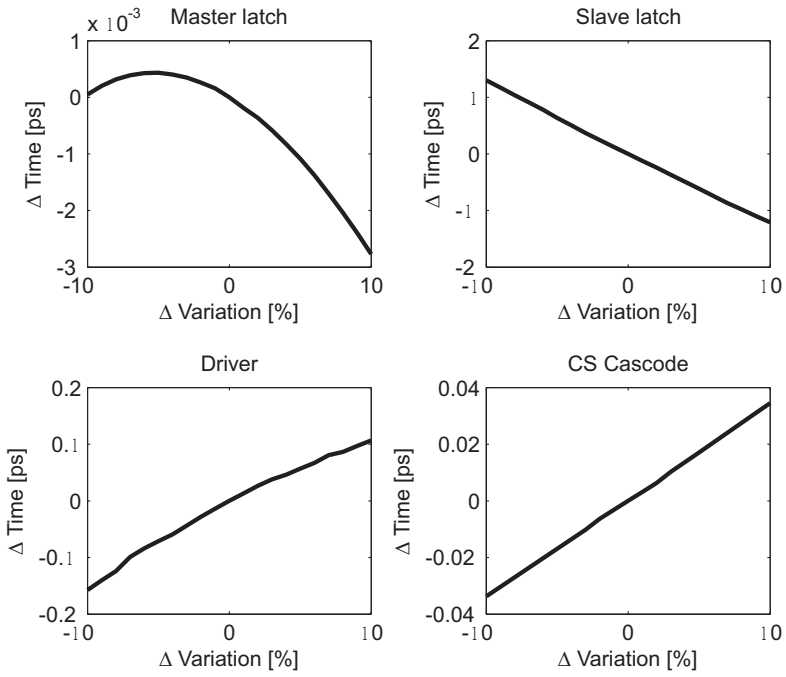
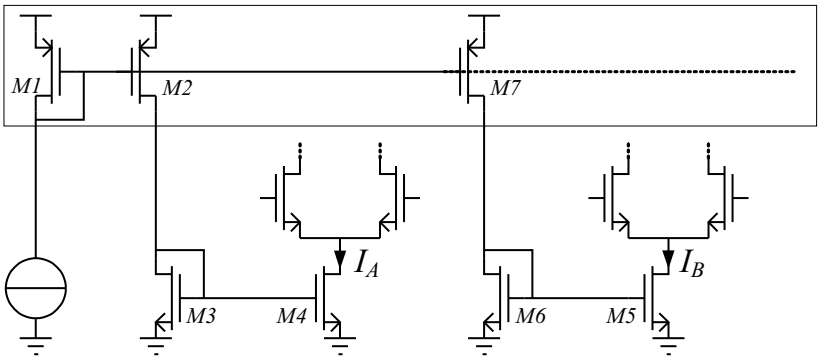


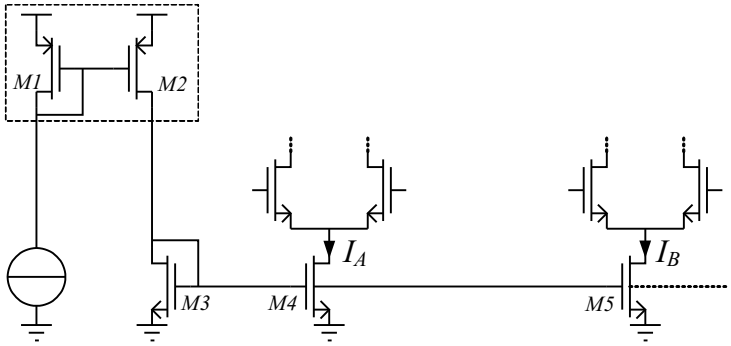
Figure 7.31: Variation of the moment of switching as a function of the variation in the bias current

of the transistors and the value of the current. Increasing the size and thereby the current of these transistors improves the matching at the cost of more power. In Fig. 7.33 the 3σ variation of the slave latch current is shown due to mismatch as a function of the current used in the bias distribution relatively to the nominal current in the slave latch. To ensure a variation less than 3.5 %, about a third of the power consumed in the slave latch is used for biasing it, thereby increasing the total power consumption significantly.

With voltage biasing, as shown in Fig 7.32(b), only a single bias distribution current is required for the DAC. The mismatch of the current through the circuits between the elements is determined by the matching of a single transistor to each other, i.e. $M4$ to $M5$. This is advantageous for the power consumption and the performance of the DAC. Mismatch in the other transistors will result in a variation in the absolute value of the current, which will not affect the



(a) Current biasing for the elements



(b) Bias distribution with voltage

Figure 7.32: Various methods to bias the circuits

performance when kept within normal limits.

However, with voltage biasing it is critical that the voltage on the gate and the source for every bias transistor is equal and care must be taken that the ground return does not create a voltage difference between the current sources, see Fig. 7.34. Since the current of a transistor in saturation is given by

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} \left(V_{gs} - V_t\right)^2, \tag{7.91}$$

the current I_D is proportional to the ΔV^2. In Fig. 7.35 the variation of the slave latch current is shown as a function of the voltage drop across the ground return. Since the target is to keep these systematic variations less than 0.2ps

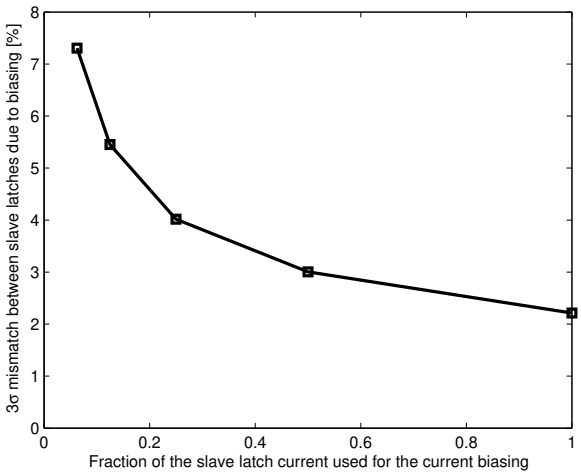


Figure 7.33: The 3σ variation of the current through the slave latch as a function of the relative current used in the bias distribution

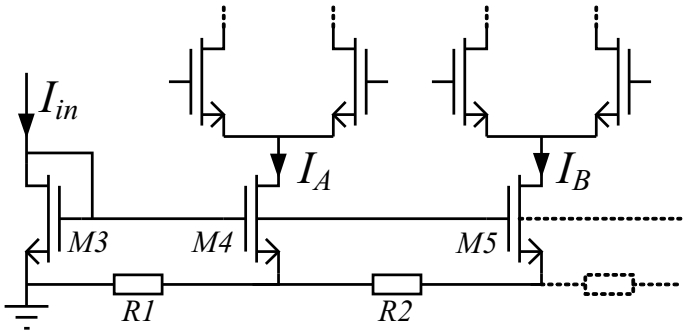


Figure 7.34: The voltage drop of a voltage biased circuit

the voltage drop across the ground should be less than 2mV, which requires a careful design of the ground supply.

In this DAC the supply connections are made with a tree structure to ensure that the resistance to the central ground connection is equal for all element, as shown in Fig. 7.36.

The biasing of the current source cascode transistor is the only exception to the chosen voltage biasing scheme. The drain of this transistor is connected

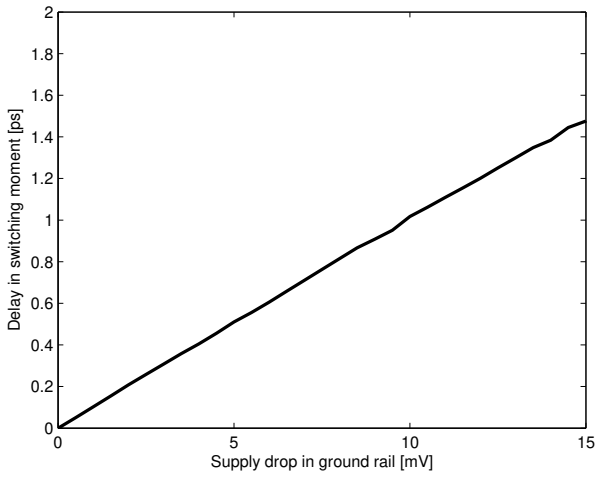


Figure 7.35: The variation of the current through the slave latch as a function of the voltage drop in the ground return

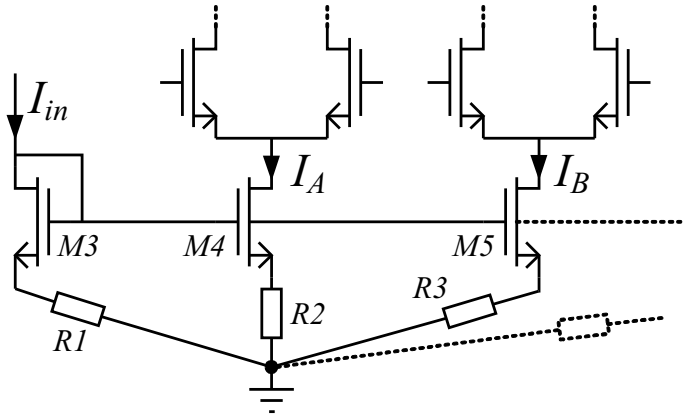


Figure 7.36: Tree structure in the ground connection to ensure equal series resistance in the supply line.

to the common source terminal of the switches. As discussed in Chapter 7.4.2 this terminal has glitches on it during the moment of switching. Through the gate-drain overlap capacitor this glitch can couple to the common bias node when voltage biasing would be used. This switching is data dependent and should not affect the other units that do not have to change state.

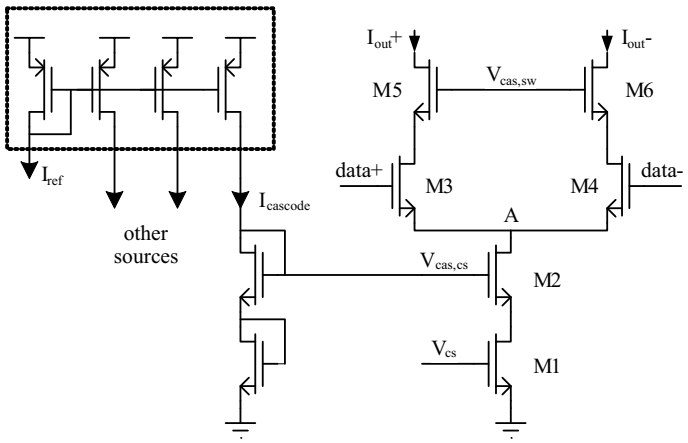


Figure 7.37: Local biasing for the current source cascode transistor.

As can be seen from Fig. 7.30 and Fig. 7.31, the influence of mismatch on the switching moment or the amplitude of the unit is small. For these reasons a local biasing voltage is created using the circuit shown in Fig. 7.37 that biases the current source cascode transistor. The part in the dashed box is placed at a separate location close to the DAC.

Current source array

The current source array is placed as a separate area in the DAC. The size of the current source array is mainly determined by the size of the current source transistors that need to be large to reduce their mismatch.

For a current steering DAC the INL is mainly determined by the matching behavior of the current sources. To achieve the resolution of 12 bit the current sources need to be matched accurately. Due to the mismatch of the CS transistors, the INL of the DACs will vary randomly. When the mismatch becomes too large, it will affect the performance of the DAC in the system. It is therefore important to be able to predict the requirements on the current source transistors. To predict the number of devices that comply to the required INL specification, yield will be taken as the criterium. For the static INL specification, the yield is commonly defined as the percentage of DACs with an INL

smaller than 0.5 LSB. When this specification is met, the DAC is guaranteed monotonic, which means that an increasing input signal will always result in a non decreasing output signal. Many attempts are made to relate the INL specification and the relative matching of the current source transistor. In literature a number of approximations have been published [137, 138, 136, 139, 140, 141].

In [142] an exact analytical formulation based on the Brownian Bridge of the yield with an INL $< 0.5LSB$, is given for an unary DAC with uncorrelated mismatch between the transistors:

$$Yield_{INL<0.5\ LSB} = 1 - 2\sum_{k=1}^{\infty}(-1)^k e^{-\frac{k^2}{2(2^N-1)\left(\frac{\sigma_u}{I_u}\right)^2}} \tag{7.92}$$

Although this equation is derived for unary converters, in typical conditions the equation is also applicable for binary or segmented converters [142]. The targeted yield is set to a value of 97.5%.

The area of the unit current source as a function of the relative standard deviation and the bias point is given by [143]

$$W \cdot L = \frac{1}{2}\left({A_\beta}^2 + \frac{4{A_{VT}}^2}{(V_{gs}-V_t)^2}\right) \Bigg/ \left(\frac{\sigma(I)}{I}\right)^2, \tag{7.93}$$

where A_β and A_{VT} are process constants. The size of the unit current source transistor depends on the V_{gs} applied to the transistor. For the smallest transistor size it is preferable to set V_{gs} as high as possible. The voltage is limited by the fact that the current source transistor has to operate in the saturation region and by the voltage headroom, as discussed before. The ratio between the width and the length, is given by

$$\frac{W}{L} = \frac{I}{KP_n \cdot (V_{gs}-V_t)^2}, \tag{7.94}$$

For a $V_{gt} = V_{gs} - V_t = 0.14V$ and 12 bits accuracy with 5 bits thermometer code, the current source transistor is calculated to have an area of $24\mu m^2$ for

the LSB current source transistor. Its width and length are 6 μm and 4 μm respectively.

The calculation of Eqn. 7.92 of the current source matching to achieve an INL below 0.5 LSB assumed that the current sources have a mismatch that is uncorrelated between each other. However, the spatial location of each transistor has an influence on its matching behavior, because due to the manufacturing process, temperature differences and mechanical stress, etc. the parameters of the transistor vary from location to location. Several methods are published to organize the locations for the sequential bits such that the errors of the individual transistors do not accumulate, which would result in a large INL [127].

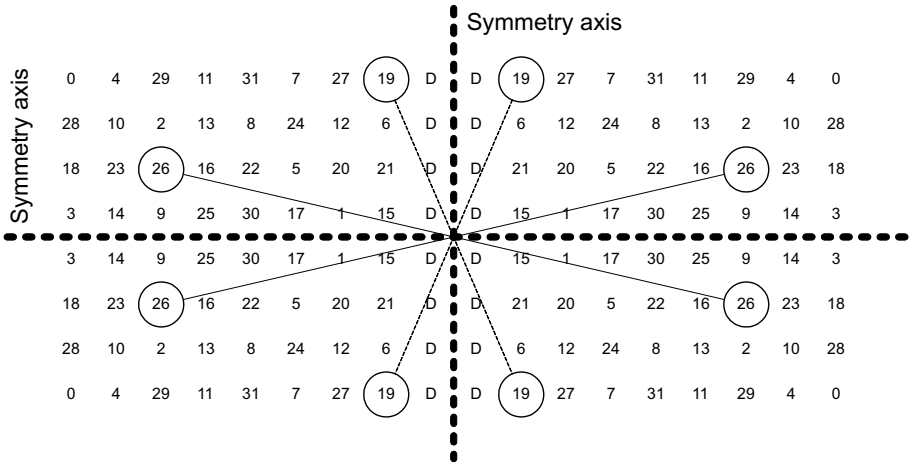


Figure 7.38: Common centroid current source array

Most of these algorithms optimize the placement for a linear gradient. The algorithm in [127] takes also parabolic gradients into account in the algorithm. In this DAC the placement of the sources has been calculated using the algorithm that is described in [127] and the result is shown in Fig. 7.38. In addition to this placement sequence, each current source transistor is split into four parts which is then placed according to the common centroid placement. These four parts of the current source transistor are then connected together by a mesh of metal lines in which care is taken to match the length interconnect lines as much as possible. This is needed because the current source transistor, nr 0,

in Fig 7.38 requires more interconnect to join the four parts of the transistor together than transistor 15 in this example. To compensate for this imbalance in interconnect resistance and interconnect capacitance, the transistors that are placed in the outer corners are connected to the unit elements that are close to the symmetry axis of the array. Transistors that require less interconnect are connected to the unit elements that are close to the outer edges, which requires therefore longer wires. To distribute the current as equally as possible over the current source transistor that is split into four parts, the wires that join the 4 parts together are placed on different layers than the wires that route the signal to the elements. These wires are connected together close to the center and therefore the interconnect resistance to the four transistors is almost equal.

To reduce the mismatch due to edge effects, dummy transistors are placed around these current source transistors.

Since the current source transistors are biased using voltage biasing, it is important that the connection of the sources of the transistors to the central ground is made using a tree structure. Special care must be taken for the binary sources, since their current is a fraction of the current for the thermometer sources. Since all binary sources have a replica in the unit element which when summed to the current of the binary bit forms a value that is equal to the current of a thermometer source, this replica is placed next to the binary source. Simulations with extracted layouts have been performed to ensure the matching of the interconnect resistances.

7.5 Layout and IC implementation

The floorplan of the DAC core is shown in Fig. 7.39 and a chip photo of the DAC is shown in Fig. 7.40. On the top of the figure the input buffers, decoder and the delay equalizers are located. Between the decoder and the DAC unit array the clock network and the interconnect between the decoder and the DAC units is placed. In the empty space beneath the clock network decoupling is placed for the supplies of the DAC. The thermometer units of the DAC are split into two parts and are placed on the right and left side of the

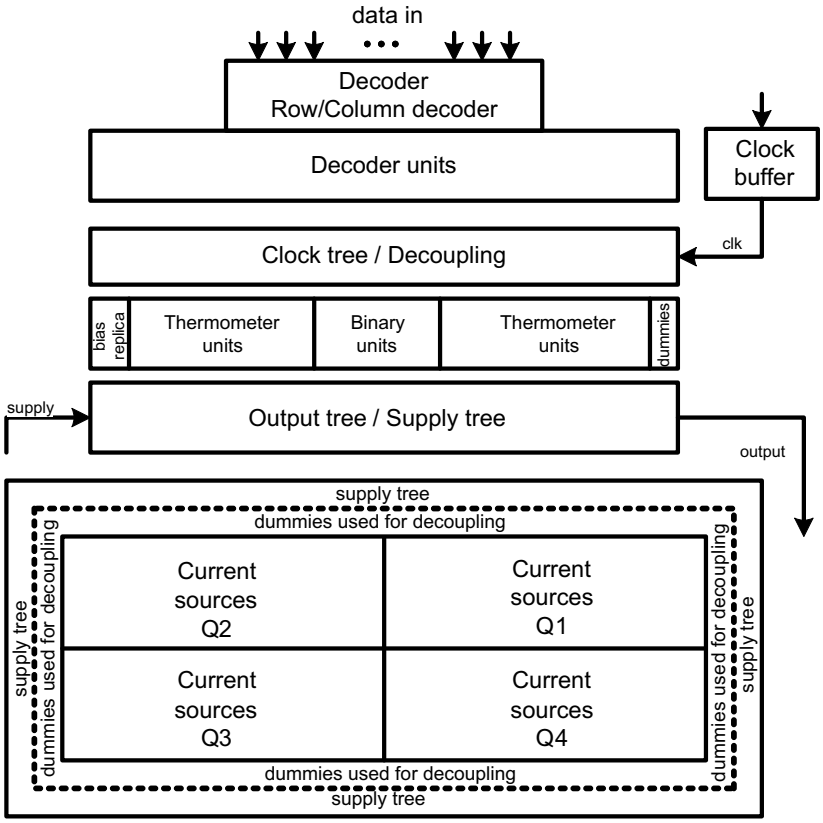


Figure 7.39: The floorplan of the DAC core

array. The binary units are placed in between those parts. On the left size a unit cell is placed that generates the bias voltages for the unit array. Dummies are placed on either side to ensure that the first and the last unit doe not suffer from edge effects. The top right corner locates the clock buffer of the DAC at a distance from the decoder to reduce the potential interference from the digital circuits. On the bottom side of the figure the current source array is placed. As said before, this array is split into four parts which are layouted in a common centroid topology. Around these current source transistors, dummy transistors are placed to reduce edge effects. These dummy transistors are used for decoupling of the supply of the DAC. In between the current source array and the units array the output tree and the supply tree are located. The

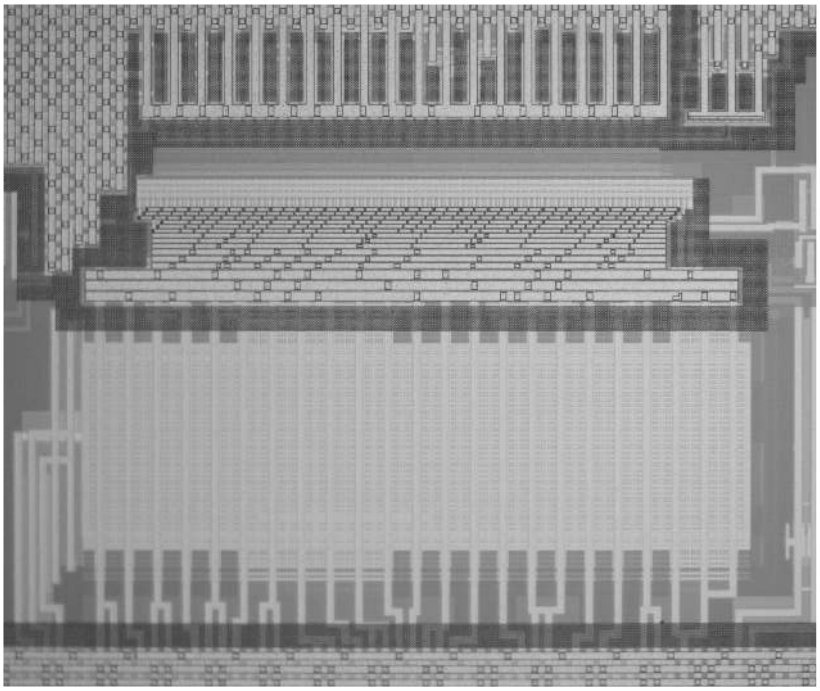


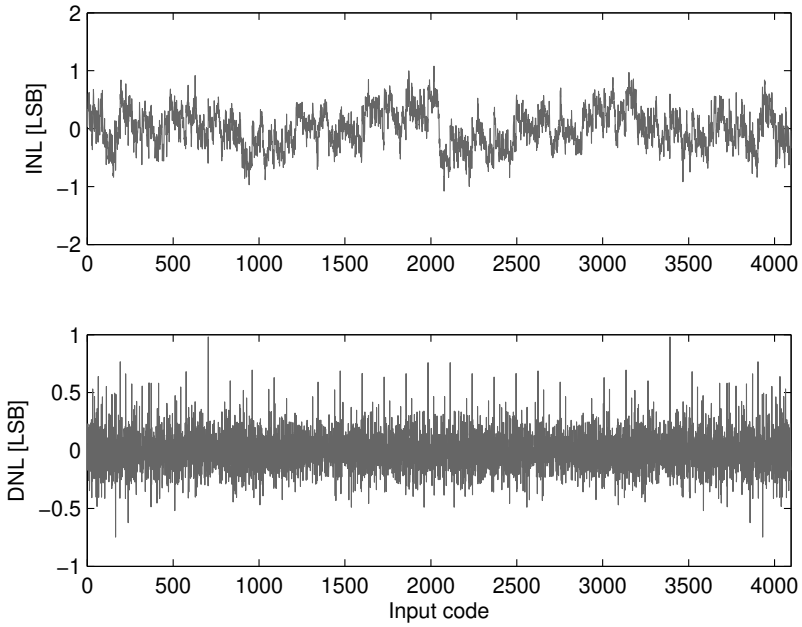
Figure 7.40: A chip photo of the DAC core

supplies of the DAC are distributed over the top metal layers of the current source array to the bottom side of the chip. All these metal lines that are routed over the current source array are placed in the pitch of the transistors to avoid metal coverage effects in the current source transistors.

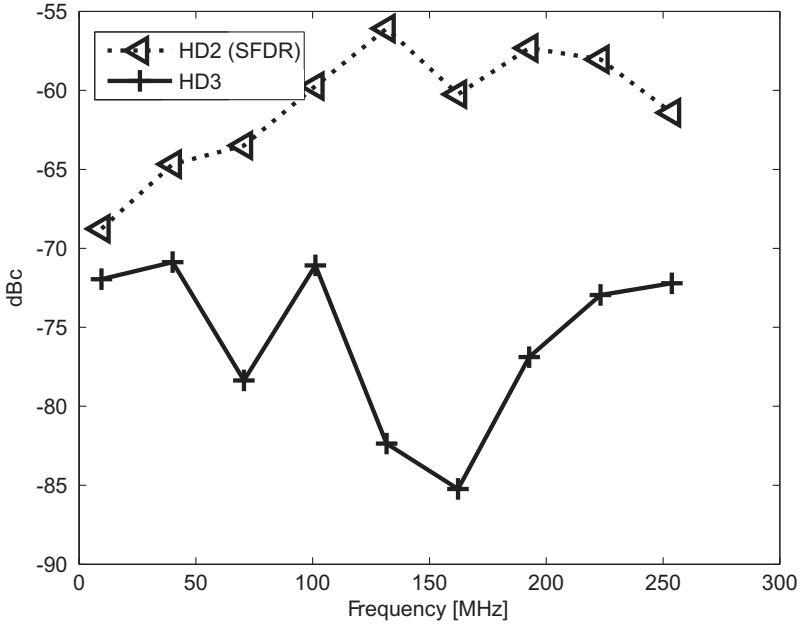
The DAC occupies an area of 1mm^2 including the current source array, the unit elements and decoder.

7.6 DAC measurements

The power consumption of the DAC is $110mW$ for the analog circuitry, $170mW$ for the digital circuits (decoder) and $80mW$ for the clock circuits at a supply voltage of $1.2V$, independent of the clock frequency.



(a) A typical INL / DNL measurement of the DAC



(b) Measured HD2 and HD3 vs input signal frequency at a sampling frequency of $650MS/s$

Figure 7.41: Measurements of the DAC

In Fig 7.41(a), a typical measured INL and DNL of the DAC is shown. The INL has a maximum value of about 1 LSB while the maximal DNL is 0.9 LSB.

Fig. 7.41(b) shows the single tone 2nd and 3rd harmonics as a function of the input signal frequency with an external input signal clocked at $650MS/s$. The second harmonic dominates the SFDR over the complete frequency band. This second harmonic is higher than expected from extracted simulations. A possible cause is the magnetic coupling between bondwires of the output signal and the power supply bondwires. Nevertheless, it is still better than $56dBc$ for up to $300MHz$. The target was a SFDR of $60dBc$ over the complete Nyquist frequency range.

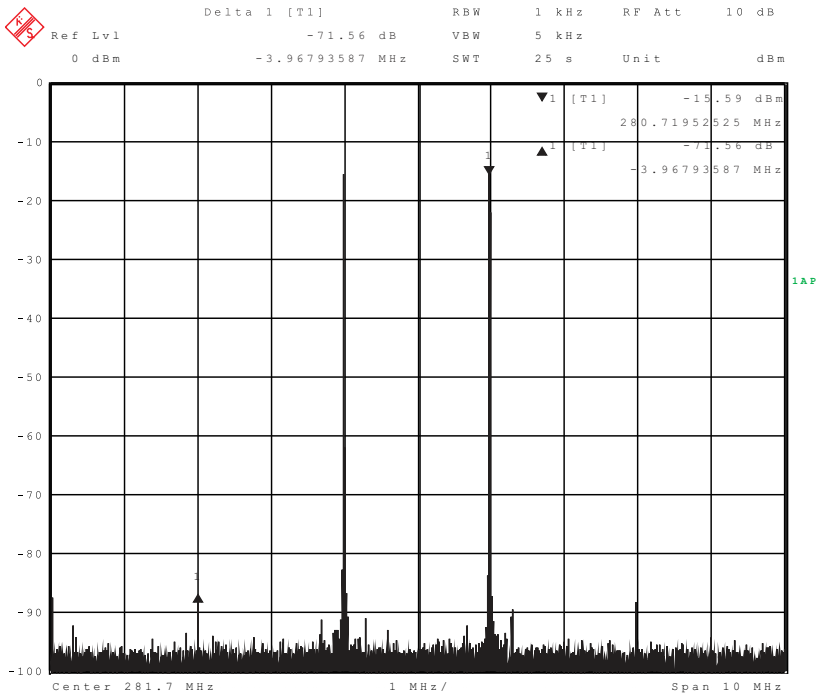


Figure 7.42: Measured IMD3 at a sampling frequency of $650MS/s$ *with two tone input at 280 MHz and 282 MHz*

Two tone measurements are reported in Fig. 7.42 and 7.43. Fig 7.42 shows the spectrum measured at the output of the DAC with the two sine-waves located at $280.7MHz$ and $282.7MHz$, respectively, at a sampling rate of $650MS/s$.

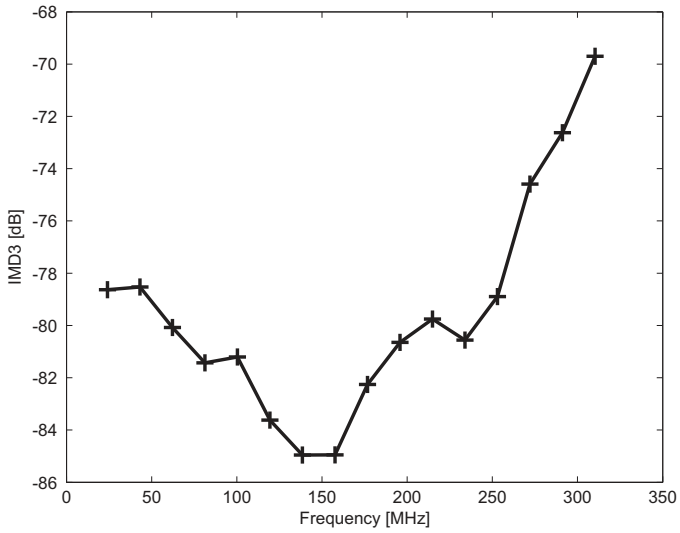


Figure 7.43: Measured IMD3 at a sampling frequency of $650MS/s$

The IMD3 is $-71.6dBc$. Fig 7.43 shows the IMD3 as function of the input frequency of the two tones again spaced $2MHz$ apart. From these figures it can be seen that the IMD3 remains $< -70dB$ up to $300MHz$.

7.7 Conclusions

In this chapter we have reviewed the basic function of the DAC and how the DAC is specified. Sofar, in literature, almost exclusively narrowband signals are being used to characterize and simulate the performance of the DAC. Since the properties of these narrowband signals are different compared to the broadband signals, a DAC that has good narrowband performance does not automatically also show good wideband performance.

For quantization effects the expected ACLR has been given and a formula is derived for a DAC whose performance is affected by a limited output impedance in the case that a wideband signal is applied to the DAC. When the DAC is af-

fected by non-idealities and the signals that are being converted have wideband properties, error mechanisms that create distortion around the mid-scale transitions are more dominant in the performance of the system then error mechanisms that create distortion at the extremes of the amplitude range. When the DAC performance is affected by output conductance, a higher output conductance is allowed to achieve a similar performance for wideband signals than for a narrowband signal.

A similar analysis has been done for a DAC that suffers from mismatch in the amplitudes of the current sources. Using full binary DACs or DACs with a low segmentation result in a higher distortion for signals that have wideband properties than for narrowband signals. The distortion that is generated by local timing variation due to mismatch was reviewed for wideband signals.

From these analyses the requirements for the DAC specifications were determined and the architecture was defined to have 5 bit thermometer coded and 7 bits binary coded. The allowed capacitance on the drain of the cascoded current source was determined to be less than 50fF and the spread in the mismatch of the current sources should be smaller than 0.01%.

In the DAC a new topology for the decoder has been used to enable high speed operation. Various aspects, such as the output transformer configuration, cascode transistors and bias methods, have been analyzed and compared to select the best alternative solution. The output transformer configuration is selected to use a center tap for the DC biasing of the DAC output and an internal 100 Ω resistor between the differential output. The DAC output stage uses cascoding for the current source transistor to reduce the parasitic capacitance on the common source node of the switches and also uses cascoding for the switches to reduce the coupling between the output signal and the switches. For the unit array voltage biasing is selected as the reference source, except for the current source cascode transistor which uses current biasing. This voltage biasing requires careful layout of the power supplies to ensure that the voltage drop over these connections is equal for every element.

The INL, SFDR, and IMD3 results have been measured of the DAC. These measurements show that the SFDR is dominated by the second harmonic and

better than $-56dB$ over the complete Nyquist frequency at a clock frequency of $650MS/s$. The IMD3 is better than $70dB$ over the complete Nyquist range and for signal frequencies up to $250MHz$ better than $-78dBc$.

8

Full DOCSIS transmitter implementation

In this chapter the new full DOCSIS transmitter IC implementation and the IC measurements are discussed. The proposed 'all-digital' architecture is compared to the multi-DAC DOCSIS transmitter that is described in Chapter 4.

8.1 DOCSIS transmitter IC implementations

Two implementations of the 'All-digital' transmitter have been made. The first implementation uses CML logic for the DSP core to prevent interference from the digital circuits as much as possible while the second implementation uses a conventional static CMOS implementation for the DSP core with a poly-phase clock to reduce the interference.

8.1.1 Transmitter IC with CML DSP

The floorplan of the proposed DOCSIS transmitter with a DSP made with CML logic is shown in Fig. 8.1 and the IC photograph is shown in Fig. 8.2. It shows the DAC core in the south east corner and the CML DSP in the north of the chip. The IC dimensions are 2.3x2.3mm^2.

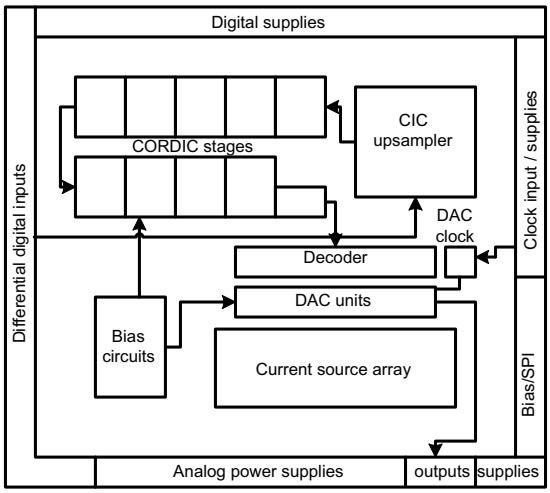


Figure 8.1: The floorplan of the IC with a CML DSP

Location of the pins

The location of the bondpads and pins is optimized such that the coupling between the different domains in the IC is minimized. The DAC core is supplied from the south side of the IC, where also the output is located. Supply pins are placed symmetrically around the differential output to reduce the effect of the coupling between the output signal and the supply pins through the bondwires.

The bias input currents are placed orthogonal to the DAC output which reduces the inductive coupling. The serial peripheral interface (SPI) pins are placed in the same domain. This SPI interface is used to program the settings of the IC, such as bias current levels and modulation frequency settings. During normal operation of the IC these pins are static and do not disturb the bias pins.

The clock inputs and its supplies are located in the north-east corner at some distance from the bias pins. Coupling between the clock pins and the bias pins should be reduced as much as possible. However, since the bias network has a large parasitic capacitance, the clock frequency components that couple on it is filtered.

The digital supplies are located at the north side. Since the CML core can

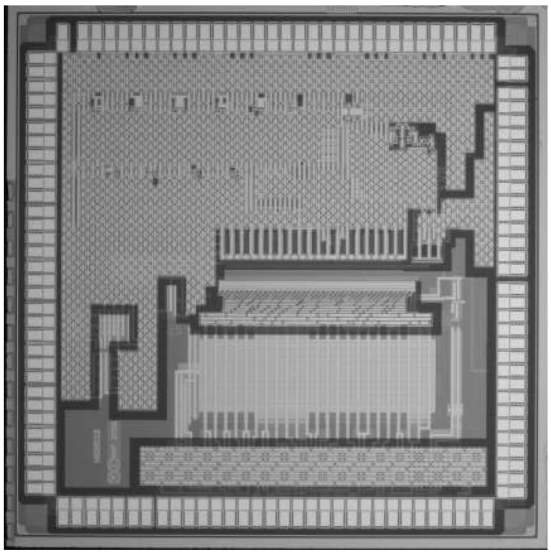


Figure 8.2: Photograph of the IC with a CML DSP

consume a lot of power, many pins are required to supply the power.

Finally, the west side of the IC contains the input pins. To reduce the effect of coupling of the input data bits to the analog supply domain, the LSBs are located at the south side and the MSB bits at the north side. Coupling between the LSB bit and the analog supply domain has commonly less influence on the performance than coupling between the MSB bit and the analog supply domain, because the LSB bit is only weakly correlated to the signal that is being converted, while this is far less the case for the MSB bit.

Placement of the blocks

The CIC upsampler is placed in the north-east corner of the IC. From there the signal is routed to the 10 CORDIC stages which are folded to reduce the length of the circuit. In the south west corner the bias network is placed, which is split into four parts, two for the analog functions, one for the clock and one for the digital circuits. The empty space between the blocks is filled by tiles that are used to supply the circuits with power and at the same time to decouple

these supplies. This is done by placing alternating vdd and ground connections next to each other and on each layer.

8.1.2 Transmitter IC with CMOS DSP

The floorplan of the proposed DOCSIS transmitter with a DSP made with CMOS logic is shown in Fig. 8.3 and the IC photograph is shown in Fig. 8.4. The IC dimensions are 2.6x2.6mm^2.

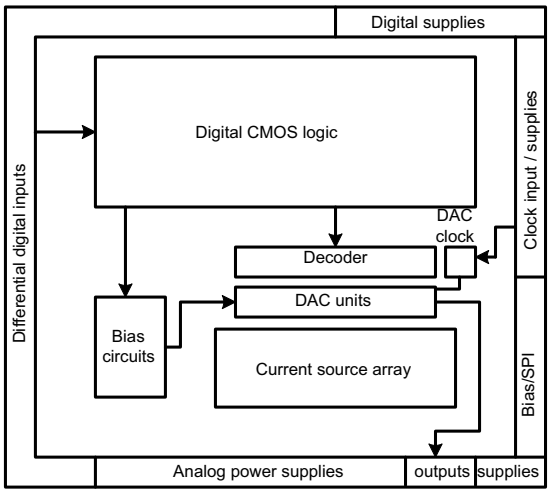


Figure 8.3: The floorplan of the IC with a CML DSP

The general floorplan of the CMOS DSP transmitter IC is comparable to the CML DSP transmitter IC. The CML logic is replaced by synthesized VHDL coded logic. The total IC area is larger because the input signal to the DAC can be a complex I/Q signal, instead of an interleaved I/Q signal as used in the CML transmitter version. Using parallel I/Q paths have as advantage that the data rate at the input can be two times lower. Because the power consumption of the static CMOS logic is lower compared to the CML logic, less supply pins are used for the digital power supply.

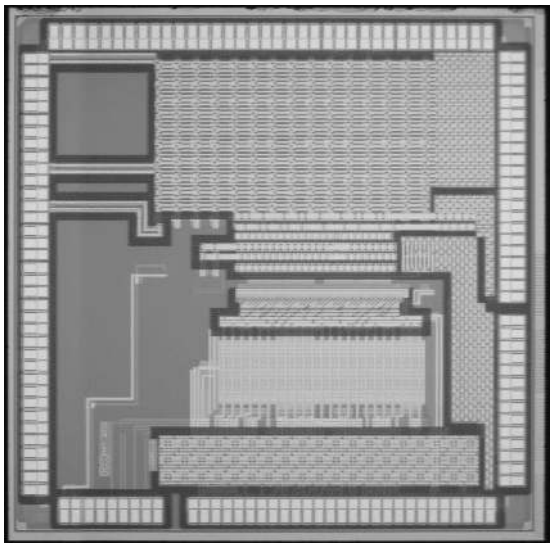


Figure 8.4: Photograph of the IC with a CMOS DSP

8.2 DOCSIS transmitter measurements

In Chapter 7 the measurements related to the DAC have been discussed. In this section the measurements of the full IC implementation which consist of the DAC and the DSP will be discussed.

8.2.1 Power consumption in CML DSP

The power consumption of the digital CML circuits was estimated in Chapter 6.4 to be about 1.6W. Measurements of the IC show that the power consumption of the digital circuits can vary between $720mW$ to over $2.1W$, depending on the bias current setting that is used for the logic. To simplify the debugging and analysis of the transmitter IC, all bias currents that are used in the chip can be varied. The tuning range of the bias current range is in the ideal case from -50 % to +50%. Given the calculated power of $1.6W$ this would result in a power consumption of $800mW$ to $2.4W$. The tuning range at the lower side correlates well to the expected value. At the upper side the current of the

current source transistors of the CML circuits do not increase anymore because of voltage headroom limitations, as was expected from simulations. The power consumption is therefore limited to a lower value than would be expected given the tuning range.

When the tail current of the CML logic is reduced, the maximum operation speed is reduced as well. With nominal bias settings the operation speed was limited to about $2400MS/s$. To reach the targeted operation speed of $2744MS/s$ the current of the logic gates had to be increased by about 40% above the nominal value. This is most likely caused by supply drop in the connection to the IC and inside the IC. The voltage drop in the supply cable alone to the PCB was already equal to about 50mV for the V_{DD} and ground connection, which is significant when the supply voltage is equal to 1.2V. To compensate for this drop, the supply voltage was increased with 50mV. The resistance of the bondwires and the internal metal might explain the difference between the expected performance and the measured performance. To reach this speed a small heat sink was required to cool the chip, because of the limited thermal capacity of about 40K/W for the package, HTQFP100, that is used.

8.2.2 Power consumption in CMOS DSP

In Chapter 6.4 the power consumption of the digital CMOS circuits was estimated to be about $650mW$ for a typical use case, in the typical process corner and nominal temperature.

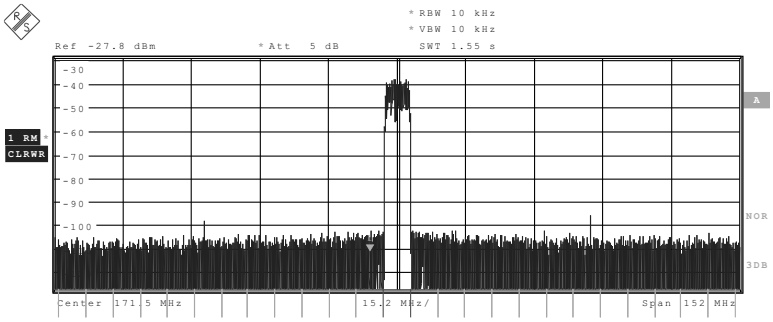
The measured power consumption with a DC input while the modulator is active, i.e. a sinewave generator, the power consumption was about $500mW$ at $2800MS/s$, while for a broadband signal at $1900MS/s$ the power consumption was about $540mW$. The exact power consumption varies depending on the frequency tuning word that is used for the modulator and the amplitude range of the input signal. This is caused by the fact that the power of CMOS logic is mainly consumed when bit change their states and the exact activity factor of a circuit depends on the input signals to this circuit.

8.2.3 ACLR performance

In Fig. 8.5 to Fig. 8.7 the ACLR performance of the transmitter is shown for 1 to 16 channels each $6MHz$ wide which are centered around a frequency of about $170MHz$. The DAC is clocked at a frequency of about $4x475MS/s$. The external data generator that was used to evaluate the performance of the transmitter was capable of delivering data with a sample rate of 475MS/s. In combination with the four times upsampling of the DSP the final sample rate of the DAC is equal to about $1900MS/s$. Without external data the transmitter was capable of achieving a sample rate of $3200MS/s$.

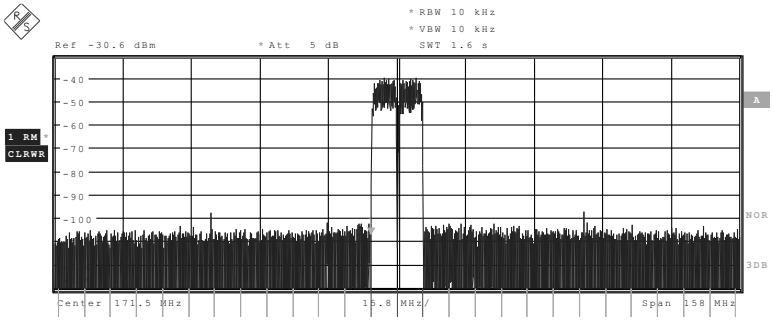
Compared to the specifications as are given in Table 3.3, it shows that the adjacent and the alternate channels comply to the mask requirements for all the tested number of channels. However, for the 2nd alternate and further alternate channels the mask requirements are violated. This is caused by the wideband noise being too high or the signal energy being too low. To avoid compression in the output signal, thereby generating a lot of distortion, the signal amplitude had to be reduced by about $6dB$ below the targeted signal power.

In Fig. 8.8 to Fig. 8.10, the ACLR plots are shown for a center frequency of about $880MHz$. At this frequency also the adjacent and the alternate ACLR do not comply to the mask requirements set by the DOCSIS standard anymore. We will further discuss this further on.



Channel	Bandwidth	Spacing	Lower	Upper
Tx Channel	6.000 MHz		-16.50 dBm	
Adjacent	6.000 MHz	6.000 MHz	-65.87 dB	-64.77 dB
Alternate	6.000 MHz	12.000 MHz	-67.56 dB	-67.38 dB
2nd Alt	6.000 MHz	18.000 MHz	-68.79 dB	-68.10 dB
3rd Alt	6.000 MHz	24.000 MHz	-69.14 dB	-68.85 dB
4th Alt	6.000 MHz	30.000 MHz	-69.66 dB	-69.65 dB
5th Alt	6.000 MHz	36.000 MHz	-69.92 dB	-69.85 dB
6th Alt	6.000 MHz	42.000 MHz	-69.72 dB	-68.92 dB
7th Alt	6.000 MHz	48.000 MHz	-70.51 dB	-69.45 dB
8th Alt	6.000 MHz	54.000 MHz	-70.24 dB	-69.74 dB
9th Alt	6.000 MHz	60.000 MHz	-70.91 dB	-70.00 dB
10th Alt	6.000 MHz	66.000 MHz	-71.20 dB	-69.62 dB
11th Alt	6.000 MHz	72.000 MHz	-71.26 dB	-69.52 dB

(a) 1 channel

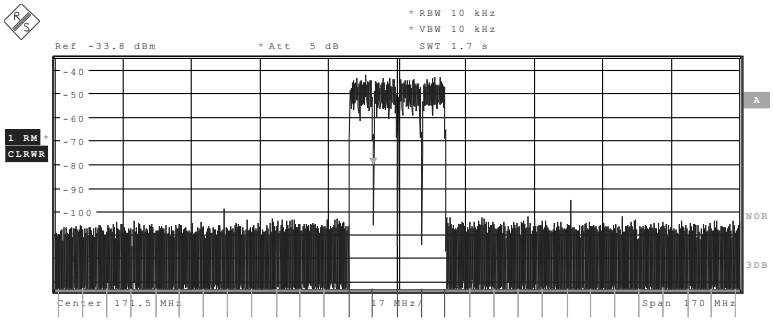


Standard: NONE

Tx Channels			Lower dB	Upper dB
Ch1 (Ref)	-19.23 dBm	Adjacent	-64.22	-63.77
		Alternate	-65.15	-65.01
Ch2	-19.33 dBm	2nd Alt	-66.48	-65.23
		3rd Alt	-66.71	-65.72
Total	-16.27 dBm	4th Alt	-67.10	-66.09
		5th Alt	-67.07	-66.44
		6th Alt	-67.18	-65.54
		7th Alt	-67.24	-66.24
		8th Alt	-67.44	-66.93
		9th Alt	-67.85	-66.92
		10th Alt	-67.76	-67.49
		11th Alt	-68.46	-67.57

(b) 2 channels

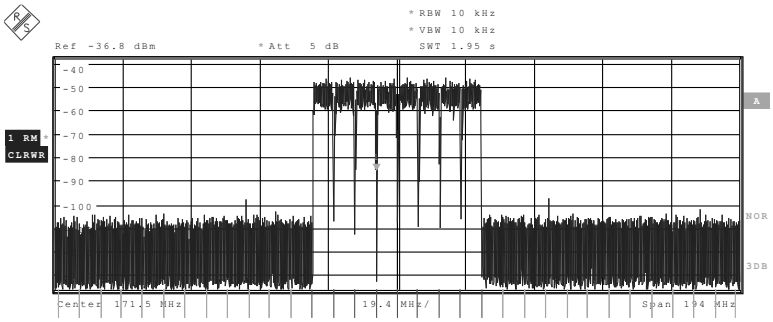
Figure 8.5: The measured ACLR for 1 and 2 channels at a center frequency of about 170MHz



Standard: NONE

Tx Channels			Lower dB	Upper dB
Ch1 (Ref)	-22.24 dBm	Adjacent	-62.71	-61.88
Ch2	-22.40 dBm	Alternate	-62.91	-62.21
Ch3	-22.38 dBm	2nd Alt	-62.63	-63.09
Ch4	-22.24 dBm	3rd Alt	-64.20	-62.51
		4th Alt	-63.54	-63.13
Total	-16.29 dBm	5th Alt	-63.95	-62.72
		6th Alt	-64.43	-63.08
		7th Alt	-64.37	-63.67
		8th Alt	-64.26	-63.30
		9th Alt	-64.08	-63.37
		10th Alt	-64.78	-63.79
		11th Alt	-64.93	-63.86

(a) 4 channels

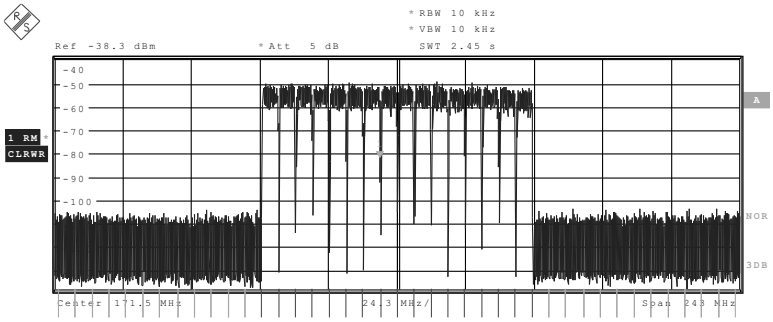


Standard: NONE

			Lower dB	Upper dB
Ch1 (Ref)	-25.28 dBm	Adjacent	-60.61	-59.26
Ch2	-25.31 dBm	Alternate	-60.38	-60.19
Ch3	-25.33 dBm	2nd Alt	-60.48	-60.58
Ch4	-25.77 dBm	3rd Alt	-60.06	-59.95
Ch5	-25.49 dBm	4th Alt	-60.63	-60.38
Ch6	-25.46 dBm	5th Alt	-61.83	-60.06
Ch7	-25.77 dBm	6th Alt	-61.24	-60.62
Ch8	-25.74 dBm	7th Alt	-61.88	-60.30
Total	-16.48 dBm	8th Alt	-61.33	-60.21
		9th Alt	-61.40	-60.74
		10th Alt	-62.03	-60.29
		11th Alt	-61.68	-61.01

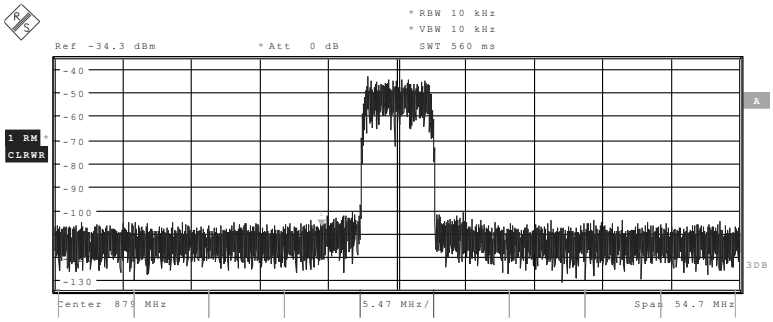
(b) 8 channels

Figure 8.6: The measured ACLR for 4 and 8 channels at a center frequency of about 170MHz



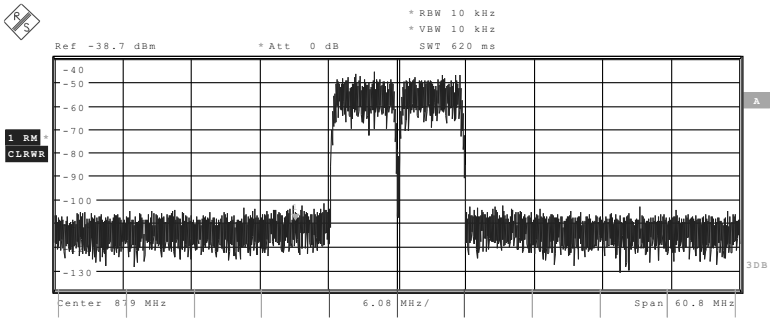
Standard: NONE					Lower	Upper
	dBm		dBm		dB	dB
Ch1(Ref)	-28.35	Ch10	-28.21	Adjacent	-57.62	-56.13
Ch2	-27.98	Ch11	-28.63	Alternate	-58.02	-57.09
Ch3	-27.99	Ch12	-29.10	2nd Alt	-57.80	-57.50
Ch4	-28.19	Ch13	-28.67	3rd Alt	-58.13	-57.85
Ch5	-28.22	Ch14	-28.90	4th Alt	-58.26	-57.05
Ch6	-28.38	Ch15	-29.31	5th Alt	-58.27	-57.76
Ch7	-28.51	Ch16	-29.78	6th Alt	-57.49	-56.63
Ch8	-28.53			7th Alt	-57.93	-57.07
Ch9	-28.40			8th Alt	-57.99	-57.02
				9th Alt	-57.53	-57.62
				10th Alt	-57.69	-56.63
Total	-16.51 dBm			11th Alt	-56.45	-56.48

Figure 8.7: The measured ACLR for 16 channels at a center frequency of about 170MHz



Channel	Bandwidth	Spacing	Lower	Upper
Tx Channel	6.000 MHz		-24.66 dBm	
Adjacent	6.000 MHz	6.000 MHz	-58.33 dB	-58.43 dB
Alternate	6.000 MHz	12.000 MHz	-60.89 dB	-60.72 dB
2nd Alt	6.000 MHz	18.000 MHz	-60.92 dB	-60.83 dB
3rd Alt	6.000 MHz	24.000 MHz	-60.77 dB	-61.05 dB

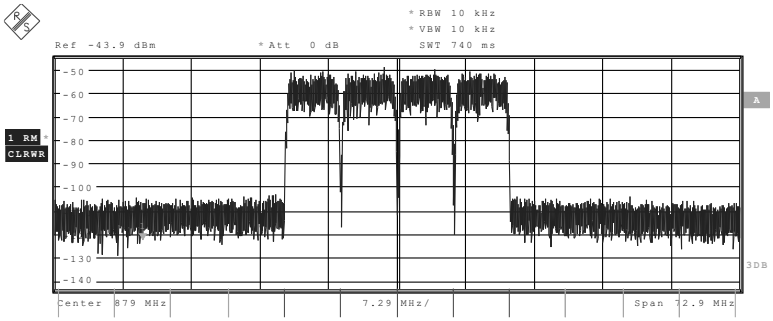
Figure 8.8: The measured ACLR for 1 channel at a center frequency of about 880MHz



Standard: NONE

Tx Channels			Lower dB	Upper dB
Ch1 (Ref)	-27.83 dBm	Adjacent	-55.43	-55.47
Ch2	-27.77 dBm	Alternate	-57.06	-57.15
		2nd Alt	-57.25	-57.56
Total	-24.79 dBm	3rd Alt	-57.68	-57.59

(a) 2 channels

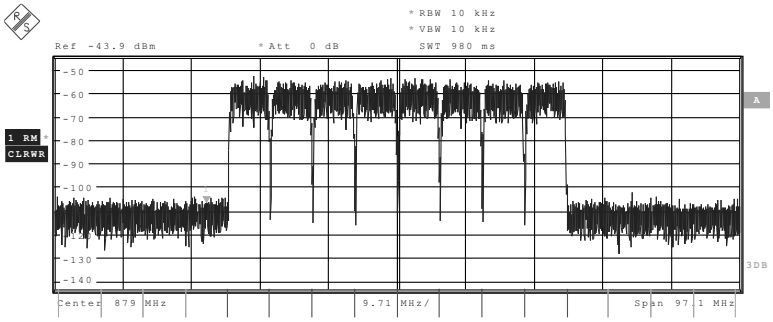


Standard: NONE

Tx Channels			Lower dB	Upper dB
Ch1 (Ref)	-31.30 dBm	Adjacent	-52.13	-52.22
Ch2	-30.94 dBm	Alternate	-52.67	-53.25
Ch3	-30.83 dBm	2nd Alt	-53.15	-53.83
Ch4	-30.96 dBm	3rd Alt	-53.88	-54.52
Total	-24.98 dBm			

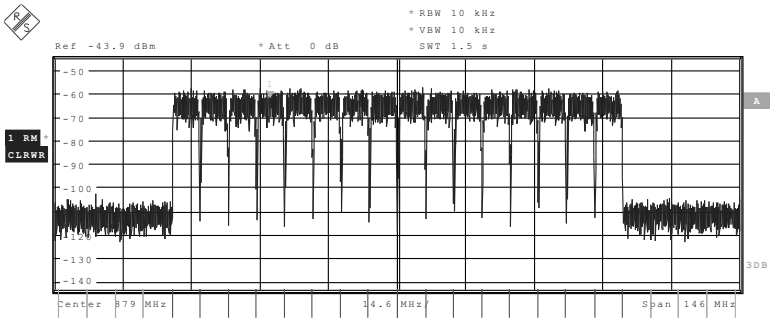
(b) 4 channels

Figure 8.9: The measured ACLR for 2 and 4 channels at a center frequency of about 880MHz



Standard: NONE			Lower dB	Upper dB
Ch1 (Ref)	-34.09 dBm	Adjacent	-49.67	-49.71
Ch2	-34.11 dBm	Alternate	-50.20	-50.50
Ch3	-34.12 dBm	2nd Alt	-50.07	-50.91
Ch4	-34.02 dBm	3rd Alt	-50.12	-51.06
Ch5	-33.72 dBm			
Ch6	-34.37 dBm			
Ch7	-34.36 dBm			
Ch8	-34.17 dBm			
Total	-25.09 dBm			

(a) 8 channels



Standard: NONE				Lower dB	Upper dB
	dBm		dBm		
Ch1(Ref)	-37.48	Ch10	-36.99	Adjacent	-46.68	-46.00
Ch2	-37.53	Ch11	-37.21	Alternate	-47.29	-46.37
Ch3	-37.25	Ch12	-37.21	2nd Alt	-47.15	-46.95
Ch4	-36.92	Ch13	-36.77	3rd Alt	-46.75	-46.51
Ch5	-36.89	Ch14	-37.02			
Ch6	-37.41	Ch15	-37.76			
Ch7	-37.13	Ch16	-37.51			
Ch8	-37.11					
Ch9	-36.83					
Total	-25.14 dBm					

(b) 16 channels

Figure 8.10: The measured ACLR for 8 and 16 channels at a center frequency of about 880MHz

8.3 CMOS DSP vs CML DSP

Since the CML transmitter version and the CMOS transmitter version use the same DAC core implementation their measured performance is similar. As can be observed in Fig. 8.6(a), which is measured for the CMOS implementation, some spurs originating from the clock of the digital circuits are visible. These spurs are caused by the digital CMOS circuits that operate at a 1/4 of the clock rate of the DAC. Although poly-phase clocking of these circuits is used, the loading of different phases of the circuit are not exactly equal to each other. This will limit the suppression of the spurs. However, the levels of these spurs are low and their energy is low enough, such that they do not noticeably affect the ACLR performance. In the CML version these spurs are not observed, since all the circuits are clocked at the same clock frequency as the clock of the DAC all the spurs that are generated will fall on frequencies outside the bandwidth of interest. In addition, due to the differential nature of the CML logic the generated interference is also lower.

Since the power consumption of the CML circuit is much higher and the implementation of the CML logic is much more labor intensive and the spur level of the CMOS version is at an acceptable level the CMOS DSP is the preferred DSP implementation style.

8.4 Proposed transmitter vs traditional transmitter

In Chapter 5 the 'All-digital' transmitter concept was introduced. This potentially more advantageous system when many carriers have to be generated is given in Fig. 5.4. This 'All-digital' multi-carrier transmitter is based on digitally combining multiple single-carrier transmitters as is shown in Fig. 5.2. All the mixing and modulation of the carriers is done in the digital domain. Therefore, only one accurate fixed frequency clock source is required, instead of multiple independent clock sources that are tunable over a large range. Extending the system such that more carriers can be transmitted becomes easier

as the main changes are in the digital domain.

In Chapter 6 the power consumption of the digital signal processing for the 'All-digital' transmitter architecture was estimated to be about $650mW$ for the main circuits of the CMOS DSP. The measured results at a sample rate of about $1900MS/s$ was equal to $540mW$. When this result is extrapolated to a sample rate of $2744MS/s$ a power consumption of about $800mW$ is expected. The difference between the measured power consumption and the calculated power consumption is mainly explained by the circuits that are not taken into account in the calculations of Chapter 6, such as the phase adders, clip counters and debug/test observation register.

The measured power consumption of the DAC for the CMOS and CML version is equal to $110mW$ for the analog circuits, $170mW$ for the decoder and $80mW$ for the clock circuits which results in a total power consumption of about $360mW$.

The clock source that is required for the 'All-digital' transmitter is assumed to be similar to the LO generator that is estimated in Chapter 4. Although the phase noise requirements of the 'All-digital' transmitter are more relaxed, the LO frequency is higher. The power consumption for the clock source was estimated to be about $200mW$ and this power consumption will be assumed here too.

In a similar way as described in Appendix A the power consumption of the upsampling of a single carrier from the data rate of 5.36MS/s to the input sample rate of $686MS/s$ using cascaded halfband filters can be estimated to be about $60mW$ each. Since the input signal is complex two of these upsamplers are needed, which gives about $120mW$.

For a single carrier transmitter using the 'All-digital' approach the total power consumption is estimated to be at a sample rate of $2744MS/s$:

Component	**Count**	**Power (mW)**	**Power consumption (mW)**
DAC	1	360	360
Clock	1	200	200
IF/RF DSP	1	800	800
Baseband to IF	2	60	120
Total			1480

Table 8.1: Estimated power consumption of a single carrier DOCSIS transmitter using the 'All-digital' transmitter approach using the CMOS DSP

In Chapter 4 the single carrier DOCSIS transmitter was analyzed which used the zero-IF, dual-conversion transmitter architecture. This architecture requires the least amount of digital signal processing and the requirements for the analog components are relatively moderate. The minimum total power consumption for the single carrier transmitter is estimated to be about $1.2W$ using the power consumption of the individual components, assuming that the interconnects between the components are lossless.

For a single carrier the power consumption is expected to be lower for the traditional transmitter. However, when the number of carriers increases, the power consumption of the traditional transmitter almost doubles, because only a few components, such as the LO1 generator which upconvertes the signal from the Zero-IF to the fixed high IF1 frequency, can be shared between the transmitters that broadcast on different frequencies. For the 'All-digital' transmitter approach, only the baseband to IF upconverter is added for each additional channel.

When the architecture of the 'All-digital' transmitter that is shown in Fig. 6.1 is used, where $N1$ is equal to 64 and $N2$ is equal to four, the estimated power consumption as a function of the number of carriers is given in Fig. 8.11. In the same figure the power consumption of the traditional dual conversion transmitter is shown. This analysis assumes that each transmitter broadcasts a single channel.

As can be observed from the figure, the 'All-digital' transmitter becomes attractive in terms of the power consumption for two channels or more, with the

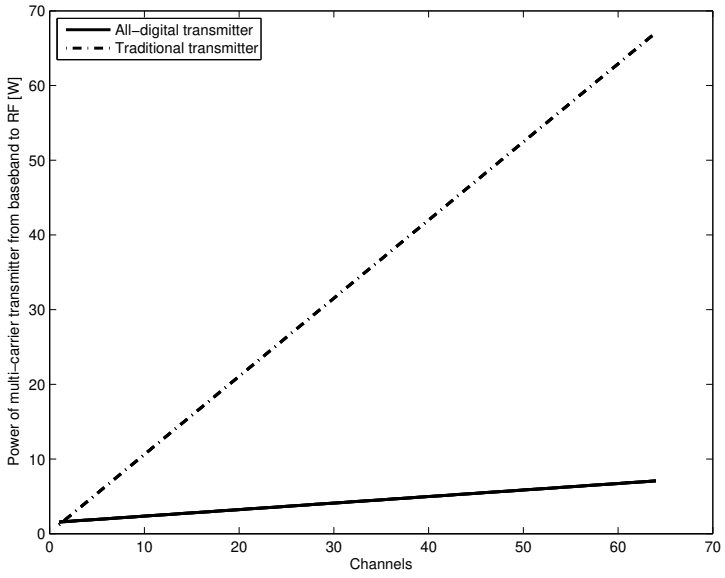


Figure 8.11: The estimated power consumption of the traditional dual-conversion transmitter and the 'All-digital' transmitter as function of the number of carriers.

additional advantage that the proposed transmitter requires less tuning and is less sensitive to effects such as aging.

8.5 Discussion on transmitter performance

To achieve high linearity the output amplitude of the signal had to be reduced more than was expected from simulations. While this reduction of the amplitude does not have an impact on figures such as SFDR and IMD3, wideband figures, however, such as ACLR are affected by thermal noise. Thereby, impeding the achieved performance.

To achieve better performance of the DAC a number of things could be improved in the DAC. Because the wideband noise is too high, this could be improved by increasing the number of bits from the current 12 bit to 14 bit. This will lower the quantization noise that is present in the signal. In addition,

the thermal noise of the DAC could be improved by allowing a larger overdrive voltage V_{gt} of the current source transistor. However, this will require a different distribution of the voltage headroom of the output stage. The output transistor stack is limited by the supply voltage of the switch driver. With the nominal supply voltage and the standard V_t of the transistors this is difficult to achieve. An option is to use low V_t transistors that are in principle available as an option at in the 90nm CMOS process of TSMC, but this option is currently not supported by NXP. The compression at the output could also be improved by using these low V_t transistors. Alternatively the thin-oxide switch cascode transistors could be replaced by thick oxide transistors, which improves the voltage headroom above the switches at the cost of additional parasitic capacitance at the output. Note that the headroom above the switches is independent of the headroom below the switches. This higher capacitance could attenuate the signal amplitude at higher signal frequencies more.

The most promising method to improve the performance of the converter is to apply a calibration method as described in [132]. This calibration method reorders the thermometer sources in such a way that the total error, being amplitude, skew and duty cycle errors, caused by mismatch errors is minimized. When this method is applied more mismatch can be tolerated in the transistors, which could be exploited to increase the voltage headroom and to reduce the parasitic capacitance on sensitive nodes.

8.6 Conclusions

In this chapter the integration aspects of the 'All-digital' DOCSIS transmitter has been discussed. Special emphasis has been made on preventing coupling between the circuits of the different components that are integrated on the same IC. In addition, the locations of the pins are optimized such that the impact of the inductive coupling between the bondwires is minimized. The chip floorplan and the photograph of the CML DSP version of the transmitter and the CMOS DSP version have been shown.

The ACLR results of the transmitter have been measured. For frequencies

up to $170MHz$, the DOCSIS mask requirements are met for the adjacent and alternate channel, but for the channels further from the modulation center frequency the noise floor is too high to comply to the mask requirements that are set by the DOCSIS standard. For higher center frequencies the ACLR performance does not meet the requirements anymore.

Since the power consumption of the CML circuit is much higher and the implementation of the CML logic is much more labor intensive and the spur level of the CMOS version is at an acceptable level the CMOS DSP is the preferred DSP implementation style. This shows that the the spurs can be kept under control even when standard CMOS logic is being used in combination with measures such as isolation and poly-clock phases.

A comparison between the multi-carrier transmitter which is constructed using the traditional transmitters and the multi-carrier 'All-digital' transmitter approach has been made. This comparison shows that for two or more carriers the 'All-digital' transmitter seems favorable in terms of the estimated power consumption.

9

General conclusions

In this chapter generic conclusions are drawn. For detailed conclusions regarding the contents of each chapter, the reader is referred to the corresponding chapters.

A new 'all-digital' transmitter concept has been given in this thesis which is favorable over the traditional transmitter in terms of power and area when more than two channels are being broadcasted. In this transmitter the majority of the analog components are replaced by digital circuits that do not require calibration or tuning and do not suffer from effects such as aging, thereby exploiting the advantage of the scaling properties of digital circuits in advanced CMOS technologies.

In this thesis the proposed multi-carrier DOCSIS transmitter is validated with both substantial theoretical analysis, synthesis concepts and experimental verification of a new approach of replacing the analog front-end in a DOCSIS transmitter by digital signal processing that upsamples, combines and upconverts the carriers, followed by a single DAC that generates the RF signal without further upconversion. One of the largest challenges in multi-carrier communication systems is their high peak-to-average power ratio. Selecting the clip-levels of the system such that clipping does not occur, would result in a non-optimal system. Therefore some clipping of the multi-carrier signal should be allowed. The clip level of the signal should be selected such, that the combined distortion due to quantization and clipping is minimized.

It has been shown that for the required performance using a traditional single carrier DOCSIS transmitter, a dual conversion transmitter architecture is required. Using such an architecture the minimum power consumption is estimated to be about 1.2W per channel that is being broadcasted. In the

'all-digital' transmitter these conversion steps are implemented in the digital domain.

The number of carriers that can be transmitted using a single 'all-digital' transmitter increases significantly, compared to the traditional analog dual conversion transmitter, because the complexity of the analog core of the 'all-digital' transmitter is independent of the number of channels. The 'all-digital' transmitter can broadcast all channels that could be present in the full DOCSIS band with a single DAC. The main limitation in the number of channels is the limit in power dissipation that can be handled by the package, since adding more channels does only affect the digital signal processing and does not increase the complexity in the analog domain.

It has been shown that the proposed multi-carrier DOCSIS transmitter can be more power and area efficient when multiple channels are being broadcasted than multiple traditional DOCSIS transmitters that have their outputs combined.

A new framework is given for modeling and analysis of current steering DAC performance in the case of broadband signals, and especially at high sample rates. For such broadband signals, error mechanisms that create distortion around the mid-scale transitions are more dominant in the performance of the system than error mechanisms that create distortion at the extremes of the amplitude range. Using fully binary DACs or DACs with a low segmentation results in a higher distortion for signals that have wideband properties than for narrowband signals. When the DAC performance is affected by output conductance, a higher output conductance is allowed to achieve a similar performance for wideband signals than for a narrowband signal.

The transmitter concepts have been used in a rationalized manner to design and implement a 12-bit $2.8GS/s$ DAC in combination with digital signal processing that upsamples, combines and upconverts the carriers in a 90nm CMOS process, which serves as a vehicle IC to verify the validity of the 'All-digital' transmitter concepts proposed in this thesis. Based on this DAC, three different versions of a complete 'all-digital' transmitter, which consist of a combination of the digital signal processing and a DAC, were designed and implemented as

ICs. The first two versions, the second being a redesigned version of the first one, use current mode logic for the digital signal processing, which is optimized to be able to run at the desired sample frequency of $2.8GS/s$. Since the digital signal processing is made in current mode logic and synchronous with the DAC clock, no interference is observed. The third version uses static CMOS logic in combination with several methods, such as the use of poly-clock phases, to reduce the interference from the digital signal processing to the sensitive analog circuits. It is shown that the combination of these techniques to reduce the interference is sufficient to achieve the required performance. The preferred logic style to implement the digital circuits is standard CMOS logic, which is efficient in terms of power consumption and effort to implement the digital circuits.

A

Power consumption estimations of the digital circuits

In this Appendix the power consumption of the digital circuits that are described in Chapter 6 is estimated using the methods given in Chapter 6.4. These calculations use the implemented designs, which are given in Chapter 6.3, as reference.

A.1 The static CMOS logic CORDIC

The equations that are given in Chapter 6.4 are used in this chapter to estimate the power consumption of the CORDIC. As is given in Chapter 6.2.4 the CORDIC consists of 14 stages with 20 bits word length for the data path and 16 bits word length for the angle. Using this information the number of gates can be estimated. The number of gates is normally expressed in the equivalent number of NAND gates for CMOS logic. To simplify the calculations it is assumed that the CORDIC uses three basic elements, namely full adders gates, multiplexers and d-flip-flops. Each of these three elements can be expressed in an equivalent number of NAND gates, which is 8, 2 and 8 respectively.

	Multiplexers	Full adders	Registers	Total
Stage 0	968	1732	464	3164
Stage 1	456	2014	448	2918
Stage 2	456	2014	448	2918
Stage 3	456	2014	448	2918
Stage 4	456	2014	448	2918
Stage 5	456	2014	448	2918
Stage 6	456	2014	448	2918
Stage 7	456	2014	448	2918
Stage 8	456	2014	448	2918
Stage 9	456	2014	448	2918
Stage 10	456	2014	448	2918
Stage 11	456	2014	448	2918
Stage 12	456	2014	448	2918
Stage 13	168	866	160	1194
Total	6616	27199	6320	40135

Table A.1: Equivalent gate count for the stages of the CORDIC for the three basic elements

Since the CORDIC has to operate at high sample rates, it is assumed that the data is reclocked at every stage to pipeline the circuit. In addition, the adder circuits are assumed to be optimized for speed. These assumptions put a limit on the lowest clock frequency for which the results are accurate. When the clock frequency is reduced too much, the synthesis tool will automatically select other, slower, architectures for the adders and remove pipelining stages, in order to optimize the circuit for power. For the adder circuits several high speed architectures do exist and are analyzed in [144, 145]. A common architecture of adders operating at these speeds is the Carry-Select Adder. In [145] the equivalent gate count of this architecture is given as

$$\#gates = 4n\log_2(n) + 2n - \log_2(n) - 2, \tag{A.1}$$

with a worst case gate delay of

$$\#gates\ delay = 2\sqrt{2n} + 2, \tag{A.2}$$

where n is the word length of the adder. The total equivalent gate count of the CORDIC is estimated to be about 40000 as given in Table A.1.

With this equivalent gate count and a value for the Rent's exponent of 0.5 [146] and an activity factor of 0.2 which is estimated from simulations and the process characteristics as are given in Table 5.2, the average interconnect length can be estimated using Eqn. 6.37 and Eqn. 6.41, and is given in Table A.2.

Using the dimensions of the CMOS 90nm process, the capacitance per unit of length as defined in Eqn. 6.42 to Eqn. 6.46 the C_{wire} can be approximated as 2.3 $[pF/m]$.

Using Eqn. 6.41 and taking the maximum fanout to be 8[1] the number of connections for the first four fanouts can be estimated to be

$$\begin{array}{rlll} 61\ \%, & \text{fanout } =1, & L_{avg} = 21.6\mu m, & C_L = 8fF \\ 19\ \%, & \text{fanout } =2, & L_{avg} = 30.2\mu m, & C_L = 13fF \\ 8\ \%, & \text{fanout } =3, & L_{avg} = 39.0\mu m, & C_L = 18fF \\ 5\ \%, & \text{fanout } =4, & L_{avg} = 47.5\mu m, & C_L = 23fF \end{array}$$

Table A.2: The average interconnect length, fanout and parasitic capacitance

The estimate the power consumption of the CORDIC, Eqn. 6.35 is being used, which gives

$$P_{CORDIC} = \sum_{Ng} \alpha f C_L V_{DD}^2, \tag{A.3}$$

where N_g is the number of gates. For the 90nm CMOS process with a supply voltage of $1.2V$ and a clock frequency of $2744MS/s$ / $4 = 686MS/s$, the power is estimated to be $87mW$. The CORDIC is placed 4 times, therefore the total estimated power is equal to $348mW$.

[1] This equation is estimated in [111] reliable up to a fanout of 8. The number of connections with a certain fanout can be estimated by taking a maximum fanout and assuming that all connections (100%) have a fanout smaller or equal to this maximum fanout.

A.2 The static CMOS logic poly-phase upsample FIR filter

Similar to the previous estimation of the power consumption of the CORDIC, the power consumption of the poly-phase upsample FIR filter will be estimated. The equations are based on the equations that are given in Chapter 6.4.

As is given in Chapter 6.2.3 the poly-phase upsample FIR filter consists of 4 phases with each a $N = 9$ taps FIR filter, giving a total of 36 coefficients. The word length for the coefficients is set to $CL = 14$ bits and the input data word length is equal to $IL = 12$ bit. Using this information the number of gates can be estimated. The number of gates is normally expressed in the equivalent number of NAND gates for CMOS logic. To simplify the calculations it is assumed that the FIR filter uses two basic elements, namely full adders gates and flip-flops. Each of these two elements can be expressed in an equivalent number of NAND gates, which is equal to 8 for both.

The coefficients that are used in the filter are fixed, therefore the multipliers can be optimized for these values. A common method of carrying out multiplications by a constant value is by using a sequence of shifts and adds. To reduce the number of adders and subtractors, the Canonic Signed Digit (CSD) format is often used. The advantage of the CSD format is that no value has more than (q +1)/2 non zero bits, often fewer, where q is the word length. Multiplication by a constant requires no more than q number of additions for its implementation. The actual number depends on the accuracy of the coefficients. As the accuracy decreases the frequency response of the filter degrades and the filters stop band attenuation decreases. As a rule of thumb [90], the number of CSD digits for a coefficient multiplication, is one non-zero digit for every $20dB$ of stopband attenuation for each coefficient as given in Chapter 6.2.3. Since about $80dB$ of suppression was required, the expected number of additions for each multiplication is $C = 4$.

For the filter architecture the transposed direct form has been selected. This architecture has as advantage that the coefficient multipliers all have the same input. Therefore common subexpressions in the coefficients can be combined.

Combining all common subexpressions can reduce the number of adders in the multiplier by a factor of $G = 2.1$ [90].

Using these approximations the number of full adders that are required is given by

$$\#FAs = \frac{N \cdot C}{G}(CL + IL + \lceil \log_2(N) \rceil), \tag{A.4}$$

where FAs is the estimated number of full adders for calculations of the coefficients. In a similar way the number of registers can be estimated

$$\#FFs = N(CL + IL + \lceil \log_2(N) \rceil) + 2IL. \tag{A.5}$$

The last equation assumes that all the number of adders per coefficient, C, can be calculated within one clock cycle. At higher operating frequencies, additional pipelining is required between these adders. The number of additional registers is given by

$$\#FFs = \frac{N(CL + CI)}{G} \cdot \left\lceil \frac{C}{NA} \right\rceil, \tag{A.6}$$

where NA is the number of additions that can be performed within a clock cycle. At the frequency at which the filter is operating, NA is equal to 1. In Table A.3 the number of elements for the filter given in Chapter 6.2.3 and its equivalent gate count is given.

Since the filter is used as a complex filter the numbers that are given before must be doubled. With this equivalent gate count and a value for the Rent's exponent of 0.6 [146] and an activity factor of 0.25 which is estimated from simulations and the process characteristics as are given in Table 5.2, the average interconnect length can be estimated using Eqn. 6.37 and Eqn. 6.41, and is given in Table A.4. The value for the Rent's exponent is higher than in the case of the CORDIC because the filters coefficient calculations requires more irregular interconnect. The complexity of the layout is therefore larger.

	Full adders	Registers	Total
Cells	1029	1479	2508
Equivalent number of gates	8229	11835	20064

Table A.3: Equivalent gate count for the poly-phase upsample FIR filter for the two basic elements

Using the dimensions of the CMOS 90nm process, the capacitance C_{wire} per unit of length as defined in Eqn. 6.42 to Eqn. 6.46 can be approximated as 2.3 $[pF/m]$.

Using Eqn. 6.41 the number of connections with a given fan-out can be estimated to be

$$\begin{array}{rlll} 60\ \%, & \text{fanout } =1, & L_{avg} = 23.9\mu m, & C_L = 9fF \\ 19\ \%, & \text{fanout } =2, & L_{avg} = 33.4\mu m, & C_L = 14fF \\ 9\ \%, & \text{fanout } =3, & L_{avg} = 52.6\mu m, & C_L = 25fF \\ 5\ \%, & \text{fanout } =4, & L_{avg} = 62.2\mu m, & C_L = 36fF \end{array}$$

Table A.4: The average interconnect length, fanout and parasitic capacitance

The estimate of the power consumption of the complex FIR filter is then calculated by using Eqn. 6.35

$$P_{filter} = \sum_{Ng} \alpha f C_L V_{DD}^2, \tag{A.7}$$

where N_g is the number of gates. For the 90nm CMOS process with a supply voltage of $1.2V$ and a frequency of $2744MS/s$ / $4 = 686MS/s$, the power is estimated to be $67mW$. For the poly phase filter four of these phases are required, the total power is therefore equal to $268mW$.

A.3 The static CMOS logic halfband upsampling filter

Similar to the previous estimation of the power consumption of the poly phase upsample FIR filter, the power consumption of the final 4 times upsampling with two complex halfband filters will be estimated. These estimations are based on the equations that are given in Chapter 6.4.

As is given in Chapter 6.2.3 the halfband FIR filter with a passband similar to the passband of the poly phase FIR filter requires at least 15 and 12 coefficients, for the first and the last stage, respectively. The word length for the coefficients is set to $CL = 14$ bits and the input data word length is equal to $IL = 12$ bit. Using this information the number of gates can be estimated. The number of gates is normally expressed in the equivalent number of NAND gates for CMOS logic. To simplify the calculations it is assumed that the FIR filter uses two basic elements, namely full adders gates and flip-flops. Each of these two elements can be expressed in an equivalent number of NAND gates, which is equal to 8 for both.

The coefficients that are used in the filter are fixed, therefore the multipliers can be optimized for these values. A common method of carrying out multiplications by a constant value is by using a sequence of shifts and adds. As is given in Chapter A.2, the expected number additions for each multiplication is $C = 4$. As described before combining all common subexpressions can reduce the number of adders in the multiplier by a factor of $G = 2.1$.

Using these approximations the number of full adders that are required is given by Eqn. A.4 and the number of registers can be estimated using Eqn. A.5 and Eqn. A.6. Since the clock frequency doubles for every next stage is the time that is available for the calculations reduced for every consecutive stage, as given in Chapter 6.2.3. In Table A.5 the number of elements for the in Chapter 6.2.3 given filter and its equivalent gate count is given.

Since the filter is used as a complex filter the numbers that are given before must be doubled. With this equivalent gate count and a value for the Rent's exponent of 0.6 [146] and an activity factor of 0.25 which is estimated from

Cells Complex Halfband filter	Full adders	Registers	Total
Filter 1	1714	2062	3776
Filter 2	1372	2550	3922
Total	3086	4612	7698

Table A.5: Equivalent gate count for the two halfband upsample FIR filters with the two basic elements

simulations and the process characteristics as are given in Table 5.2, the average interconnect length can be estimated using Eqn. 6.37 and Eqn. 6.41, and is are given below. The capacitance C_{wire} is equal to the before estimated capacitance of 2.3 $[pF/m]$ for the CMOS 90nm process.

Using Eqn. 6.41 the number of connections with a given fan-out for the first halfband filter can be estimated to be

$$\begin{array}{rlll} 60\ \%, & \text{fanout } =1, & L_{avg} = 25.4\mu m, & C_L = 9fF \\ 19\ \%, & \text{fanout } =2, & L_{avg} = 35.6\mu m, & C_L = 14fF \\ 9\ \%, & \text{fanout } =3, & L_{avg} = 45.8\mu m, & C_L = 20fF \\ 5\ \%, & \text{fanout } =4, & L_{avg} = 56.0\mu m, & C_L = 26fF \end{array}$$

Table A.6: The average interconnect length, fanout and paracitic capacitance of the first halfband filter

Using Eqn. 6.41 the number of connections with a given fan-out for the second halfband filter can be estimated to be

$$\begin{array}{rlll} 60\ \%, & \text{fanout } =1, & L_{avg} = 25.6\mu m, & C_L = 9fF \\ 19\ \%, & \text{fanout } =2, & L_{avg} = 35.8\mu m, & C_L = 15fF \\ 9\ \%, & \text{fanout } =3, & L_{avg} = 46.1\mu m, & C_L = 20fF \\ 5\ \%, & \text{fanout } =4, & L_{avg} = 56.3\mu m, & C_L = 26fF \end{array}$$

Table A.7: The average interconnect length, fanout and parasitic capacitance of the second halfband filter

The estimate of the power consumption of the filter is then calculated by using Eqn. 6.35

$$P_{filter} = \sum_{Ng} \alpha f C_L V_{DD}^2, \tag{A.8}$$

where N_g is the number of gates. For the 90nm CMOS process with a supply voltage of $1.2V$ and a frequency of $2744MS/s$ / $4 = 686MS/s$, for the first stage the power is estimated to be $104mW$ and $2744MS/s$ / $2 = 1372MS/s$ the power is estimated to be $216mW$. The total power for the two stages is equal to $320mW$.

A.4 The CML logic DSP

For the estimation of the power consumption of the CML DSP, the method as described in Chapter 6.4.2 is used. The implemented CIC filter consists of 5 stages with a maximum upsample rate of 16. The total number of comb cells is equal to 65 and the total number of integrator cells is 100. The integrator stage is fully pipelined to achieve the required operation speed. The total equivalent number of cells is equal to 2040, with a tail current of $40\mu A$ each upsampler for the I/Q path requires about $250mW$ including the clock network. More details about the implementation can be found in [147].

The power of the CORDIC can be calculated in a similar way as for the CIC. The CML CIC has 10 stages with an angle word length of 12 bits and 13 bits data word length. In Table A.8 the number of elements is shown for this mixer for the various stages.

The number of elements for				
	Multiplexers	Full adders	Registers	Total
Stage 0	73	24	302	399
Stage 1	73	24	302	399
Stage 2	39	38	570	647
Stage 3	39	38	552	629
Stage 4	39	38	536	613
Stage 5	39	38	522	599
Stage 6	39	38	510	587
Stage 7	39	38	500	577
Stage 8	39	38	492	569
Stage 9	14	38	243	295
Total	400	376	4763	5539

Table A.8: Equivalent gate count for the CORDIC

The total number of equivalent gates is equal to 14062. With a tail current of $40\mu A$ each and including the clock network this results in an estimated power consumption of $1.35W$.

The total estimated power consumption of the DSP which consists of the CIC and the CORDIC is therefore estimated to be $1.6W$, independent of the clock frequency or the data activity.

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Summary
Multi-carrier single-DAC transmitter approach applied to digital cable television

Traditionally the front-end of a transmitter for cable television designed for the DOCSIS standard consists of a combination of multiple DACs and analog mixers. In this traditional transmitter architecture, in each front-end a single carrier is converted in a DAC and upconverted to the desired RF frequency. This research work analyzes and realizes a new approach of replacing this analog front-end in the transmitter by digital signal processing that upsamples, combines and upconverts the carriers, followed by a single DAC that generates the RF signal without further upconversion.

The new approach has the advantage that the complexity of a multi-carrier transmitter is reduced, because less analog components are required which require tuning and calibration.

Chapter 2 presents the communication system at hand and the challenges when many channels are combined. A theoretical study about the consequences of the combining of multiple channels in the digital domain on the properties of the signal that is converted with the DAC is given, and the optimal level for amplitude clipping, in the case of a limited number of carriers and in the case of many carriers, is analyzed.

Chapter 3 introduces the DOCSIS broadcast system and the RF requirements that are specified in the standard. From this standard the requirements on a single transmitter that is capable to transmit multiple channels is derived.

Chapter 4 studies the traditional DAC/mixer combination and the requirements for the individual components that are needed and from these specifications the power consumption of such a transmitter is estimated and is used to compare against the proposed method. Using the traditional architecture the minimum power consumption is estimated to be about 1.2W per channel that

is being broadcasted.

In Chapter 5 the advantages of increasing the digitization and of advanced CMOS technologies are explained. The new approach of combining the carriers in the digital signal processing is analyzed and requirements for the digital signal processing functions are set. The number of carriers that can be transmitted using a single 'all-digital' transmitter increases significantly, compared to the traditional analog dual conversion transmitter, because the complexity of the analog core of the 'all-digital' transmitter is independent of the number of channels. The 'all-digital' transmitter can broadcast all channels that could be present in the full DOCSIS band with a single DAC. The main limitation in the number of channels is the limit in power dissipation that can be handled by the package, since adding more channels does only affect the digital signal processing and does not increase the complexity in the analog domain.

Chapter 6 proposes the implemented 'all-digital' transmitter architecture. Of this architecture the requirements for the building blocks are studied and the power consumption of these digital circuits is estimated.

In Chapter 7 the digital-to-analog converter used in this 'All-digital' transmitter is analyzed and several models are derived to estimate the performance of the DAC in case of imperfections. A new framework is given for modeling and analysis of current steering DAC performance in the case of broadband signals, and especially at high sample rates. For such broadband signals, error mechanisms that create distortion around the mid-scale transitions are more dominant in the performance of the system than error mechanisms that create distortion at the extremes of the amplitude range. Using fully binary DACs or DACs with a low segmentation results in a higher distortion level for signals that have wideband properties than for narrowband signals. When the DAC performance is affected by output conductance, a higher output conductance is allowed to achieve a similar performance for wideband signals than for a narrowband signal. Using these models an architecture for the DAC is selected and the measurement results of the realized DAC are shown.

In Chapter 8 the IC implementations are being discussed. The transmitter concepts have been used in a rationalized manner to design and implement

a 12-bit $2.8GS/s$ DAC in a 90nm CMOS process in combination with digital signal processing that upsamples, combines and upconverts the carriers. This serves as a vehicle IC to verify the validity of the 'all-digital' transmitter concepts proposed in this thesis. Based on this DAC, three different versions of a complete 'all-digital' transmitter, which consist of a combination of the digital signal processing and a DAC, were designed and implemented as ICs. The first two versions, the second being a redesigned version of the first one, use current mode logic for the digital signal processing, which is optimized to be able to run at the desired sample frequency of $2.8GS/s$. Since the digital signal processing is made in current mode logic and synchronous with the DAC clock, no interference is observed. The third version uses static CMOS logic in combination with several methods, such as the use of poly-clock phases, to reduce the interference from the digital signal processing to the sensitive analog circuits. It is shown that the combination of these techniques to reduce the interference is sufficient to achieve the required performance. The preferred logic style to implement the digital circuits is standard CMOS logic, which is efficient in terms of power consumption and of effort to implement the digital circuits. The proposed multi-carrier transmitter architecture is compared against the traditional multi-carrier transmitter. It is shown that the proposed multi-carrier DOCSIS transmitter can be more power and area efficient when multiple channels are being broadcasted than multiple traditional DOCSIS transmitters that have their outputs combined. In the case of 64 channels the expected reduction in the power consumption is more than 90%.

Samenvatting

Een traditionele zender die ontworpen is voor het verzenden van signalen over een televisiekabel, volgens de DOCSIS (Data Over Cable Service Interface Specification) standaard, bestaat uit meerdere digitaal-naar-analoog omzetters, welke gevolgd worden door analoge mixers. In deze traditionele zender wordt in ieder front-end n enkel kanaal geconverteerd van het digitale domein naar het analoge domein. Dit gebeurt met behulp van een digitaal-naar-analoog omzetter. Vervolgens wordt het analoge signaal naar de gewenste RF frequentie omgezet met behulp van een mixer.

Dit onderzoekswerk analyseert en realiseert een nieuwe manier om de traditionele analoge front-end in de zender te vervangen door digitale signaalverwerking. Hiemee wordt het ingangssignaal genterpoleerd, gecombineerd en gemoduleerd op de gewenste RF-frequentie. Vervolgens wordt met n enkele digitaal-naar-analoog omzetter het digitale RF signaal omgezet naar het analoge RF signaal, zonder dat er verdere analoge frequentie omzetting noodzakelijk is.

Deze nieuwe methode heeft als voordeel dat de complexiteit van de zender die meerdere kanalen kan verzenden verminderd is, omdat minder analoge componenten noodzakelijk zijn, voor welke afstemming en calibratie nodig zijn.

Een theoretische studie is uitgevoerd naar de consequenties van het combineren van meerdere kanalen in het digitale domein voor de eigenschappen van het signaal, dat met de digitaal-naar-analoog omzetter wordt geconverteerd. Naar aanleiding van deze veranderde eigenschappen, zijn eisen opgesteld voor de specificaties voor de digitaal-naar-analoog omzetter en de digitale signaalverwerking.

Bovendien bestudeert dit werk de traditionele zender die een analoog front-end bevat. De vereiste prestaties van de onderdelen die deze zender bevat worden afgeleid en daarmee wordt het minimale vermogen dat vereist is om deze functies uit te voeren vastgesteld. Ook de nieuwe manier van het verzenden van de kanalen wordt bestudeerd en de eisen voor de signaalverwerking worden

bepaald. Uit deze vereisten wordt het opgenomen vermogen afgeschat. Deze afschatting van het energieverbruik wordt gebruikt om de traditionele manier van het verzenden van de kanalen te vergelijken met de nieuwe methode. Uit deze vergelijking blijkt dat de voorgestelde methode minder vermogen nodig heeft dan de traditionele manier, wanneer meerdere kanalen verzonden worden.

Drie verschillende versies van een complete 'all-digital' zender bestaande uit een digitaal-naar-analoog omzetters in combinatie met de digitale signaalverwerking zijn ontworpen en gerealiseerd in een IC, welke geproduceerd is in 90nm CMOS technologie. Dit IC wordt gebruikt om het nieuwe concept te karakteriseren en te valideren. De eerste twee versies gebruiken logica die opgebouwd is volgens het 'current mode logic' principe voor de digitale signaalverwerking, welke geoptimaliseerd is om tot 2.8GS/s te kunnen werken. De laatste versie gebruikt standaard CMOS logica in combinatie met verschillende methoden, zoals meerdere clock fasen, om de impact van ongewenste koppeling van de digitale storing naar de gevoelige analoge componenten te minimaliseren.

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Biography

Pieter C.W. van Beek was born in 1978, in Waalwijk, The Netherlands. In 2000, he received his Bachelor degree with honours at the Hogeschool Rens & Rens, in Hilversum, The Netherlands. In 2003, he received the M.Sc. degree Cum Laude at the Faculty of Electrical Engineering at the Eindhoven University of Technology, The Netherlands. The graduation project was on the design of a high-speed, high-resolution current steering digital-to-analog converter. In 2003, he started as a PhD-student at the Eindhoven University of Technology on "Multi-Carrier single-DAC transmitter approach, applied to digital cable television". In 2007, he became a research scientist in the Mixed Signal Circuits and Systems group at NXP, Eindhoven, The Netherlands. Since 2010, he is working in the Product Line High Speed Converters Eindhoven as principal engineer. Since then, he has been working on high-speed, high-linearity digital-to-analog converters.