Multi-channel high-linearity time-to-digital converters in 20 nm and 28 nm FPGAs for LiDAR applications

Wujun Xie, Haochang Chen, Zhenya Zang, and David Day-Uei Li

***Abstract*—This paper proposes a new calibration method, the mixed-binning method, to pursue a TDC with high linearity in field-programmable gate arrays (FPGAs). This method can reduce the nonlinearity caused by large clock skews in FPGAs efficiently. Therefore, a wide dynamic range tapped delay line (TDL) TDC has been developed with maintained linearity. We evaluated this method in Xilinx 20nm UltraScale FPGAs and Xilinx 28nm Virtex-7 FPGAs. Results conduct that this method is perfectly suitable for driverless vehicle applications which require high linearity with an acceptable resolution. The proposed method also has great potentials for multi-channel applications, due to the low logic resource consumption. For a quick proof-of-concept demonstration, an 8-channel solution has also been implemented. It can be further extended to a 64-channel version soon.**

***Index Terms*—Carry chains, field-programmable gate array (FPGA), time-of-flight, time-to-digital converter (TDC), Automatic Vehicle.**

I. Introduction

A TIME-TO-DIGITAL converter (TDC) can convert a time interval into a digital number. High-precision TDCs have been widely used in time-resolved measurements in high energy physics, medical imaging, and other time-of-flight measurement applications.

TDCs can be implemented in both analog and digital methods. Recent advances in complementary metal-oxide-semiconductor (CMOS) manufacturing technologies have allowed digital TDCs to have an extremely high resolution in highly integrated systems [1]. Due to shorter development cycles and low cost, a field-programmable-gate-array (FPGA)-based TDC is also popular, compared with an application-specific integrated circuit (ASIC)-based TDC.

The tapped delay line (TDL) structure has been a mainstream approach for FPGA-based TDCs since carry-chain modules can easily construct TDLs in modern FPGAs. Other logic elements, such as look-up tables (LUTs) and digital signal processing (DSP) blocks, have also been used to build a TDL [2], [3]. The resolution of a TDL-TDC is related to the signal propagation delay in TDLs and is determined by CMOS manufacturing technologies. To overcome the process-related limitations and further improve the resolution, many methods, such as the Vernier delay line, the multi-phase design, and multi-chain structures, have been proposed.

There is a growing research trend in developing high-resolution TDCs for the increasing demand, for example, for clinical positron emission tomography (PET) [4]. However, for laser light detection and ranging (LiDAR) applications, especially in driverless vehicles, the linearity is the prioritized parameter. In driverless vehicles, the distance of objects can be from a few centimeters up to hundreds of meters. Hence, the typical TDC resolution is around 50-200 ps (corresponding to 1.50-6.00 cm) and the typical measurement range is around 100-200 m [5], [6]. However, to detect the location and movement of the objects, precise and accurate measurements are vital. Therefore, a high-linearity TDC is needed. The recently reported TDC for driverless vehicles achieves 50 ps resolution with DNL and INL (peak-to-peak) less than 1 LSB [7].

The non-uniformity of carry-chains and clock skews are the main reasons for nonlinearity. Uneven TDLs degrade the linearity and generate ultra-small bins and ultra-wide bins. Because of the clock distribution trees in FPGAs, large clock skews usually appear at the boundaries or in the middle of clock regions (CRs). To improve the linearity, many calibration methods, such as bin decimation and bin width calibration methods, were proposed [8], [9]. However, the nonlinearity caused by the large clock skews cannot be suppressed easily through these methods.

In this paper, we proposed a new calibration method, the mixed-binning method. This method can ignore the nonlinearity caused by the boundaries between clock regions in FPGAs. With this method, the proposed TDC can have DNL and INL (peak-to-peak) less than 0.1 LSB. This method is suitable for multi-channel applications. An 8-channel TDC with the mixed-binning method has been implemented in Virtex-7 and UltraScale FPGAs, respectively.

The remainder of this paper is structured as follows: Section II presents the proposed TDC architecture and the mixed-binning method. The experimental results and implementation details are included in Section III. Finally, in Section IV, the main conclusions are drawn, and some future research paths regarding the proposed TDC are explained.

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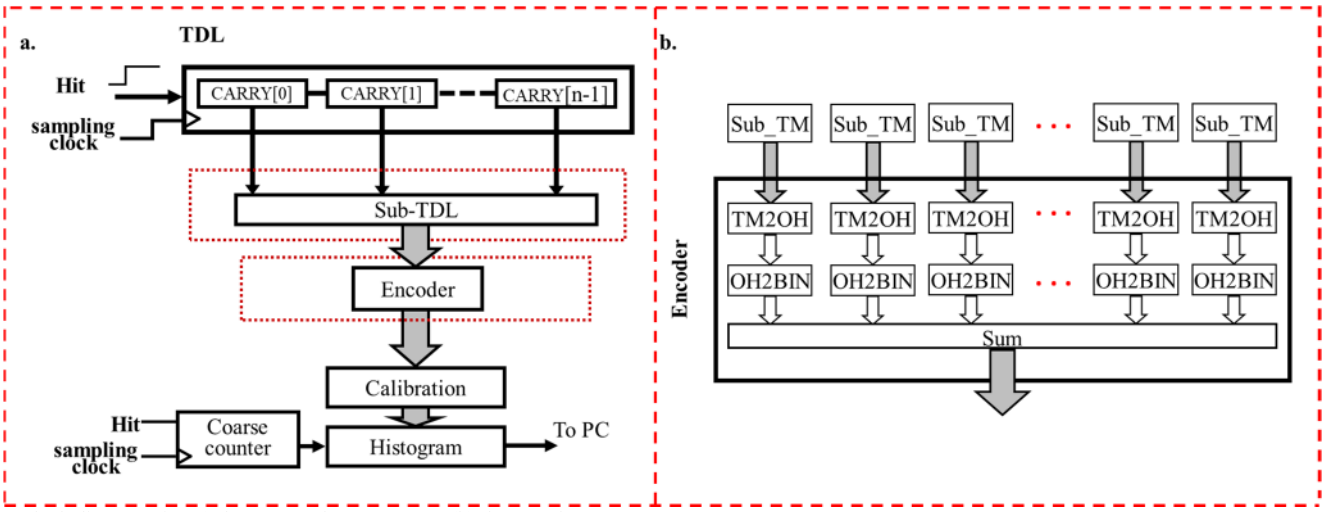

Fig. 1. Block diagrams for (a) the proposed TDC system, (b) the encoder.

II. Architecture and Design

A. Architecture

Figure 1(a) shows the architecture of the proposed TDC. TDLs were implemented with the cascaded carry-chain modules, CARRY4 in Virtex-7 and CARRY8 in UltraScale, respectively. The TDLs have been tuned in this study to minimize the nonlinearity [10]. The sub-TDL structure proposed by Chen and Li [8] can remove bubbles. With the sub-TDL structure, the raw thermometer code generated by a TDL is split into several subsets. These codes are transferred to corresponding one-hot codes (by TM2OH modules) and then encoded to binary codes (OH2BIN) in the encoder, see Fig. 1(b). The coarse counter is introduced to extend the measurement range of the TDC [11].

B. Mixed-Binning method

The mixed-binning method was inspired by the mixed calibration method and the bin decimation method in [8], [12], [13]. This method contains two parts: the binning method and mixed width calibration.

Similar to the bin decimation method, the main concept of the binning method is merging actual bins into a merged ideal bin, see Fig. 2. Small bins and ultra-wide bins are therefore ignored. In [14], it has been reported that the ultra-wide bins can be around 120-170 ps, because of the clock skews between some clock regions in Kintex-7 FPGAs. Chen *et al.* also examined the nonlinearity for a full-length TDL with 2000 bins in Virtex-7 FPGAs [13]. The test results show that the widths of the ultra-wide bins are less than 5.00 LSB (about 52.50 ps, LSB: 10.50 ps). Therefore, if the merged bins are wide enough, a long TDC can be constructed regardless of the large clock skews. To show the capability of ignoring large clock skews, in this study, a 400-tap TDL is implemented within two clock regions in Virtex-7 FPGAs. Moreover, for the LiDAR system in driverless vehicles, the required resolution is around 50-200 ps [5], [6]. Therefore, as a prototype, after merging, the LSB of the proposed TDCs are 10-fold larger in UltraScale FPGAs (LSB: from 5.02 ps to 50.92 ps) and Virtex-7 FPGAs (LSB: from 10.54 ps to 105.73 ps).

After binning, the linearity can be further improved by the bin width calibration. The bin width calibration performs bin-by-bin calibration on-chip and enhances the linearity.

Figure 3 shows the hardware implementation of the binning and mixed-binning method. Two block random-access memories (BRAMs) were used: the calibration BRAM and the histogram BRAM. Two factors, the bin correction factor (BCF) and the width calibration factor (WCF), are stored at the calibration BRAM. The BCF is the address of the merged ideal bin based on the binning method, and its value can be calculated based on the code density test on the plain TDC. WCF is the width calibration factor. For the binning method, the value of WCF is a fixed value. However, for the mixed-binning method, the results of code density tests can calculate the value of WCF after binning:

$$WCF[M] = \frac{1}{DNL\{BCF[M]\} + 1}, \qquad (1)$$

, where M is the bin number of the merged ideal bin.

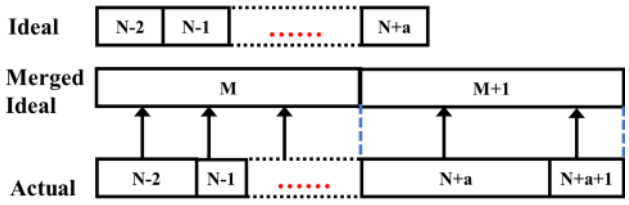

Fig. 2. The concept of the binning method.

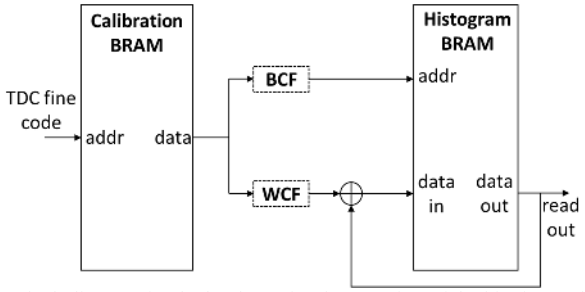

Fig. 3. Block diagram for the hardware implementation of the binning and mixed-binning method.

Table I
Linearity Performance of the proposed TDCs

		Origin	Binning	**Mixed-Binning**
UltraScale 20 nm	LSB (ps)	5.02	**50.92**	
	DNL (LSB)	[-0.97, 2.94]	[-0.23, 0.24]	**[-0.03, 0.06]**
	DNL_{pk-pk} (LSB)	3.90	0.47	**0.09**
	σ_{DNL} (LSB)	0.75	0.11	**0.02**
	INL (LSB)	[-2.33, 6.21]	[0.07, 0.24]	**[-0.02, 0.09]**
	INL_{pk-pk} (LSB)	8.55	0.31	**0.11**
	σ_{INL} (LSB)	1.70	0.07	**0.03**
Virtex-7 28 nm	LSB (ps)	10.54	**105.73**	
	DNL (LSB)	[-0.95, 1.89]	[-0.18, 0.18]	**[-0.02, 0.02]**
	DNL_{pk-pk} (LSB)	2.84	0.36	**0.04**
	σ_{DNL} (LSB)	0.54	0.08	**0.01**
	INL (LSB)	[-2.25, 2.40]	[-0.13, 0.10]	**[-0.06, 0.03]**
	INL_{pk-pk} (LSB)	4.65	0.23	**0.09**
	σ_{INL} (LSB)	0.89	0.05	**0.02**

III. Experimental Results and Implementation

A. Experimental Results

The proposed TDCs have been implemented in UltraScale FPGAs and Virtex-7 FPGAs, respectively. To evaluate the linearity, we performed code density tests. For the long-range precision, a laser single-shot precision test with a single-photon avalanche diode (SPAD) array will be performed in the continuing work.

Table I summarizes the linearity performance of the proposed TDCs in UltraScale and Virtex-7. With the binning method, the linearity is improved significantly. The values of DNL_{pk-pk} are 0.47 LSB and 0.36 LSB in UltraScale and Virtex-7 FPGAs, and the resolutions are 50.92 ps and 105.73 ps, respectively. With the mixed-binning method, the linearity can be further enhanced, and the bins are more even; the values of σ_{DNL} are 0.02 LSB and 0.01 LSB in UltraScale and Vitex-7 FPGAs, respectively. In this paper, the TDC with the binning method is named as the binned TDC and the TDC with the mixed-binning method the hybrid TDC, hereafter, for simplicity.

Figure 4 shows the nonlinearity curves for the plain TDCs in UltraScale and Virtex-7 FPGAs. In Fig. 4(a), the wider bins around 230 cause a distinct step in the INL curve. Similar phenomena appear in Fig. 4(b), see bin 100 and bin 300. Large clock skews contribute significant nonlinearity for these plain TDCs due to the bifurcation of the clock distribution tree in the middle of a clock region.

However, with the binning method, the nonlinearity caused by the large clock skews can be significantly suppressed. Figure 5 shows the linearity performances of the proposed TDCs. The binned TDCs achieve 0.31 LSB INL_{pk-pk} in UltraScale FPGAs and 0.23 LSB INL_{pk-pk} in Virtex-7 FPGAs. The hybrid TDCs achieve 0.11 LSB INL_{pk-pk} and 0.09 LSB INL_{pk-pk} in UltraScale and Virtex-7 FPGAs, respectively.

Figure 6 shows the bin width distributions between the binned TDCs and the hybrid TDCs. From Fig. 6, the hybrid TDCs have a more concentrated bin distribution, both in UltraScale and Virtex-7 FPGAs. It also supports the statement that the width calibration method can further enhance the linearity.

B. Implementation

The implementation layouts of the proposed 8-channel TDCs in UltraScale and Virtex-7 FPGAs are shown in Fig. 7. To ease the large nonlinearity contributed by the clock tree distributions, the TDLs are placed in central clock regions for Virtex-7 FPGAs and are constrained within a clock region for UltraScale digital resources, the proposed TDC design has great potential for multi-channel applications. The prototype only contains 8 channels for a quick proof-of-concept study. It can be easily extended to a 64-channel version.

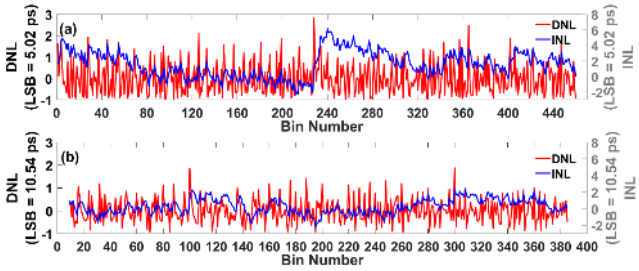

Fig. 4. Nonlinearity curves for the plain TDCs in (a) UltraScale and (b) Virtex-7 FPGAs.

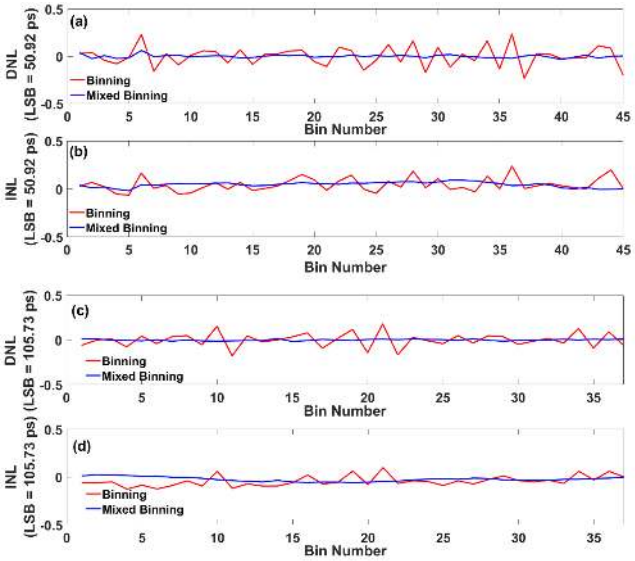

Fig. 5. Nonlinearity curves for the proposed TDCs with the binning method and the mixed-binning method. (a) and (b) for the UltraScale FPGAs. (c) and (d) for the Virtex-7 FPGAs.

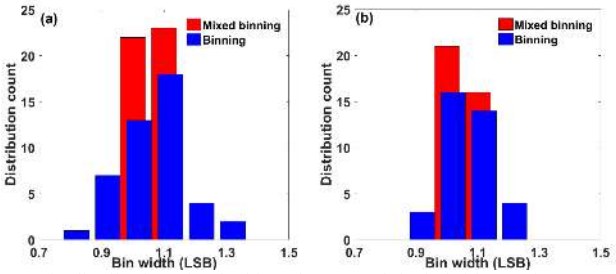

Fig. 6. Bin distributions for the binned TDC and the hybrid TDC in (a) UltraScale and (b) Virtex-7 FPGAs.

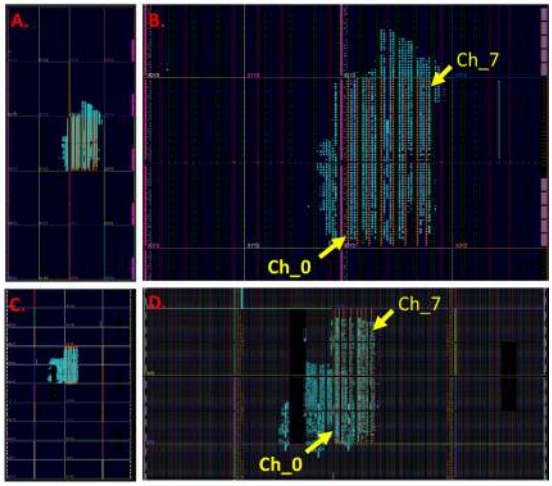

Fig. 7. Layouts of 8-channel hybrid TDC. a) Overview and b) center clock regions in UltraScale FPGAs. c) Overview and d) center clock regions in Virtex-7 FPGAs.

Table II
Consumption of Logic Resources

			Single channel	8 channels
	Resource	Total	Used	Used
UltraScale 20 nm	CARRY	30300	80 (0.26%)	639 (2.11%)
	LUTs	242400	703 (0.29%)	5170 (2.13%)
	FFs	484800	1195 (0.24%)	9537 (1.97%)
	BRAM	600	1.5 (0.25%)	13.5 (2.25%)
	Slice	30300	356 (1.17%)	1672 (5.52%)
Virtex-7 28nm	CARRY	108300	100 (0.09%)	857 (0.79%)
	LUTs	433200	822 (0.19%)	4580 (1.06%)
	FFs	866400	1219 (0.14%)	8108 (0.94%)
	BRAM	1470	2 (0.14%)	16 (1.09%)
	Slice	108300	986 (0.91%)	3028 (2.79%)

IV. Conclusion

In this paper, we propose a new calibration method, the mixed-binning method. The proposed solution achieves excellent linearity, $DNL_{pk-pk} = 0.09$ LSB and $INL_{pk-pk} = 0.11$ LSB with 50.92 ps resolution in UltraScale FPGAs, and $DNL_{pk-pk} = 0.04$ LSB and $INL_{pk-pk} = 0.09$ LSB with 105.73 ps resolution in Virtex-7 FPGAs. Furthermore, the measurement range can be easily extended using coarse counters. The proposed method is suitable for LiDAR applications, especially for driverless vehicles which require high-linearity and a typical measurement range (around 128 m or, equivalently, 853 ns) [5], [6].

Moreover, the proposed method is suitable for multi-channel applications. The 8-channel designs have been implemented in UltraScale and Virtex-7 FPGAs. This method does not need to use a lot of logic resources; it has great potential for multi-channel applications.

In the near future, we will integrate the proposed TDC with a SPAD array; the long-range single-shot precision test will be implemented, and a LiDAR system will be built based on the proposed multi-channel TDCs.

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