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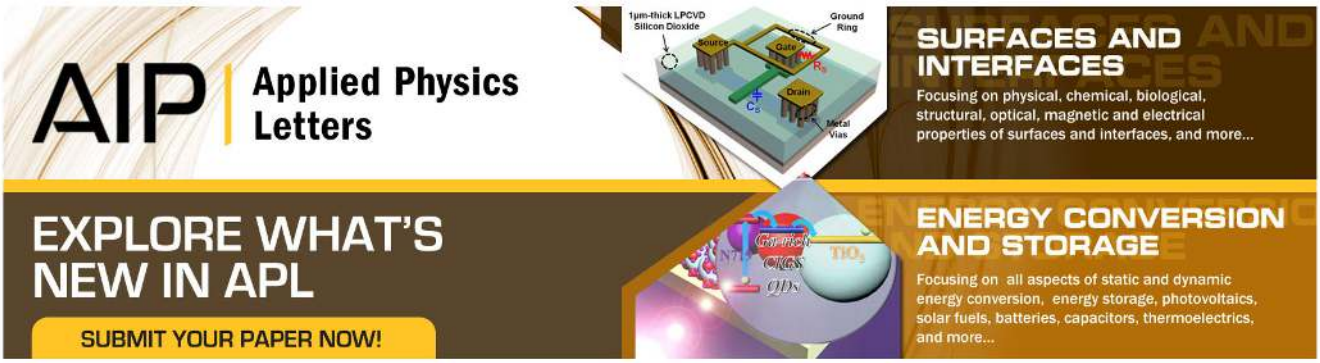

Multi-finger flexible graphene field effect transistors with high bendability

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Highly bendable graphene field-effect transistors are fabricated on polyimide films. The device offers robust performance against various conditions including immersion in liquids, and dynamic loading tests, which are hazardous to conventional electronics. Bendability of the sample is tested with the bending radius of down to 1.3 mm; the devices remain fully functional with less than 8.7% reduction and no reduction in the electron and hole mobility after repeated bending tests, respectively. Multi-finger electrodes are implemented on flexible substrates to enhance its current drive. Silicon-nitride passivation offers efficient chemical protection over diverse liquids and robust mechanical protection against impacts. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4772541]

Smart mobile electronic systems in the future will be fully integrated on to seamless monolithic substrates and will have a variety of attributes that transcend existing electronics, ushering in a new era of unprecedented system performance and functionality. The desired attributes of such a system include mechanical flexibility, resilience to liquid spills, and physical drops and mechanical shocks that are typically hazardous to current monolithic electronic systems. While much progress has been achieved in demonstrating mechanically flexible organic and inorganic electronics,[1–4] substantial research remains for realizing nanoelectronics that are immune to everyday hazardous conditions. Flexible monolithic nanoelectronics immune to harsh conditions are expected to have a substantial societal benefit beyond system functionality, concerning cost, electronic waste, environmental impact, weight, and portability.

In this letter, we report the development of rugged multi-finger embedded-gate graphene field-effect transistors (MEGFETs) on flexible polyimide (PI) sheets. These devices exhibit robust electrical performance after mechanical bending and exposure to harsh conditions including submersion in several liquids (water, tea, coffee, and milk), and high dynamic loading to mimic very extreme conditions that probe the mechanical resilience of the flexible GFETs. These GFETs combine state-of-the-art device features required for high-performance, such as sub-micron channel length for high-speed transport, high-k dielectric for improved gate control, embedded gate for improved gate dielectric scaling,[4,5] multi-finger gates for high drive current, and silicon nitride passivation for protection from the environment. While the rugged flexible devices have been achieved based on monolayer graphene, suitable for analog transistors,[5–7] similar results should be achievable for graphene nanoribbons and carbon nanotubes for digital transistors,[8,9] thereby, affording a route for carbon-based smart and rugged electronic systems.

Industrial PI sheet (100 μm thick) was chosen as the substrate because of its high glass transition temperature (>300 °C), Young's modulus (~3.5 GPa), and high solvent resistance. PI has an uneven topography with surface roughness exceeding 100 nm. To make the surface smooth, liquid polyimide (PI2574 from HD Microsystems) was spin-coated (~15 μm thick) onto the PI sheet to obtain a smooth surface (RMS ~1–2 nm),[10] which is necessary for preserving material quality and for achieving the best lithographic resolution and registration. The PI coating was cured at 200 °C and 300 °C for 30 min and 60 min, respectively, under nitrogen flow at atmospheric pressure.

The 3-D image of the fabricated 10-finger MEGFET unit-cell is illustrated in Fig. 1(a). In brief, an array of gate electrodes were patterned directly on PI by electron-beam lithography (EBL), evaporation, and lift-off. A high-k

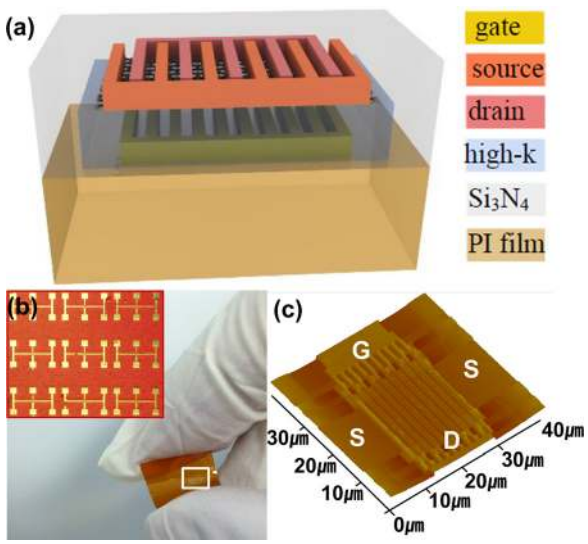

FIG. 1. Multi-finger EGFET fabricated on plastic substrates. (a) 3-D image of the complete device of a 10-finger unit cell. (b) Optical image of the sample. The device area is highlighted by a white rectangle. Inset shows an array of the unit cells with gate (G), source (S), and drain (D) pads. (c) AFM image of the active channel area revealing a device with 10-fingers.

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dielectric of 15-nm thick Al_2O_3 was deposited by atomic layer deposition (ALD) with estimated gate-oxide capacitance of 405 nF/cm^2. Another EBL followed by wet-etching of Al_2O_3 by a 1:3 diluted solution of H_3PO_4:DI water isolated each device while leaving local dielectric islands for the channel. High quality monolayer graphene film grown by chemical vapor deposition (CVD) was then transferred via the conventional poly(methyl methacrylate) (PMMA) wet-transfer process using ammonia persulfate to etch the supporting copper foil.[11,12] The active channel area of graphene was then patterned, and source and drain electrodes were defined to complete the device structure. After completing initial electrical measurements, the top of the sample was then covered with a 30-nm thick plasma-enhanced chemical vapor deposited (PECVD) Si_3N_4 layer to protect the MEGFETs from the outside environment.

The highly uniform graphene monolayer enabled the fabrication of large area devices with multi-finger configurations for the electrodes. The channel length and width for each finger were fixed at 0.5 μm and 20 μm, respectively. Devices with both 10-finger and 18-finger configurations were prepared resulting in effective channel widths of 200 μm and 360 μm, respectively, on the same PI substrate. The optical image given in Fig. 1(b) shows the freestanding PI with an array of flexible MEGFETs bent with fingers. The inset shows a 3 × 3 array of the unit cells. Fig. 1(c) is a high-resolution image of the active channel area obtained with an atomic force microscope (AFM) revealing a 10-finger electrode configuration.

Electrostatic device properties of the MEGFETs evaluated under ambient conditions are presented in Fig. 2. The room-temperature measurements show good agreement with a widely used low-field graphene transistor model which takes into account non-idealities such as contact resistance (R_C) and charged impurities as shown in Fig. 2(a).[13] Fig. 2(a) shows the gate modulation over the total resistance including contributions from the graphene channel and contacts. Figs. 2(b)–2(d) represent the statistical histograms of device parameters measured from all implemented devices.

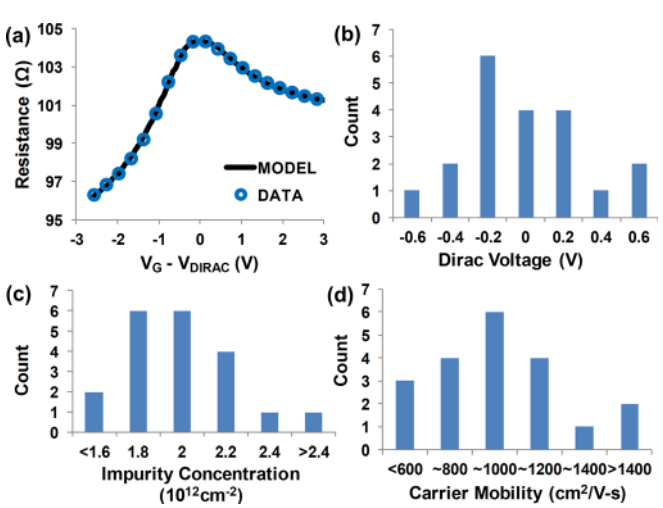

FIG. 2. Experimental electrical characteristics of MEGFETs. (a) Gate modulation of the total resistance including contact resistance from a device. (b), (c), and (d) Histograms of the Dirac voltages, residual carrier concentrations, and peak carrier mobilities from all measured devices, respectively.

Fig. 2(b) represents measured Dirac voltages. Fig. 2(c) shows residual charged impurity concentrations and (d) shows extracted carrier mobilities, respectively. The peak mobility measured here (over 1400 cm^2/Vs) has previously been shown to afford ~100 GHz transit frequency.[14] The mobility in these devices is limited by impurity scattering and grain boundaries based on temperature dependent studies of a similar device process that indicated negligible phonon scattering.[4] Further improvements in mobility can be achieved with larger graphene domains and improved transfer methods.[15] The highly uniform graphene, with negligible un-intentional doping and smoothened PI surface, afforded an array of MEGFETs with the Dirac voltage close to a gate voltage (V_G) of 0 V as shown in Fig. 2(b), which we suggest is an important achievement for uniform graphene transistor arrays for large-area flexible nanoelectronics.

Bending measurements on a custom mechanical fixture with sub-millimeter dimensional precision (Fig. 3(a)) revealed robust graphene transistor performance down to a bending radius of ~1.3 mm,[16] The 1.3 mm radius corresponds to a bending strain of ~4.6%.[17] The Dirac voltage remained within ±0.2 V of the nominal values as shown in Fig. 3(b); the infinity symbol(∞) in Fig. 3 indicates the value obtained under flat conditions. Carrier mobilities in some cases showed modest improvements (Figs. 3(c) and 3(d)), indicating that strain engineering might be an attractive route for appreciable mobility enhancement on flexible substrates for devices limited by impurity or grain boundary scattering. Contact resistances were relatively robust against bending with an average change of ~15% down to 1.3 mm bending

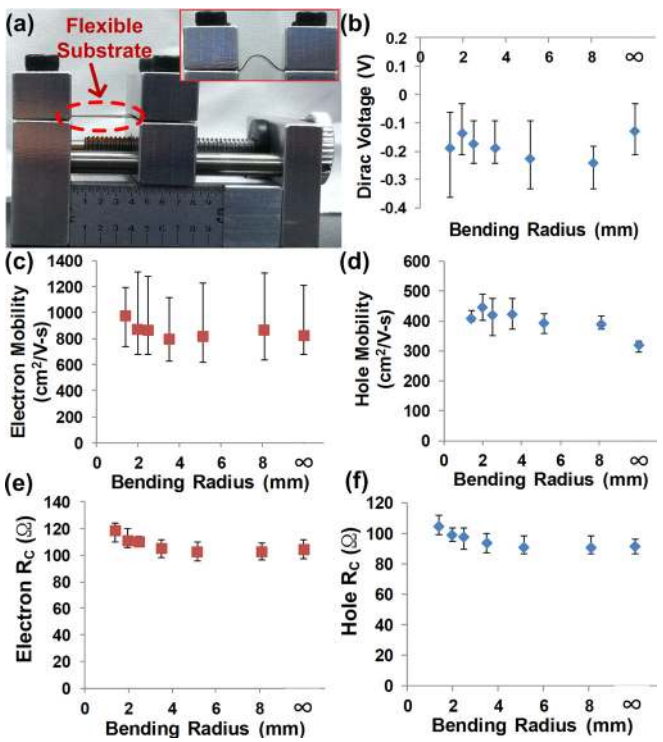

FIG. 3. The dependence on device properties on mechanical bending of the substrate. (a) Mechanical fixture for bending measurements. The flexible substrate is highlighted by a red circle. Inset shows the flexible substrate under bending. (b) The dependence of the Dirac voltage on the bending radius. (c) and (d) Effects of bending on carrier mobilities. (e) and (f) Effects of bending on the contact resistances.

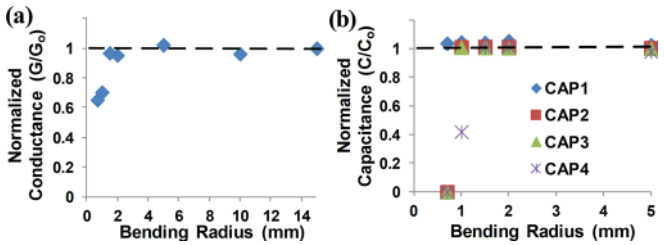

FIG. 4. Mechanical bending experiments for metal interconnects and MIM capacitors on PI films. (a) The change in conductance of metal lines. (b) The change in normalized capacitances of MIM capacitors. CAP1, CAP2, CAP3, and CAP4 are $10 \times 10\,\mu m^2$, $50 \times 50\,\mu m^2$, $100 \times 100\,\mu m^2$, and 200x200 μm^2, respectively. The dashed line is a visual guide indicating invariant properties over a wide bending radius.

radius as seen in Figs. 3(e) and 3(f). We note that the substrate bending was parallel to the transport (channel length) direction, which has been observed to be the critical direction most impacted by mechanical strain.[17]

In order to understand the failure mechanisms during mechanical bending, test structures with metal interconnects and metal-oxide-metal (MIM) capacitors were prepared and experimentally evaluated as given in Fig. 4. Fig. 4(a) shows the change in normalized conductance from metal interconnects corresponding to the bending radius down to 0.7 mm; G stands for the conductance at the specific bending radius while G_o represents the original value under the flat condition. Fig. 4(b) presents the similar test results for capacitors; $10 \times 10\,\mu m^2$, $50 \times 50\,\mu m^2$, $100 \times 100\,\mu m^2$, and $200 \times 200\,\mu m^2$ unit devices were patterned on PI substrates; 30-nm thick ALD Al_2O_3 was deposited as dielectrics. The metal interconnects show lower conductances (40% reduction) at smaller bending radius owing to mechanical deformation and elongation making locally thinner lines with higher resistance. While supported on polymeric substrates, metal electrodes are uniformly stretched so as to approach their maximum allowable strain without degradation of over 4%,[18] which corresponds to the bending radius of ~1.5 mm. Beyond this point, metal films show increasing resistance while still maintaining functionality, indicating good adhesion at the PI interface without de-bonding of metal films from the substrate.[18] In Fig. 4(b), MIM capacitors are evaluated. Here, C and C_o are the capacitance at the specific bending radius and the original capacitance under the flat condition, respectively. The largest unit cell (CAP4 with $200\,\mu m \times 200\,\mu m$ dimension) shows dramatic reduction in its value at the radius of 1 mm and total failure at smaller radius. CAP2 ($50\,\mu m \times 50\,\mu m$) and CAP3($100\,\mu m \times 100\,\mu m$) cells failed at the minimum bending radius of 0.7 mm. The smallest unit cell (CAP1) did not lose functionality even at the smallest bending radius. These results supports the idea that by predefining local dielectric islands where the active channel is located, the bendability of the flexible devices can be further improved and maximized with perhaps a small degradation of the electrical properties owing to increased electrode resistances.

The graphene transistors were evaluated in a variety of harsh conditions (Fig. 5), that can be hazardous for conventional monolithic electronics. At the outset, the sample was fully immersed sequentially in liquids in the following order: water, green tea, warm coffee, and thick milk for ~3 s each to emulate unexpected everyday conditions that can occur suddenly for a short time. At each interval, the sample was dried with a compressed air duster and the current-voltage response measured before the next immersion. Afterwards, the sample was exposed to mechanical stresses such as a walking test at ~4 ft/s, and automobile driving test at ~5 mile/h. The human and automobile weigh approximately 115 lbs and 3300 lbs, respectively. As seen in Fig. 5, the MEGFETs retain their electrical functionality under these harsh conditions. In the graphene device selected for

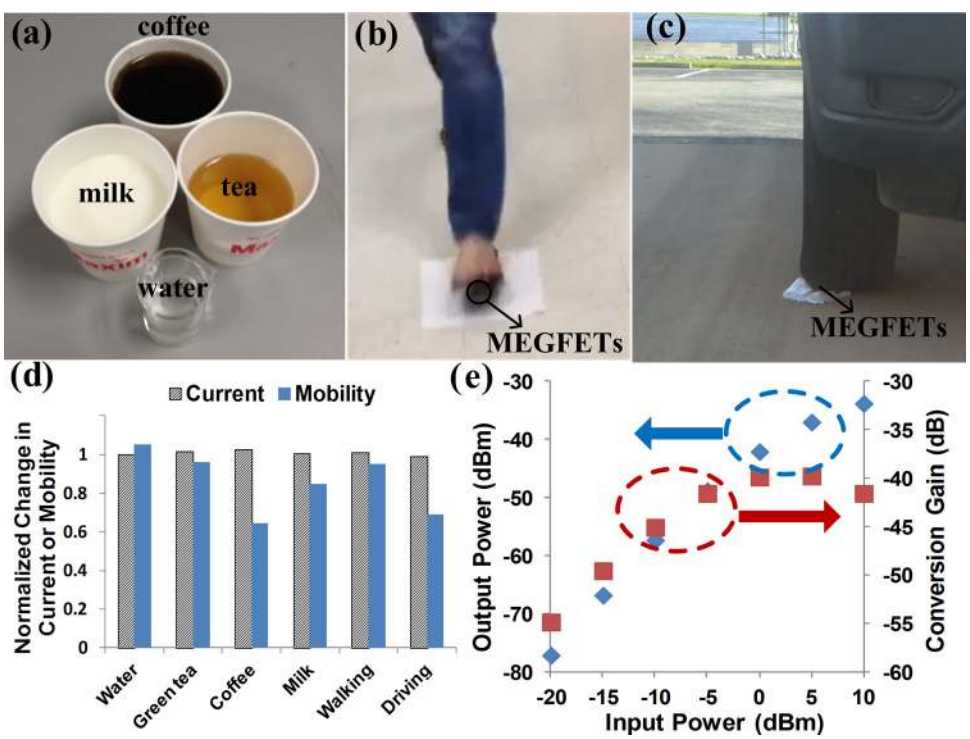

FIG. 5. Experiments involving harsh conditions. (a) Photographs of the different liquids used during the test. (b) Still image of the devices been walked over to emulate a slow-moving load. (c) Still image of 2002 Honda CRV sport-utility vehicle going over the devices. The real time video for (b) and (c) is available online. (d) The normalized change in current and mobility after the different harsh conditions. (e) Doubler characteristics. The output power at the doubled frequency (2f) and the conversion gain as a function of the input power at the fundamental frequency (1f = 2 MHz) are given. The gate is biased at the Dirac point and $V_D = 300$ mV (enhanced online) [URL: http://dx.doi.org/10.1063/1.4772541.1].

monitoring, the degradation in current was less than 4%. The mobility dropped by as much as ~40% after immersion in warm coffee, but recovered to 90% of the initial mobility after the walking test, indicating that the impact of the warm fluid is at least partially reversible likely owing to thermal relaxation and fluid desorption. These electrical results suggest that nitride passivated GFETs on PI provide a route for realizing high-performance rugged nanoelectronic systems. More systematic precision uniaxial compressive loading and impact testing are required for further electro-mechanical understanding. By comparison, a silicon chip from a commercial 45 nm-node technology featuring transistors with PI/Si_3N_4 topside passivation,[19] was not robust against immersion with more than 60% drop in the on-current and no current after immersion in water and coffee respectively for the same duration. Fig. 5(e) shows the frequency doubler performance of the device evaluated after completing immersion tests and dynamic loading tests. The frequency doubler evaluated in this work showed high-spectral purity (>90%) while affording a peak conversion loss of ~39.7 dB, which is within 5 dB of our earlier report achieved with graphene transistors on a smooth single-crystal quartz substrate.[7] These results motivate further developments of graphene-based analog and RF circuits on flexible sheets.

In conclusion, graphene transistors with state-of-the-art device features such as embedded gates, high-k dielectrics, sub-micron channel length, multi-fingers with up to 18-fingers, and Si_3N_4 passivation have been realized on flexible substrates. The transistors are robust against a variety of harsh conditions that are hazardous for conventional electronics, including immersion in liquids, mechanical deformation, and loads from moving person and objects. This work enables a route for high-performance flexible carbon nanoelectronics that offer resilient performance that transcend contemporary monolithic electronics.

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[1]Q. Cao, H.-S. Kim, N. Pimparkar, J. P. Kulkarni, C. Wang, M. Shim, K. Roy, M. A. Alam, and J. A. Rogers, Nature **454**, 495 (2008).
[2]C. Yoon, G. Cho, and S. Kim, IEEE Trans. Electron Devices **58**(4), 1096 (2011).
[3]O. M. Nayfeh, IEEE Electron Device Lett. **32**(10), 1349 (2011).
[4]J. Lee, L. Tao, Y. Hao, R. S. Ruoff, and D. Akinwande, Appl. Phys. Lett. **100**, 152104 (2012).
[5]S.-J. Han, K. A. Jenkins, A. V. Garcia, A. D. Franklin, A. A. Bol, and W. Haensch, Nano Lett. **11**(9), 3690 (2011).
[6]F. Schwierz, Nat. Nanotechnol. **5**, 487 (2010).
[7]M. E. Ramon, K. N. Parrish, J. Lee, C. W. Magnuson, L. Tao, R. S. Ruoff, S. K. Banerjee, and D. Akinwande, in *2012 IEEE MTT-S International Microwave Symposium Digest (MTT)*, Montreal, Canada, June 17–22 (2012), p. 1–3.
[8]D. Akinwande, J. Liang, S. Chong, Y. Nishi, and H.-S. P. Wong, J. Appl. Phys. **104**, 124514 (2008).
[9]X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, Science **319**(5867), 1229 (2008).
[10]L. Tao, J. Lee, and D. Akinwande, J. Vac. Sci. Technol. B **29**(6), 06FG07 (2011).
[11]X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo, and R. S. Ruoff, Science **324**(5932), 1312 (2009).
[12]L. Tao, J. Lee, H. Chou, M. Holt, R. S.Ruoff, and D. Akinwande, ACS Nano **6**(3), 2319 (2012).
[13]S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. K. Banerjee, Appl. Phys. Lett. **94**(6), 062107 (2009).
[14]Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, Science **327**(5966), 662 (2010).
[15]A. Pirkle, J. Chan, A. Venugopal, D. Hinojos, C. W. Magnuson, S. McDonnell, L. Colombo, E. M. Vogel, R. S. Ruoff, and R. M. Wallace, Appl. Phys. Lett. **99**(12), 122108 (2011).
[16]J. Lee, L. Tao, K. N. Parrish, Y. Hao, R. S. Ruoff, and D. Akinwande, in IEEE 12th International Conference on Nanotechnology (IEEE-NANO), Birmingham, United Kingdom, 20-23 August 2012.
[17]K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y.Choi, and B. H. Hong, Nature **457**, 706 (2009).
[18]T. Li, Z. Huang, Z. Suo, S. P. Lacour, and S. Wagner, Appl. Phys. Lett. **85**(16), 3435 (2004).
[19]S. Lee, B. Jagannathan, S. Narasimha, A. Chou, N. Zamdmer, J. Johnson, R. Williams, L. Wagner, J. Kim, J.-O. Plouchart, J. Pekarik, S. Springer, and G. Freeman, Tech. Dig. - Int. Electron Devices Meet. 2007, 255–258.