Multi-Input DC/DC Converter Based on the Multiwinding Transformer for Renewable Energy Applications

Yaow-Ming Chen, *Member, IEEE*, Yuan-Chuan Liu, and Feng-Yu Wu

***Abstract*—A multi-input dc/dc converter based on the flux additivity is proposed in this paper. Instead of combining input dc sources in the electric form, the proposed converter combines input dc sources in magnetic form by adding up the produced magnetic flux together in the magnetic core of the coupled transformer. With the phase-shifted pulsewidth-modulation (PWM) control, the proposed converter can draw power from two different dc sources and deliver it to the load individually and simultaneously. The operation principle of the proposed converter has been analyzed in detail. The output voltage regulation and power flow control can be achieved by the phase-shifted PWM control. A prototype converter with two different dc voltage sources has been successfully implemented. Computer simulations and hardware experimental results are presented to verify the performance of the proposed multi-input dc/dc converter.**

***Index Terms*—Flux additivity, multi-input dc/dc converter, phase-shifted pulsewidth-modulation control.**

I. Introduction

APPLICATIONS with renewable energy such as the solar cell array, wind turbines, or fuel cells have increased significantly during the past decade. Different circuit topologies for multi-input dc/dc converters have been proposed to combine different types of clean energy to obtain the regulated dc output voltage. Different dc sources can be put in series to implement the multi-input dc/dc converter and the regulated output voltage can be achieved [1], [2]. However, if one of the dc sources is diminished, it will be very difficult to obtain the regulated voltage output since the input voltage variation is significant. Another approach is to put dc sources in parallel by using the coupled transformer [3], [4]. Control schemes for those multi-input dc/dc converter with paralleled dc sources are based on the time-sharing concept because of the clamped voltage on the winding of the coupled transformer. Hence, only one of these dc sources is allowed to transfer energy to the load at a time. Since energy can be transferred or combined in different varieties of forms, it is possible to combine input dc sources in the magnetic form rather than the electric form.

Paper IPCSD 02–018, presented at the 2001 Industry Applications Society Annual Meeting, Chicago, IL, September 30–October 5, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. Manuscript submitted for review October 15, 2001 and released for publication May 9, 2002.

The authors are with the Power Electronics Applied Research Laboratory (PEARL), Department of Electrical Engineering, National Chung Cheng University, Chia-Yi, Taiwan, R.O.C. (e-mail: ieeymc@ccu.edu.tw).

Publisher Item Identifier 10.1109/TIA.2002.800776.

Transformers in different varieties of converters are used to deliver the electric power from the primary side to the secondary side to meet the desired voltage and current requirements as well as to provide the electric isolation for the application. According to Ampere's law, currents in the primary winding will produce magnetic flux in the magnetic core which will induce voltages in the secondary winding based on Faraday's law. The induced voltage on the fixed-turn-number secondary winding is determined by the total flux linkage produced by different magnetomotive force (MMF) sources, which are created by currents in different windings. Consequently, the magnetic flux linkage provides a possible approach to combine energy from different sources.

The objective of this paper is to propose an innovative multi-input dc/dc converter, which is based on the concept of the transformer flux additivity. A two-input current-fed full-bridge dc/dc converter with phase-shifted pulsewidth-modulation (PWM) control [5], [6] is proposed in this paper to realize the proposed idea. The proposed circuit topology has the following advantages: 1) magnitudes of dc input voltages can be different; 2) dc sources can deliver power individually and simultaneously; 3) the soft-switching technology is accessible; and 4) the electric isolation is naturally achieved. Computer simulations and hardware experimental results are presented in this paper to confirm the performance of the proposed innovative multi-input dc/dc converter.

II. Operation Principle of the Proposed Converter

The schematic diagram of the proposed two-input current-fed full-bridge dc/dc converter is shown in Fig. 1. It consists of two current-source input-stage circuits, a three-winding coupled transformer, and a common output-stage circuit. The number of the input-stage circuits can be increased to meet the practical multi-input dc sources requirement while the coupled transformer and the output-stage circuit remain unchanged. In order to produce the desired magnetic flux in the coupled magnetic core, the current source input-stage circuit is implemented by the current-fed full-bridge dc/ac converter. Each dc voltage source associated with a choke inductor becomes a dc current source, which implies that the amplitude of the dc voltage source can be different. This is a very important feature for the multi-input dc/dc converter since voltage variations of these dc sources could be significant. Each switch of the current-fed full-bridge dc/ac converter in the input-stage circuit should be

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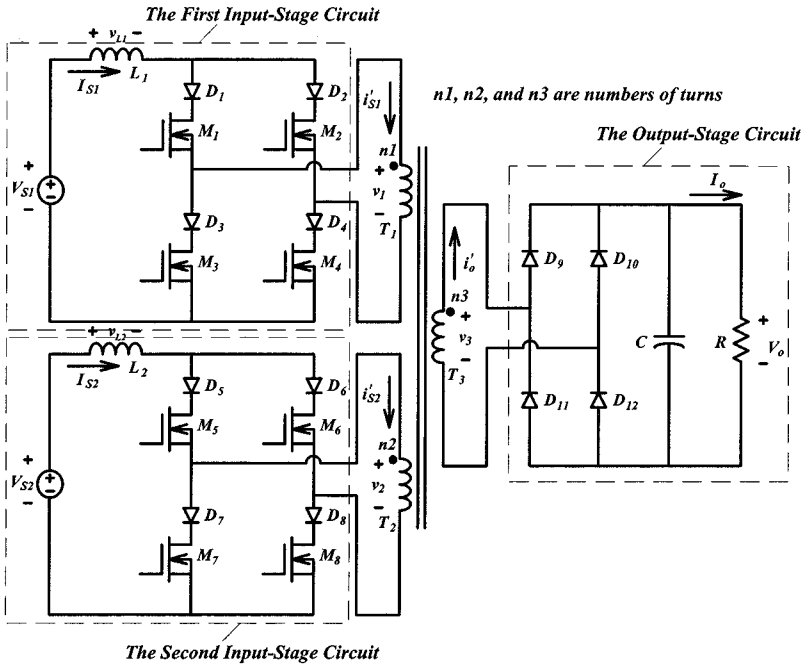


Fig. 1. Circuit topology of the proposed two-input current-fed full-bridge dc/dc converter.

in series with a reverse-blocking diode. The reverse-blocking diode can regulate the direction of the current flow and prevent the reverse power flow from other dc sources via the coupled transformer and switches' body diodes. Without these reverse-blocking diodes, different dc sources of the proposed multi-input dc/dc converter cannot deliver power to the load simultaneously. Also, all input-stage windings and the output-stage winding of the coupled transformer should be wound on the same magnetic core to ensure that the total flux linkage produced by each input current source can entirely pass through the output-stage winding. The output-stage circuit is implemented by an ac/dc full-bridge rectifier with appropriate output filters.

When two MOSFETs located at the diagonal position of the full-bridge converter in each input-stage circuit are turned on, power is transferred from the current source of the input-stage circuit to the output-stage circuit through the transformer. This is called the power transferring stage. On the other hand, when two MOSFETs of the right leg or left leg of the full-bridge converter in each input-stage circuit are turned on, the input current source is freewheeling through these turned-on MOSFETs and no power is transferred to the output-stage circuit. This is referred to as the freewheeling stage. Demanded power transferring from the input-stage circuit to the output-stage circuit can be achieved by controlling the time ratio of the power transferring stage to the freewheeling stage.

If the first input-stage circuit is in the power transferring stage and the second input-stage circuit is in the freewheeling stage, the induced voltages on each winding of the coupled transformer will be clamped to the value that is proportional to the output voltage. The clamped winding voltage intends to deliver power to the second input-stage circuit, which is in the freewheeling stage. Since all MOSFETs are in series with reverse-blocking diodes, the second input-stage circuit will still stay in the freewheeling stage. Thus, there is no power transferring between the two input-stage circuits, even when they are all in the power transferring stage. Therefore, power can be delivered from two input-stage circuits to the common output-stage circuit individually and simultaneously without disturbing each other.

The conventional PWM control scheme cannot be directly applied to the proposed multi-input dc/dc converter because of the transformer winding voltage-clamping problem. For the current-fed full-bridge dc/ac converter with the conventional PWM control scheme, switches in the diagonal position form a simultaneous conduction switch pair to transfer power to the load. Two switch pairs of the current-fed full-bridge dc/ac converter should be all conducted in order to avoid an abrupt current change in the input choke inductor while alternating the conducting switch pair. This overlapping conduction time will cause all transformer winding voltages to be clamped to zero since the induced voltage on each winding of the transformer should follow the turn ratio relationship between windings. The appearance of the unexpected and unwanted clamped voltage will disable the normal operation of the other dc input-stage circuit. The solution to this voltage-clamping problem is to use a phase-shifted PWM control scheme.

A phase-shifted PWM control scheme for current-fed full-bridge dc/dc converter is used in this paper. The phase-shifted PWM controller IC UC3879 with auxiliary circuits is used to generate gate signals for MOSFETs in the proposed converter. Also, the functions of soft start and overcurrent protection, which are very important issues for the boost-derived full-bridge converter, are accessible via pin 6 and pin 4 of IC UC3879. A typical phase-shifted PWM control pattern for the proposed multi-input dc/dc converter is shown in Fig. 2. During the transient of alternating conducting switches, at least two switches will be kept conducted and no more than three switches can be turned on at a time. Hence, the operation

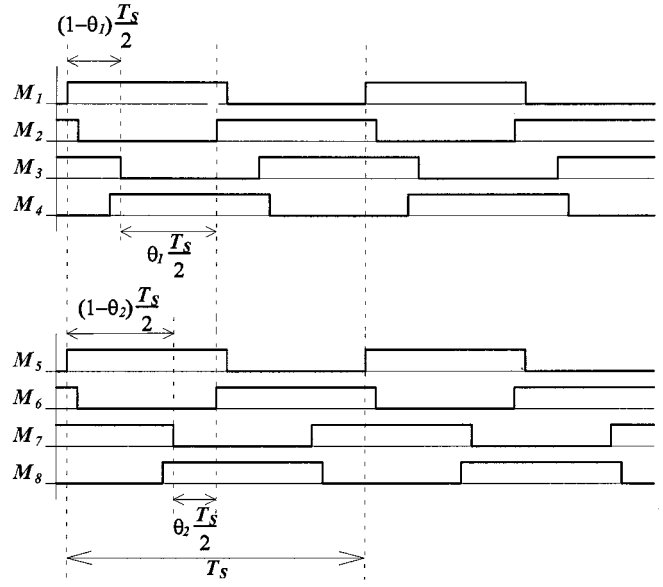


Fig. 2. Driving waveforms of MOSFETs $M_1 \sim M_8$ with phase-shifted PWM control.

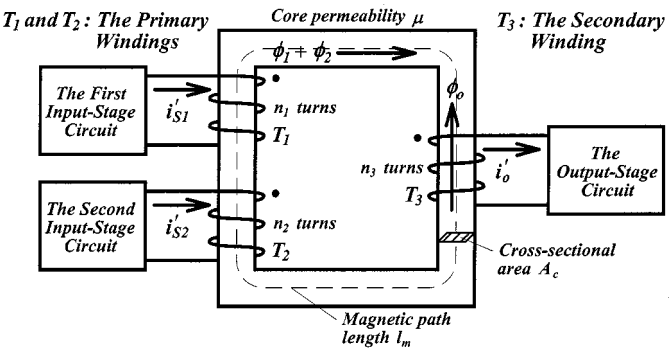


Fig. 3. Block diagram of the proposed converter.

of each input-stage circuit will not be affected by the clamped voltage of the transformer winding.

Some other important concepts for the proposed multi-input dc/dc converter are introduced as follows.

A. Magnetic Flux Additivity

The concept of the magnetic flux additivity is employed in the proposed two-input current-fed full-bridge dc/dc converter. Instead of combining input dc sources in the electric form, the proposed converter combines input dc sources in magnetic form by adding up the produced magnetic flux together in the magnetic core of the coupled transformer. To clearly describe the concept of the magnetic flux additivity employed in the proposed multi-input dc/dc converter, the schematic diagram shown in Fig. 1 is redrawn in Fig. 3 with an ideal transformer and three circuit block diagrams. By using Ampere's law, the net MMF F_T around a closed path of length l_m produced by i'_{S1} and i'_{S2} can be determined as

$$F_T = n_1 i'_{S1} + n_2 i'_{S2} = H_1 l_m + H_2 l_m \tag{1}$$

where n_1 and n_2 are turn numbers of the first and the second primary windings of the coupled transformer, and H_1 and H_2 are the magnetic field intensity produced by the primary winding currents i'_{S1} and i'_{S2}, respectively. The basic electromagnetic definition indicates

$$H = B/\mu \quad B = \phi_/ A_c \tag{2}$$

where B is the magnetic flux density, μ is the magnetic permeability of the transformer core, ϕ is the magnetic flux, and A_c is the cross-sectional area of the transformer. From (1) and (2), the net MMF can be expressed as

$$F_T = (\phi_1 + \phi_2)\frac{l_m}{\mu A_c} \tag{3}$$

where ϕ_1 and ϕ_2 are the magnetic flux produced by i'_{S1} and i'_{S2}, respectively. As a result, the net magnetic flux linkage in the magnetic core becomes $\phi_1 + \phi_2$, which is the summation of the magnetic flux produced by the two different current sources. By Lenz's law, the induced current i'_O in the secondary winding as shown in Fig. 3 should produce an opposite magnetic flux ϕ_O which tends to cancel $\phi_1 + \phi_2$. Hence, the magnitude of i'_O is determined by the magnetic flux linkage $\phi_1 + \phi_2$ which is the combination of i'_{S1} and i'_{S2} in the magnetic form.

B. Operating Stage

The following assumptions are made to simplify the analysis.

1) The inductances of choke inductors L_1 and L_2 are large enough that currents flowing through them are constant. The dc input voltage sources V_{S1} and V_{S2} with their associated choke inductors L_1 and L_2 can be considered as constant current sources I_{S1} and I_{S2}.
2) The transformer is assumed to be ideal. Thus, the leakage inductance and magnetizing current can be neglected and winding voltages can be determined by turn ratios of these windings.
3) All switching devices, MOSFETs and diodes, are considered ideal.
4) The output filter capacitor is large enough that the output voltage V_O is constant.

Based on the above assumptions, the operation of the proposed two-input current-fed full-bridge dc/dc converter over one full switching cycle can be divided into 12 different operating stages. The timing diagrams for the gate driving signals $v_{GS1} \sim v_{GS8}$, the current and voltage waveforms for transformer windings $T_1 \sim T_3$, and the voltage waveforms of choke inductors L_1 and L_2 are illustrated in Fig. 4. The equivalent circuits of each operating stage are shown in Fig. 5(a)–(l). For the sake of brevity, only six operating stages over one-half switching cycle will be described here since the remaining six operating stages within the other half switching cycle are symmetrical to the first six operating stages.

Just before t_0, as shown in Fig. 5(l), the input current I_{S1} in the first input-stage circuit was freewheeling through D_1, M_1, D_3, and M_3 and the input current I_{S2} in the second input-stage circuit was freewheeling through D_5, M_5, D_7, and M_7. Diodes in the output-stage circuit are all reverse biased. There is no power transferring from any input-stage circuit to the output-stage circuit. Additionally, M_4 was turned on but conducted no current.

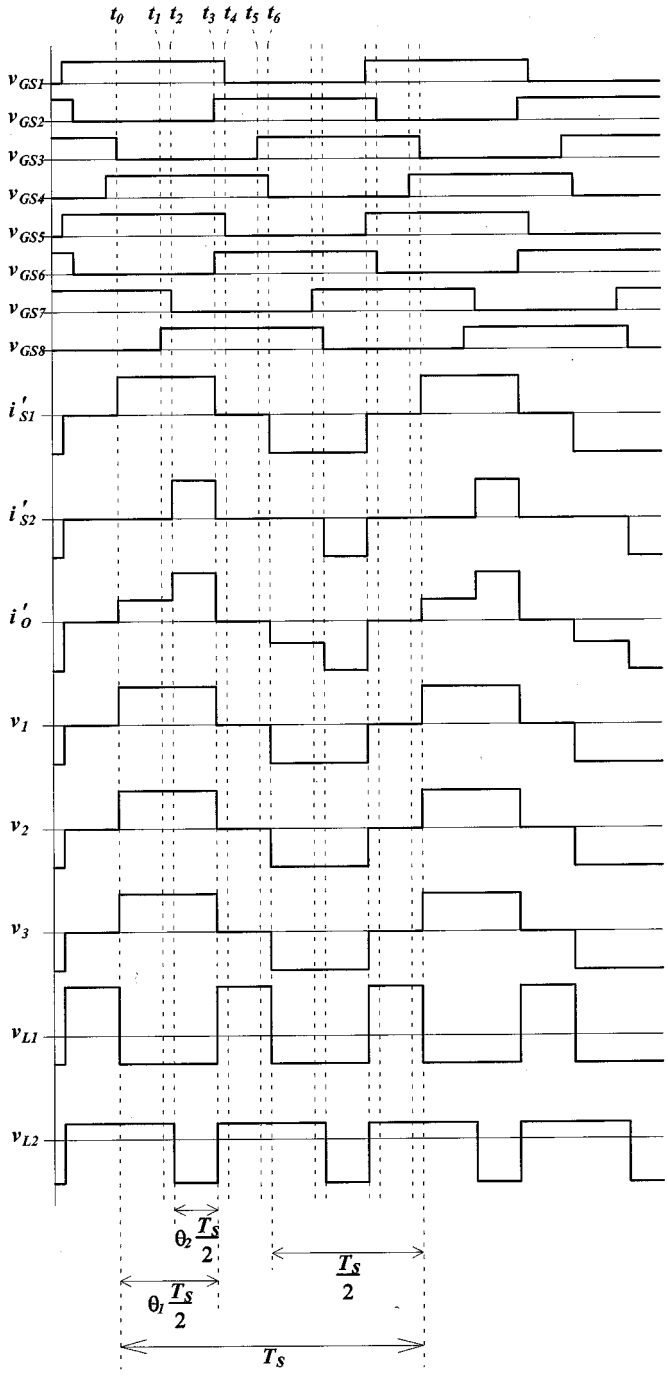


Fig. 4. Conceptual current and voltage waveforms of key components.

1) Stage 1—$(t_0 \leqq t < t_1)$*:* At time instant t_0, M_3 is turned off. Power starts to flow from the first input-stage circuit through the transformer to the load. The current source I_{S1} in the first input-stage circuit will flow through the first transformer winding T_1 via switches D_1, M_1, D_4, and M_4, while I_{S2} is still kept freewheeling in the second input-stage circuit. The magnetic flux produced by the first winding current i'_{S1} will induce voltages on other transformer windings. Induced voltages across transformer windings T_1, T_2, and T_3 are clamped to n_1V_O/n_3, n_2V_O/n_3, and V_O, respectively. Diodes D_9 and D_{12} in the output-stage circuit will be turned on because of the induced transformer winding voltage V_3, which causes the body diode of MOSFET M_8 to be forward biased. The equivalent circuit of stage 1 is shown in Fig. 5(a).

2) Stage 2—$(t_1 \leqq t < t_2)$*:* At time instant t_1, M_8 is turned on at zero voltage due to its forward-biased body diode in the previous operating stage. That is, M_8 is operated with zero-voltage switching (ZVS) at turn-on transition. The equivalent circuit of stage 2 is shown in Fig. 5(b). During this stage, M_8 is turned on but conducts no current. The input current I_{S2} is still kept freewheeling through D_5, M_5, D_7, and M_7 in the second input-stage circuit. Operations of the first input-stage and the output-stage circuits remain unchanged.

3) Stage 3—$(t_2 \leqq t < t_3)$*:* This stage begins when MOSFET M_7 is turned off at t_2. As shown in Fig. 5(c), the current source, I_{S2}, in the second input-stage circuit will flow through the second transformer winding T_2 via switches D_5, M_5, D_8, and M_8 and start to transfer power to the load. During this operating stage, both the first and the second input-stage circuits are delivering power to the load simultaneously. The total magnetic flux linkage in the coupled transformer is increased because of the additional magnetic flux produced by the second winding current i'_{S2}. The operation of the output-stage circuit and the clamped transformer winding voltages remain unchanged.

4) Stage 4—$(t_3 \leqq t < t_4)$*:* At time instant t_3, both M_2 and M_6 are turned on and low-impedance circuit branches $D_2 \rightarrow M_2 \rightarrow D_4 \rightarrow M_4$ and $D_6 \rightarrow M_6 \rightarrow D_8 \rightarrow M_8$ are formed for current sources I_{S1} and I_{S2}, respectively. The equivalent circuit of this operating stage is shown in Fig. 5(d). MOSFETs M_1 and M_5 are still kept on but conduct no current. The input currents I_{S1} and I_{S2} are freewheeling through these low-impedance routes and no current will flow through the transformer windings. All of the diodes in the output-stage circuit will be reverse biased since all of the transformer winding voltages are clamped to zero because of the freewheeling currents in the two input-stage circuits. No power is transferred from any input-stage circuit to the output-stage circuit. The power demanded by the load is provided by the output filter capacitor C.

5) Stage 5—$(t_4 \leqq t < t_5)$*:* As shown in Fig. 5(e), MOSFETs M_1 and M_5 are turned off with zero current at t_4. That is, M_1 and M_5 are operated with zero-current switching (ZCS) at turn-off transition. The current sources I_{S1} and I_{S2} are kept freewheeling in the input-stage circuits, and no power is delivered to the load.

6) Stage 6—$(t_5 \leqq t < t_6)$*:* At time instant t_5, M_3 is turned on at zero voltage due to the clamped zero voltage across the first transformer winding T_1. That is, M_3 is operated with ZVS at turn-on transition. The rest of the circuit is the same as described in the previous operating stage. Two current sources are freewheeling in the input-stage circuits and no power is delivered to the load. The equivalent circuit is shown in Fig. 5(f).

Stage 7 begins when M_4 is turned off at t_6. The equivalent circuit shown in Fig. 5(g) is similar to the equivalent circuit shown in Fig. 5(a) with symmetrical conducting and freewheeling switches in the input-stage and output-stage circuits. Also, the polarity of transformer voltages and currents are opposite to those shown in stage 1. Consequently, stages 8–12 can be found to be symmetrical to stages 2–6, also.

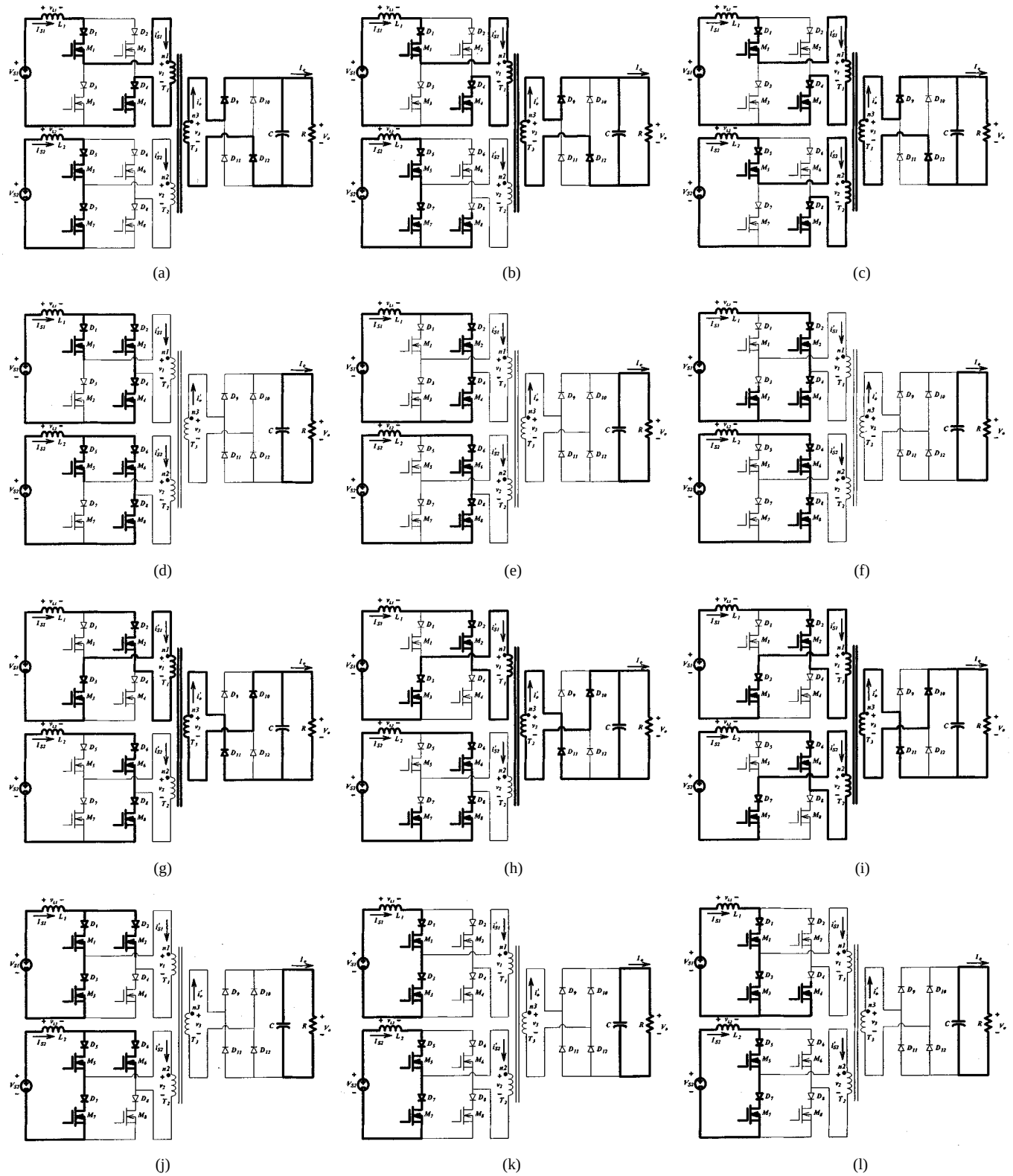


Fig. 5. Equivalent circuits of operating stages. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6. (g) Stage 7. (h) Stage 8. (i) Stage 9. (j) Stage 10. (k) Stage 11. (l) Stage 12.

According to the operating stages described above, all the MOSFETs in the proposed converter can achieve either ZCS or ZVS. The upper MOSFETs in each input-stage circuit are operated with ZCS at turn-off transition while the lower MOSFETs are operated with ZVS at turn-on transition.

C. Output Voltage and Current

In the phase-shifted PWM control scheme for the proposed full-bridge dc/dc converter, the regulation of the output voltage V_O is achieved by adjusting the phase-shift percentage of gate

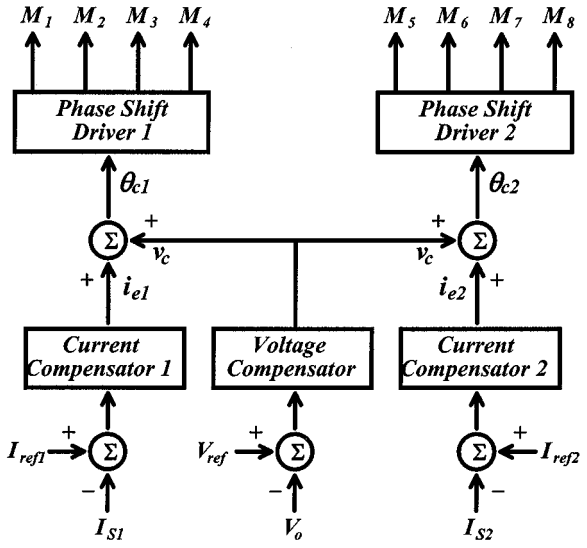


Fig. 6. Block diagram of the control circuit for the proposed converter.

signals. As shown in Fig. 2, the phase-shift percentage represents the percentage of the converter operated in the power transferring stage over a switching period. In order to have different amount of power delivered from different input-stage circuits to the load, two different phase-shift percentages θ_1 and θ_2 are needed. Hence, the output voltage and input currents are all related to the phase-shift percentages.

By referring to the waveform of v_{L1} shown in Fig. 4, the voltage across inductor L_1 during the power transferring stage can be expressed as

$$v_{L1} = V_{S1} - \frac{n_1}{n_3} V_O \tag{4}$$

and the one for the freewheeling stage is

$$v_{L1} = V_{S1} \tag{5}$$

where n_1 and n_3 are the turn numbers of the first and the third winding of the transformer, and V_{S1} is the input dc voltage in the first input stage. In steady state, the average inductor voltage V_{L1} must be equal to zero. Hence, the following equation can be obtained:

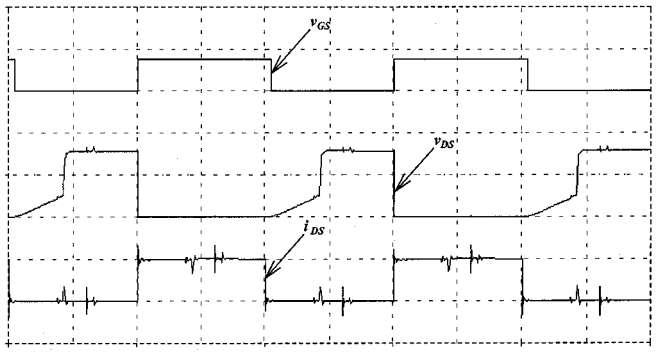
$$V_{L1} = \left(V_{S1} - \frac{n_1}{n_3} V_O\right) \theta_1 \frac{T_S}{2} + V_{S1}(1-\theta_1)\frac{T_S}{2} = 0 \tag{6}$$

where θ_1 is the phase-shift percentage for the first input-stage circuit, and T_S is the switching period. Then, by using (6), the relationship between V_{S1} and V_O can be derived as

$$V_{S1} = \frac{n_1}{n_3} \theta_1 V_O. \tag{7}$$

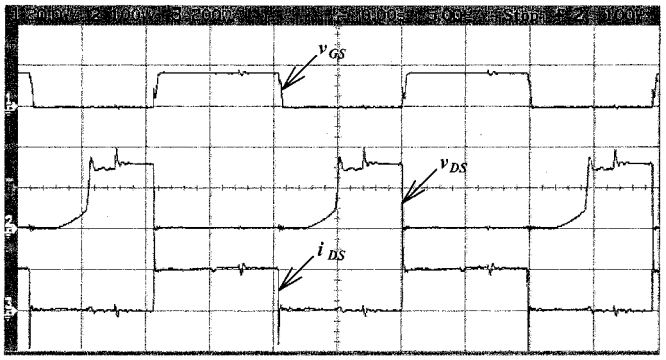
By using a similar procedure, the relationship between input dc voltage V_{S2} and output voltage V_O can be derived as

$$V_{S2} = \frac{n_2}{n_3} \theta_2 V_O \tag{8}$$



(v_{GS}: 20 V/div, v_{DS}: 100 V/div, i_{DS}: 2 A/div, 5 μs/div)

(a)



(v_{GS}: 20 V/div, v_{DS}: 100 V/div, i_{DS}: 2 A/div, 5 μs/div)

(b)

Fig. 7. (a) Simulated waveforms of the gate signal v_{GS}, drain–source voltage v_{DS}, and drain current i_{DS} of MOSFET M_5. (b) Measured waveforms of the gate signal v_{GS}, drain–source voltage v_{DS}, and drain current i_{DS} of MOSFET M_5.

where θ_2 is the phase-shift percentage for the second input-stage circuit. The output power P_O is the summation of the input power P_{S1} and P_{S2} and can be expressed as

$$V_O I_O = V_{S1} I_{S1} + V_{S2} I_{S2}. \tag{9}$$

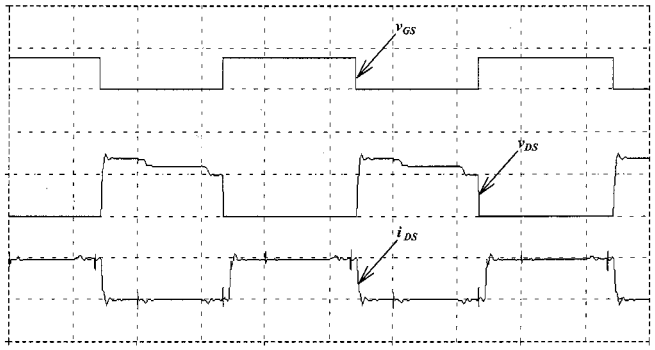
By substituting (7) and (8) into (9), the output current I_O can be determined by the following equation:

$$I_O = \frac{n_1}{n_3} \theta_1 I_{S1} + \frac{n_2}{n_3} \theta_2 I_{S2}. \tag{10}$$

In order to regulate the output voltage, a voltage feedback signal is needed to dynamically control the phase-shift percentage of each input-stage circuit. Also, in order to control the power delivered from each input-stage circuit, current command signals for input-stage circuits are needed.

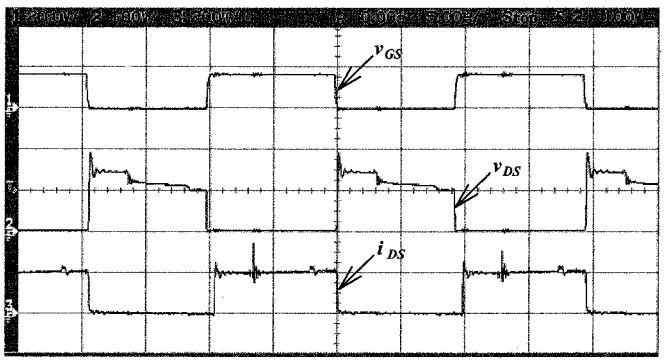
D. Control Strategy

The block diagram of the control circuit for the proposed multi-input converter is shown in Fig. 6, where V_O is the output voltage, $V_{\rm ref}$ is the reference voltage, I_{S1} and I_{S2} are the actual input currents, and $I_{\rm ref1}$ and $I_{\rm ref2}$ are the reference input currents. In Fig. 6, the phase-shift control signal θ_{c1} is the summation of the voltage control signal v_c and the current error signal i_{e1}, while θ_{c2} is the summation of v_c and i_{e2}. The phase-shift percentage of gate signals for each input-stage circuit can be determined when the phase-shift control signals θ_{c1} and θ_{c2} are



(v_{GS}: 20 V/div, v_{DS}: 100 V/div, i_{DS}: 2 A/div, 5 μs/div)

(a)



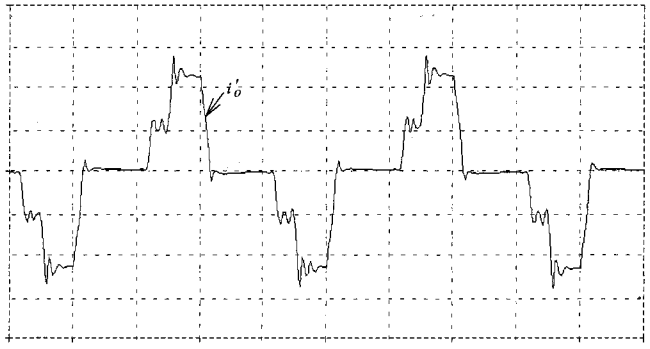
(v_{GS}: 20 V/div, v_{DS}: 100 V/div, i_{DS}: 2 A/div, 5 μs/div)

(b)

Fig. 8. (a) Simulated waveforms of the gate signal v_{GS}, drain–source voltage v_{DS}, and drain current i_{DS} of MOSFET M_8. (b) Measured waveforms of the gate signal v_{GS}, drain–source voltage v_{DS}, and drain current i_{DS} of MOSFET M_8.

(i'_{S1}: 2 A/div, i'_{S2}: 2 A/div, 5 μs/div)

(a)



(i'_O: 2 A/div, 5 μs/div)

(b)

Fig. 9. (a) Simulated waveforms of the transformer input current i'_{S1} and i'_{S2}. (b) Simulated waveforms of the transformer output current i'_O.

sent to the phase-shift drivers. By adjusting the phase-shift percentage with proper current control signals, the regulation of the output voltage V_O can be achieved and the balanced power flow from different input-stage circuits to the load can be obtained. If a constant output voltage with constant output power is demanded by the load, which could be a resistor, then only one of the two current reference signals shown in Fig. 6 can exist and the other should be disconnected. The input-stage circuit with reference current signal will provide a constant power to the load and the other input-stage circuit without the reference current signal will automatically deliver the remaining portion of the demanded output power to balance the power flow. If each power source for the input-stage circuit has to supply specified power, e.g., solar arrays with maximum power point tracking, then both of the reference current signals should be used to transfer the demanded input power. Meanwhile, the load, such as a battery bank, has to be able to accept a changeable output power in order to meet the balanced power transformation. In addition, voltage values of the two input dc sources for the proposed multi-input converter can be different since the input-stage circuits are current-fed full-bridge inverters.

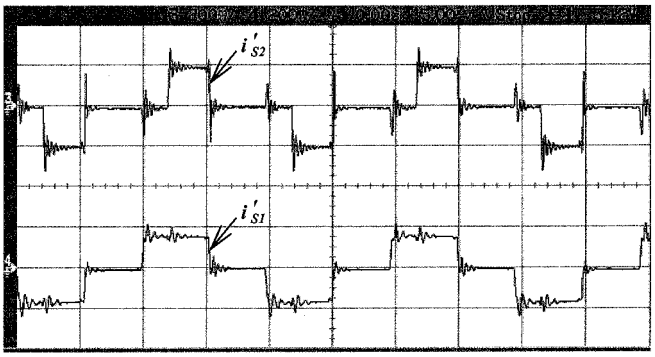
III. Simulation and Experiment Results

In this section, a prototype of the proposed two-input current-fed phase-shifted full-bridge dc/dc converter with the following specifications is implemented to verify the theoretical analysis:

1) input dc voltage: $V_{S1} = 80$ V, $V_{S2} = 50$ V;
2) output dc voltage: $V_O = 100$ V;
3) input current: $I_{S2} = 2$ A;
4) output current: $I_O = 2$ A;
5) switching frequency: $f_s = 50$ kHz;
6) power MOSFETs ($M_1 \sim M_8$): IRF634;
7) reverse-blocking diodes ($D_1 \sim D_8$): 8ETH03;
8) transformer turn ratio: $n_1 : n_2 : n_3 = 4 : 4 : 3$.

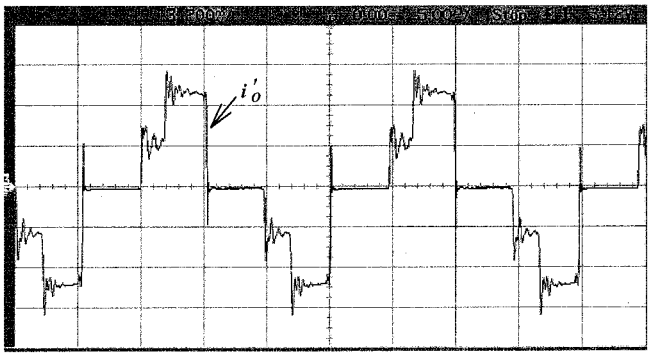
Computer simulations of the prototype by using PSpice are also included for comparisons. Fig. 7(a) and (b) shows the simulated and measured waveforms of the gate signal v_{GS}, drain–source voltage v_{DS}, and drain current i_{DS} of MOSFET M_5, respectively. It can be seen that the MOSFET M_5 is operated with ZCS at turn-off transition. In fact, all upper MOSFETs in each input-stage circuit of the proposed converter are operated with ZCS at turn-off transition with similar drain–source voltage and drain current waveforms. On the other hand, the simulated and measured waveforms of v_{GS}, v_{DS}, and i_{DS} of M_8 with ZVS at turn-on transition are shown in Fig. 8(a) and (b), respectively. Actually, all lower MOSFETs in each input-stage circuit of the proposed converter are operated with ZVS at turn-on transition. Noises appearing in voltage and current waveforms are caused by the parasitic elements of the switching devices and the transformer.

Fig. 9 shows the simulated waveforms of the transformer input current i'_{S1} and i'_{S2}, and the transformer output current i'_O,



(i'_{S1}: 2 A/div, i'_{S2}: 2 A/div, 5 μs/div)

(a)



(i'_O: 2 A/div, 5 μs/div)

(b)

Fig. 10. (a) Measured waveforms of the transformer input current i'_{S1} and i'_{S2}. (b) Measured waveforms of the transformer output current i'_O.

while the measured ones are shown in Fig. 10. From Figs. 9 and 10, it can be shown that the transformer output current i'_O is the combination of the transformer input current i'_{S1} and i'_{S2}, which results from the concept of the magnetic flux additivity. It also illustrates that power can be delivered from these two voltage sources to the load individually and simultaneously. In order to demonstrate the efficiency performance of the proposed multi-input converter, curves of efficiency η versus output power P_O for different operating conditions as listed in Table I are plotted in Fig. 11. It can be seen that the proposed multi-input converter has the minimum efficiency of 84% for various operating conditions. These experimental results verify the performance of the proposed multi-input dc/dc converter with the phase-shifted PWM control.

IV. Conclusion

A multi-input current-fed full-bridge dc/dc converter has been proposed in this paper. Instead of combining input dc sources in the electric form, the proposed converter combines input dc sources in magnetic form by adding up the produced magnetic flux together in the magnetic core of the coupled transformer. The proposed converter has the following advantages: 1) magnitudes of dc input voltages can be different; 2) dc sources can deliver power individually and simultaneously; 3) the soft-switching technology is accessible; and 4) the electric isolation is naturally achieved. The development of the proposed multi-input dc/dc converter was presented in detail. The operation principle of the proposed converter based on the flux additivity was introduced. Different operating stages and their equivalent circuits were explained. Mathematical equations of the output voltage and current were derived. The phase-shifted PWM control strategy was illustrated. A prototype of the proposed converter has been successfully implemented. The feasibility and the performance of the proposed multi-input dc/dc converter were verified by computer simulation results and hardware experimental measurements.

TABLE I
Different Operating Conditions of the Proposed Multi-Input DC/DC Converter

Case 1	V_{S1}= 80 V, V_{S2}= 50 V, I_{S2}= 2 A, V_O= 100 V
Case 2	V_{S1}= 80 V, V_{S2}= 50 V, I_{S2}= 1 A, V_O= 100 V
Case 3	V_{S1}= 50 V, V_{S2}= 80 V, I_{S2}= 1 A, V_O= 100 V
Case 4	V_{S1}= 50 V, V_{S2}= 80 V, I_{S2}= 1.2 A, V_O= 100 V

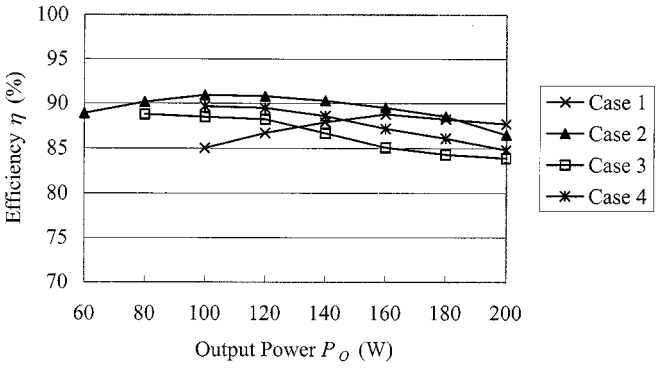


Fig. 11. Curves of efficiency η versus output power P_O for different operating conditions as listed in Table I.

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Yaow-Ming Chen (S'96–M'98) received the B.S. degree from National Cheng-Kung University, Tainan, Taiwan, R.O.C., and the M.S. and Ph.D. degrees from the University of Missouri, Columbia, in 1989, 1993, and 1997, respectively, all in electrical engineering.

From 1997 to 2000, he was with I-Shou University, Taiwan, R.O.C., as an Assistant Professor. In 2000, he joined National Chung Cheng University, where he is currently an Assistant Professor in the Department of Electrical Engineering. His research interests include power electronic converters, power system harmonics and compensation, and intelligent control.

Dr. Chen is a member of the IEEE Power Electronics and IEEE Industrial Electronics Societies.

Yuan-Chuan Liu was born in Chia-Yi, Taiwan, R.O.C., in 1973. He received the B.S. degree in 1996 from the Department of Electrical Engineering, National Chung Cheng University, Chia-Yi, Taiwan, R.O.C., where he is currently working toward the Ph.D. degree in the Power Electronics Applied Research Laboratory (PEARL).

His research interests include developing and designing of converter topologies, power-factor correctors, and electronic ballasts.

Feng-Yu Wu was born in Tainan, Taiwan, R.O.C., in 1977. He received the B.S. degree from the Department of Electrical Engineering, Southern Taiwan University of Technology, Tainan, Taiwan, R.O.C., in 2000. He is currently working toward the M.S. degree at National Chung Cheng University, Chia-Yi, Taiwan, R.O.C.

His research interests include electronic dimming ballasts, power converters, and microprocessor-based application systems.