Multi-Output DC-DC Converters Based on Diode-clamped Converters Configuration: Topology and Control Strategy

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Abstract

This paper presents a new DC-DC Multi-Output Boost (MOB) converter which can share its total output between different series of output voltages for low and high power applications. This configuration can be utilised instead of several single output power supplies. This is a compatible topology for a diode-clamed inverter in the grid connection systems, where boosting low rectified output-voltage and series DC link capacitors is required. To verify the proposed topology, steady state and dynamic analysis of a MOB converter are examined. A simple control strategy has been proposed to demonstrate the performance of the proposed topology for a double-output boost converter. The topology and its control strategy can easily be extended to offer multiple outputs. Simulation and experimental results are presented to show the validity of the control strategy for the proposed converter.

1. Introduction

DC-DC converters are widely used in low and high power applications. Recently, multi-output DC-DC converters have been employed with multiple inductors, in which, for M output voltage, M inductors are required. As the number of output voltages increases, the number of required inductors will also be increased which leads to an increase in the cost and size of the system. A new generation of Single-Inductor Multiple-Output (SIMO) DC-DC converters have been addressed in [1] based on buck, boost, and buck-boost topology. This approach reduces the number of external bulky components such as inductors and power switches, leading to decreased cost and losses in the system. Several voltage [2] and current control [3, 4] techniques have been applied for SIMO converters to improve the dynamic performance in CCM or DCM operation. However, in these configurations, loads are independently constructed (Fig.1).

This paper presents a new single inductor MOB converter structure with series regulated output voltages. Series regulated DC voltages may be required in different low and high power applications. One of the most interesting applications of this new family of DC-DC converters is the boosting and regulating the low and variable output voltage of renewable energy for the DC link of grid connected systems [5-7], based on multilevel inverters. Multilevel inverters can synthesise the output voltage with more voltage steps, which approaches the reference with low harmonic distortion as well as low switching frequency compared with traditional converters. Also, as the transformers operating at the line frequency are bulky and high-priced, the need for the direct connection of these systems to a high and medium voltage grid forces the modification

of the single-phase or three-phase multilevel topologies [5]. Among them, diode-clamped is the most common type of converter, widely used in wind turbine and photovoltaic applications [8, 9]. However, the most crucial issue in diode-clamped topology is the neutral point voltage balancing [10-13]. Using an MOB converter at the DC link voltage of the diode-clamped inverter can solve the capacitor voltage imbalance and help to simplify the control strategy. To verify the feasibility of the MOB converter's topology, both steady state and dynamic analysis have been carried out. A current control strategy combined with voltage control has been utilized to keep the simplicity of the system as it can be extended from a double-output converter to a multi-output converter without a significant change in the control circuit. This control strategy may be implemented by a combination of analogue and logical ICs, or a simple microcontroller to keep the output voltages of the MOB converter at desired voltages against variation in load or input voltage. Finally, simulation and experimental results have been presented to show the validity of the control strategy and proposed topology.

2. Basic Circuit Configuration

A circuit diagram of the *N*-output boost converter is shown in Fig.2 (a). This circuit consists of a boost switch S_0, *N-1* sharing switches S_1 to S_{N-1}, *N* diodes (D_1 to D_N), an inductor, and *N* capacitors (C_1 to C_N) with different loads (R_1 to R_N). In the subinterval zero, S_0 is turned "on" and the inductor can be charged by the current flowing through it. In the next *N* subintervals, S_0 remains "off" and the S_1 to S_{N-1} are switched to charge *N-1* capacitors into the desired value. When S_1 to S_{N-1} are "off", the diode (D_N) directs the inductor current to charge all C_1 to C_N to generate V_1 to V_N, respectively. D_1 to D_{N-1} are used to block the negative voltage and provide two quadrant operation of S_1 to S_{N-1}. In a double-output converter there are three possible switching states as S_1 can not be turned "on" while S_0 is "on". The operation of the circuit in three different switching states has been summarised in Table 1 for *N=2*. The equivalent circuits of all switching states have been demonstrated in Fig.2 (b) to 2(d).

Table 1: Switching states of double-output boost converter

Switching states	S_0	S_1	C_1	C_2
10	on	off	Discharge	Discharge
00	off	off	Charge	Charge
01	off	on	Charge	Discharge

Fig.3 shows the proposed DC-DC converter connected to a three-level diode-clamped inverter. By controlling the proposed DC-DC converter, the DC link capacitors of the inverter can be regulated to the desired voltage level. Therefore, the MOB converter can address the capacitor voltage balancing in diode-clamped converters, which then will decrease the complexity of the inverter control strategy.

2.1. Steady State Equations

To analyse the steady state performance of the MOB converter, time intervals of each switching are considered as T_{10}, T_{00}, and T_{01}. Then, switching period can be expressed as follows:

$$T_{10} + T_{00} + T_{01} = T \quad (1)$$

where, T is switching period. Based on the averaging technique and waveforms shown in Fig.4, the average inductor voltage over one cycle should be zero in the steady state:

$$T_{10}(V_{in}) + T_{00}(V_{in} - V_1 - V_2) + T_{01}(V_{in} - V_1) = 0 \quad (2)$$

By definition of duty cycles in Eq.3 and substitution in Eq.2, it can be rewritten as follows:

$$\begin{cases} (D_0 + D_1)' = \dfrac{(T_{00})}{T} \\ D_0' = \dfrac{(T_{00} + T_{01})}{T} \end{cases} \quad (3)$$

$$V_{in} = (D_0')V_1 + (D_0 + D_1)'V_2 \quad (4)$$

where, V_{in} is input voltage and V_1 and V_2 are the bottom capacitor (mid point) and top capacitor voltages, respectively. Also, the average capacitor current over one cycle should be zero in the steady state.

$$\begin{cases} T_{10}\left(-\dfrac{V_1}{R_1}\right) + T_{00}\left(I - \dfrac{V_1}{R_1}\right) + T_{01}\left(I - \dfrac{V_1}{R_1}\right) = 0 \\ I = \dfrac{V_1}{R_1(D_0')} \end{cases} \quad (5)$$

$$\begin{cases} T_{10}\left(-\dfrac{V_2}{R_2}\right) + T_{00}\left(I - \dfrac{V_2}{R_2}\right) + T_{01}\left(-\dfrac{V_2}{R_2}\right) = 0 \\ I = \dfrac{V_2}{R_2(D_0 + D_1)'} \end{cases} \quad (6)$$

From Eq.4 to Eq.6, the steady state equation can be derived as follows:

$$\begin{cases} V_1 = \dfrac{n(D_0')V_{in}}{n(D_0')^2 + (D_0 + D_1)'^2} \\ V_2 = \dfrac{(D_0 + D_1)'V_{in}}{n(D_0')^2 + (D_0 + D_1)'^2} \\ I = \dfrac{V_{in}}{R_1(D_0')^2 + R_2(D_0 + D_1)'^2} \end{cases} \quad (7)$$

where, $n = \dfrac{R_1}{R_2}$. According to Eq.7, two different voltages can be obtained on output. Comparing this situation with the basic single output (V_1) Boost converter, although the total output voltage (V_T) in both converters is increased, in the MOB converter different output voltages can be obtained based on different duty cycles of the boost switch (S_0) and sharing switch (S_1) in steady state operations. Since the output voltage in Eq.7 is related to the load ratio, Table 2 shows some limitations to achieve diverse voltages that should be considered due to the fundamental nature of the circuit.

Table 2: Nature limitation of load ratio in different output voltage

$V_1 = V_2$	$n = \dfrac{(D_0 + D_1)'}{D_0'}$
$V_1 > V_2$	$n > \dfrac{(D_0 + D_1)'}{D_0'}$
$V_1 < V_2$	$n < \dfrac{(D_0 + D_1)'}{D_0'}$

Regarding Fig.4 in steady state operation, peak to peak inductor current variation (ΔI) in CCM will be:

$$L\frac{\Delta I}{D_0 T} = V_{in} \Rightarrow \Delta I = \frac{V_{in} D_0 T}{L} \quad (8)$$

Also, Eq.9 and Eq.10 show the peak to peak voltage ripple of output voltages.

$$\frac{\Delta V_1}{V_1} = \frac{D_0 T}{R_1 C_1} \tag{9}$$

$$\frac{\Delta V_2}{V_2} = \frac{(D_0 + D_1)T}{R_2 C_2} \tag{10}$$

By substitution of Eq.8 in Eq.9 and Eq.10, output voltage ripple can be derived as follows:

$$\begin{cases} \dfrac{\Delta V_1}{V_1} = \dfrac{\Delta IL}{R_1 C_1 V_{in}} \\ \dfrac{\Delta V_2}{V_2} = \dfrac{\Delta IL}{R_2 C_2 V_{in}} + \dfrac{D_1 \Delta IL}{D_0 R_2 C_2 V_{in}} \end{cases} \tag{11}$$

Regarding Eq.11, the percentage of ripple in V_1 is related to ΔI as the other parameters are of constant value in a steady state operation. However, the percentage of ripple in V_2 is associated with the ratio of $\frac{D_1}{D_0}$ in addition to ΔI.

2.2. Dynamic Model

Using an averaging method in each switching cycle, state equations can be developed for the dynamic analysis of inductor current or capacitor voltages in terms of systems variables. To construct a small-signal ac model at the quiescent operation (I, V_1, V_2), we can assume a small perturbation at the operating point. Thus, all input and output variables are defined as $x(t) = X + \hat{x}(t)$ where X is a DC amount and x (t) is an AC small-signal.

$$\begin{aligned} L\frac{di(t)}{dt} &= \frac{1}{T}[t_{10}(t)(v_{in}(t)) + t_{00}(t)(v_{in}(t) - v_1(t) - v_2(t)) + t_{01}(t)(v_{in}(t) - v_1(t))] \\ C_1\frac{dv_{1(t)}}{dt} &= \frac{1}{T}[t_{10}\left(-\frac{v_1(t)}{R_1}\right) + t_{00}(t)\left(i(t) - \frac{v_1(t)}{R_1}\right) + t_{01}(t)\left(i(t) - \frac{v_1(t)}{R_1}\right)] \\ C_2\frac{dv_2(t)}{dt} &= \frac{1}{T}[t_{10}(t)\left(-\frac{v_2(t)}{R_2}\right) + t_{00}(t)\left(i(t) - \frac{v_2(t)}{R_2}\right) + t_{01}(t)\left(-\frac{v_2(t)}{R_2}\right)] \end{aligned} \tag{12}$$

Regarding Eq.3 and linearization method, Eq.13 shows the dynamic model space state of the proposed configuration.

$$\begin{bmatrix} L & 0 & 0 \\ 0 & C_1 & 0 \\ 0 & 0 & C_2 \end{bmatrix}\begin{bmatrix} \dot{i} \\ \dot{v}_1 \\ \dot{v}_2 \end{bmatrix} = \begin{bmatrix} 0 & -(D_0') & -(D_0 - D_1)' \\ (D_0') & -\frac{1}{R_1} & 0 \\ (D_0 - D_1)' & 0 & -\frac{1}{R_2} \end{bmatrix}\begin{bmatrix} i \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 1 & V_1 + V_2 & V_1 \\ 0 & -I & 0 \\ 0 & -I & -I \end{bmatrix}\begin{bmatrix} \hat{v}_{in} \\ \hat{d}_0 \\ \hat{d}_1 \end{bmatrix} \tag{13}$$

According to Eq.12 and Eq.13, changing $(D_0+D_1)'$ and D_0' with a different ratio in a closed loop control system can keep the output voltages constant while the inductor current value has been modified. Developing this concept will lead to a current control strategy combined with voltage control to achieve the desired output voltage with a proper dynamic response. Regarding the steady state statements and dynamic model, the proposed MOB converter acts as a boost converter topology with a series of multiple output voltages.

2.3. MOB Converter with Multiple Outputs Configuration

Steady state and dynamic analysis can be extended for the proposed topology with multiple outputs (see Fig.2 (a)). Rewriting the state space variables for N outputs:

$$\begin{bmatrix} L & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & C_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \ddots & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_i & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \ddots & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_j & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \ddots & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & C_k \end{bmatrix} \begin{bmatrix} \dot{i} \\ \dot{v}_1 \\ \vdots \\ \dot{v}_i \\ \vdots \\ \dot{v}_j \\ \vdots \\ \dot{v}_K \end{bmatrix} = \begin{bmatrix} 0 & -(1-D_0) & \cdots & -(1-\sum_{k=1}^{i} D_{K-1}) & \cdots & -(1-\sum_{k=1}^{j} D_{K-1}) & \cdots & -(1-\sum_{k=1}^{n} D_{K-1}) \\ (1-D_0) & \frac{1}{R_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ \vdots & 0 & \ddots & 0 & 0 & 0 & 0 & 0 \\ (1-\sum_{k=1}^{i} D_{K-1}) & 0 & 0 & \frac{1}{R_i} & 0 & 0 & 0 & 0 \\ \vdots & 0 & 0 & 0 & \ddots & 0 & 0 & 0 \\ (1-\sum_{k=1}^{j} D_{K-1}) & 0 & 0 & 0 & 0 & \frac{1}{R_j} & 0 & 0 \\ \vdots & 0 & 0 & 0 & 0 & 0 & \ddots & 0 \\ (1-\sum_{k=1}^{n} D_{K-1}) & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{R_k} \end{bmatrix} \begin{bmatrix} i \\ v_1 \\ \vdots \\ v_i \\ \vdots \\ v_j \\ \vdots \\ v_K \end{bmatrix} + \begin{bmatrix} 1 & \sum_{k=1}^{n} V_K & \cdots & \sum_{k=1}^{n-i} V_K & \cdots & \sum_{k=1}^{n-j} V_K & \cdots & V_1 \\ 0 & -I & 0 & 0 & \cdots & 0 & \cdots & 0 \\ 0 & -I & -I & 0 & \cdots & 0 & \cdots & 0 \\ 0 & -I & -I & 0 & \cdots & 0 & \cdots & 0 \\ 0 & -I & -I & -I & \cdots & 0 & \cdots & 0 \\ 0 & -I & -I & -I & \cdots & 0 & \cdots & 0 \\ 0 & -I & -I & -I & \cdots & -I & \cdots & 0 \\ 0 & -I & -I & -I & \cdots & -I & \cdots & -I \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{d}_0 \\ \vdots \\ \hat{d}_i \\ \vdots \\ \hat{d}_j \\ \vdots \\ \hat{d}_{K-1} \end{bmatrix} \quad (14)$$

Extracting transfer function from these equations:

$$\begin{cases} I(s) = \dfrac{1}{Ls + \sum_{k=1}^{N} \left(\dfrac{R_k (1 - \sum_{j=1}^{k} D_{j-1})^2}{1 + R_k C_k s} \right)} \\ V_k(s) = \dfrac{R_k (1 - \sum_{j=1}^{k} D_{j-1}))}{1 + R_k C_k s} I(s) \end{cases} \quad (15)$$

Finally, the steady state equations for N output voltages would be:

$$V_k = \frac{R_K (1 - \sum D_{K-1}) V_{in}}{\sum R_K (1 - \sum D_{K-1})^2}, \quad I = \frac{V_{in}}{\sum R_K (1 - \sum D_{K-1})^2} \quad (16)$$

It is clear that different output voltages can be achieved based on different duty cycles.

3. Control System and Switching Strategy

Several current-mode control strategies have been conducted to improve the dynamic response converters [14-18]. To have the potential of combining the advantages of digital control and current mode control in a relatively simple controller realisation for a MOB converter, a cross voltage control (V_T) with an internal hysteresis current control loop has been performed combined with mid point voltage (V_1) control. Fig.5 illustrates the block diagram of the control method for a double-output boost converter. As shown, the solid loop is a cross voltage control with a hysteresis current control loop for the inductor current, in which the cross output of the MOB converter is controlled by switching the boost switch (S_0). The dashed loop is a mid point voltage control where a sharing switch (S_1) is forced to balance the capacitors' voltage.

3.1. Cross Voltage Control with Hysteresis Current Control Loop

This control loop consists of two cascaded control loops. The outer loop is a voltage control mode through which the reference current is modified based on voltage error to force this error to zero. The inner loop is the hysteresis current control which is the main loop that runs to forcibly constrain the inductor current between the hysteresis bands around the defined reference current.

3.1.1. Current Reference Generator Block

To find the correct current reference against any disturbance in load or input voltage, the reference current generator applies based on the level of total output voltage error. The reference current is modified discontinuously in discrete time to predict the desired inductor reference current to force the voltage error to zero. The signal to update the reference current is

generated from the PLD block. The reference current will be decreased (increased) whenever the error is more (less) than a defined dead band. Subsection “1” in Fig.6 (a) shows the flowchart of this control section. There is a gain (G) for closed loop control to change the step change of the reference current. The gain will be increased when the error is high and decreased when the error is low, in which dynamic response can be improved as the current step is changed in respect to the error. This block can be implemented by a sample and hold IC which can keep the current reference as an analogue signal and modify it based on the error signal. On the other hand, a microcontroller can generate a reference current according to the error.

3.1.2. Current Hysteresis Block

This block changes its output signal based on comparing the actual inductor current and its reference to track the reference current. Therefore, once the inductor current error hits the upper (lower) band, the output signals change to zero (one). In this manner, the inductor current is controlled in defined hysteresis band. The output of the hysteresis block applies to a Programmable Logic Device (PLD) block and the boost switch S_0. Since the S_0 is controlled by the hysteresis current control, the control law is defined as Eq.17.

$$\begin{aligned} &if \quad I \geq I_{ref} + B \quad then \quad S_0 = 0 \\ &if \quad I \leq I_{ref} - B \quad then \quad S_0 = 1 \end{aligned} \tag{17}$$

where, I, I_{ref}, B are the inductor actual current, inductor reference current, and hysteresis band height respectively. The control scheme of the hysteresis current control is depicted in subsection 2 in Fig.6 (a). This block can be implemented by a logic device or a simple program in a microcontroller.

3.2. Mid Point Voltage Control

Due to the nature of the proposed converter in Table 1, there is no chance to turn S_0 and S_1 “on” simultaneously. To balance the mid point of capacitors, only two switching states are utilisable (00 and 01). Although there is no chance to charge the C_2 regardless of C_1, the reference current generator can modify the total voltage (V_T=V_1+V_2) in this case. In the dead band voltage control block, the amount of mid point voltage (V_1) error is compared with the defined voltage dead band (assumed 1% of reference) , if the voltage is higher than the upper (lower) dead band output signal of block changes to one (zero). The output signal applies to the PLD block. The control scheme flowchart of the mid point voltage control is shown in subsection 3 in Fig.6 (a). It should be mentioned that defining the dead band can decrease unnecessary switching when the mid point voltage error is negligible; otherwise it can be set to zero to increase accuracy.

3.3. Programmable Logic Device (PLD)

This block involves two tasks. The first is designed to count the hysteresis pulses and enable signal for current reference generator block after a defined hysteresis pulses frequently. By doing so, the current reference does not change faster than the inductor current dynamics. Furthermore, the inductor reference current can change within a different number of hysteresis pulses to control the dynamic response.

The second task is to apply a proper switching state for S_1 to balance the mid point voltage. To do so, the best switching state is chosen from Table 3 to make an optimum balance between the actual output voltages and their references, during the discharging period of the inductor (S_0=*off*) in each switching cycle. Therefore, the duty cycle of S_1 (D_1) is defined to balance the mid point voltage. By receiving the digital signals from hysteresis and mid point voltage control block, proper signals for the current generator block and S_1 are generated by the PLD block, so that it can be implemented with a logic device or programmed in a microcontroller.

Table 3: Switching states based on V_1 position

Position of V_1	Switching state of S_0	Switching state of S_1
V_1 is below the reference voltage	S_0=*0*	S_1=*on*
V_1 is above the reference voltage	S_0=*0*	S_1=*off*

3.4. Switching Pattern and Flowchart of Control Strategy

The entire flowchart of the proposed control strategy has been depicted in Fig.6 (a). As illustrated, except for changing the inductor reference current that can be implemented with an analogue sample and hold IC, the other parts of the control are based on logic signals. Also, control circuit can easily be applied for multiple outputs by measuring the mid point voltages and controlling the relevant sharing switch of that point with the mid point voltage control. The switching pattern of S_0 and S_1 based on hysteresis block pulses and mid point voltage control has been demonstrated in Fig.6 (b). In the hysteresis current control, the hysteresis band of the current regulator is adjusted to control the switching frequency. By assuming the hysteresis band height as 2B and substituting it in Eq.8, the switching frequency can be calculated as follows:

$$2B=\frac{D_0 T\, V_{in}}{L} \Rightarrow \quad f_{sw}=\frac{V_{in}\, D_0}{2L\, B} \tag{18}$$

In Eq.18, switching frequency is defined based on hysteresis band height, rate of inductor, input voltage, and duty cycle. Therefore, by considering the constant hysteresis band and circuit parameter, the switching frequency is constant whenever the ratio of loads ($n = \frac{R_1}{R_2}$) is constant.

Also, by substituting of Eq.11 into Eq.18, the switching frequency can be calculated as follows, based on the voltage ripple:

$$\begin{cases} f_{sw} = \dfrac{V_1}{\Delta V_1} \times \dfrac{D_0}{R_1 C_1} \\ f_{sw} = \dfrac{V_2}{\Delta V_2} \times \dfrac{(D_0 + D_1)}{R_2 C_2} \end{cases} \tag{19}$$

Regarding Eq.19, the hysteresis band can be controlled to have a constant voltage ripple.

4. Simulation Results

To show the performance of the proposed converter under the presented control strategy, simulations in different conditions with load and input voltage variation have been performed. In all simulations L=1*mH*, C_1=C_2=0.1*mF*, V_{in}=100*V*, and the total output voltage (V_T) has been boosted to 300*V*. To show the ability of the system to control the mid point voltage (V_1) to the different value, it has been set for 200V which is twice the input voltage. As discussed, the time for modification of current reference and closed loop gain are the parameters in the control strategy which can affect the dynamic response. In

these simulations, the current generator block is enabled in each five hysteresis cycles as it can increase the stability of the system, and closed loop gain varies from 0.005 to 0.001 regarding to the value of voltage error. A controller function to generate a proper reference current against a load variation is simulated in Fig.7 (a), when the voltage is dropped due to an increment in load current. As it is exposed, the inductor reference current modification is proportional to the voltage error and it occurs after defined enable time. Increasing the enable time helps to increase the stability of the control strategy, however, it reduces the response of the system. Fig.7 (b) and 7 (c) illustrate the dynamic performance of the control scheme against variation in load and input voltage respectively. As has been shown, the reference current has been updated based on voltage error to achieve the desired output voltages. To show the validity of the control technique for more than double-output converters, Fig.7 (d) demonstrates the regulation of mid point voltages for triple-output converters.

5. Hardware results

To verify the proposed MOB converter with the control strategy, a prototype of a double-output converter has been developed and controlled. The instantaneous values of the inductor current and output voltages are used to compare the threshold values given by the hysteresis current control and the dead band voltage control respectively. The control signal is fed into the gate of the main switching device (IGBT) through the gate driver circuit which provides the necessary isolation of the switching signal ground and power ground. The Prototype of the power board for the double-output boost converter is shown in Fig.8.

In the laboratory prototype, two SK50 Gal 065 switches, which is a compact design of the IGBT and diode module suitable for the boost converter, are used as the main switching devices; S_0, S_1, and D_2. Also, an ultrafast diode (*MUR820G)* has been used in series with S_1. In the controller part, the *NEC V850E/IG3* microcontroller has been utilised to implement the control strategy. Skyper 32-pro is used as a gate driver, which can drive two switches independently and is compatible with the utilised IGBT module. Also, the load disturbances are applied using toggle switches. As the power supply used in the laboratory has current-limiting protection, the test has been conducted at low voltage. In all tests, the mid point voltage (V_1) and total output (V_T), are assumed to be kept at *20V* and *30V* respectively, while V_{IN}=*15V*. The steady-state response under the proposed control scheme is shown in Fig.9. The switching pulses (control signal) and the inductor-current waveforms are shown in Fig.9 (a) for the CCM operation of the converter with load resistances of $R_1=R_2=50\ \Omega$. From the waveforms shown Fig.9 (b), it is clear that the required output voltages are maintained under the proposed control scheme. Fig.9 (c) shows the voltage ripple of each output voltage corresponding to switching states which is discussed in theory.

The control strategy is tested under disturbances in both load and input voltage, and the corresponding variations in the output voltage and inductor current are demonstrated in Fig.10. In Fig.10 (a) R_2=*50* and R_1 is varied from *50* to *35* Ω and back, while in Fig.10 (b) both R_1 and R_2 are varied from *50* Ω-*35* Ω and *50* Ω-*25* Ω respectively. It is noted that the operation of the converter still remains in the CCM and the current modification applies in each five hysteresis cycles discontinuously. The output voltages display an undershoot (overshoot) for the load current increase (decrease), but they quickly settle

around the reference value. Also, due to the switching options to control V_1 and V_2, the controlling of V_1 surpasses the other output, so that it has less undershoot and overshoot. While the converter is working with a load of $R_1=R_2=50\ \Omega$ (CCM operation), a change in the input voltage from the *15–10 V* and back is applied. The change in the input voltage and the corresponding output-voltage waveforms are depicted in Fig.10 (c). It is observed that the total output voltage shows small undershoot (overshoot) for the input voltage increase (decrease) and settles down after a short time. However, the mid point voltage remains constant, and the transients in voltage are sufficiently diminished.

6. Conclusion

In this paper, a new DC-DC multi-output boost (MOB) converter has been presented, in which different output voltage sharing can be achieved by a given duty cycle for low and high power applications. In addition, to boost the low rectified output-voltage of renewable energy systems, the DC link capacitor imbalance problem in diode-clamped converter based systems could be avoided, which leads to a decrease in the complexity of inverter control. A simple and cost effective control strategy has been proposed to control the mid point voltage and also boost the low input voltage. A double-output MOB converter and its control strategy have been implemented by a laboratory prototype. Simulation and experimental results establish the success of the control strategy and the performance of the proposed converters. The proposed topology could easily be extended to offer multiple outputs. The salient features of the proposed scheme are as follows:

- Approaching multiple series output instead of one output voltage in DC-DC converters.
- Boosting and adjusting the low input voltage of renewable energy systems into different output voltages.
- Removing the capacitor voltage imbalance problem to decrease the complexity of the inverter control system by connecting the MOB converter to the DC link of diode-clamped converter.
- offering a simple control scheme based on logic signals which can easily be extended for structure with multiple output voltages.

7. Acknowledgment

The authors thank the Australian Research Council (ARC) for the financial support of this project through the ARC Discovery Grant DP0774497.

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Figures:

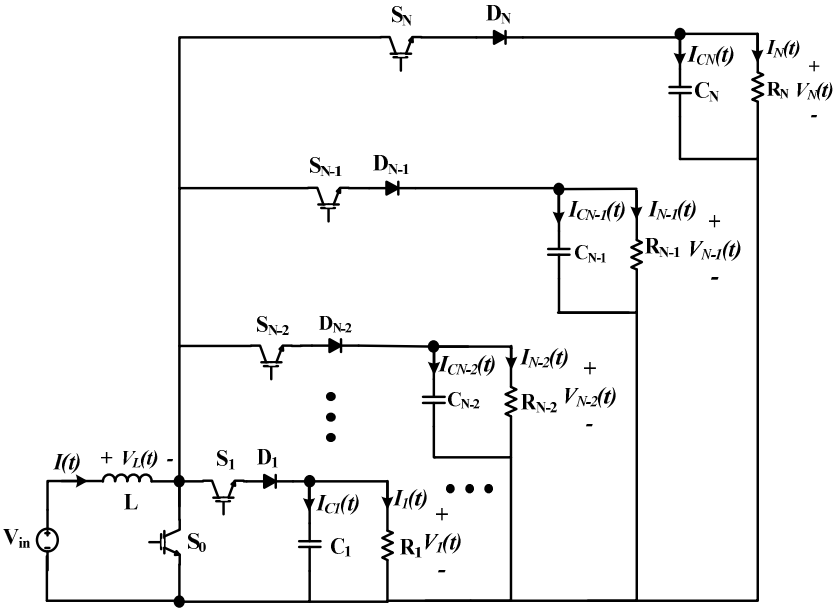


Fig.1. SIMO converter with independent loads

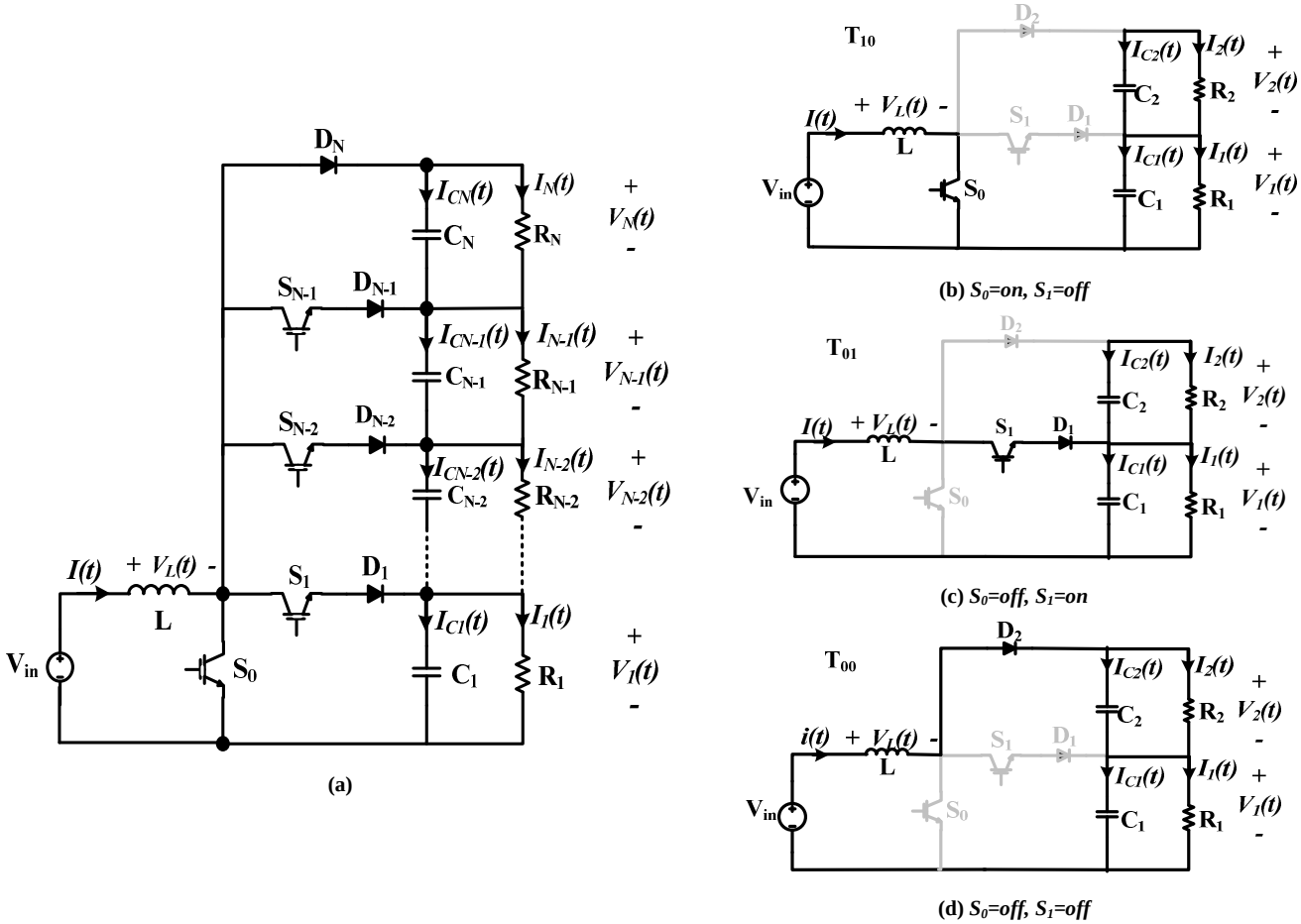


Fig.2. Configuration of MOB converter (a)schematic;(b)-(d) equivalent circuit in different switching intervals for double-output (N=2)

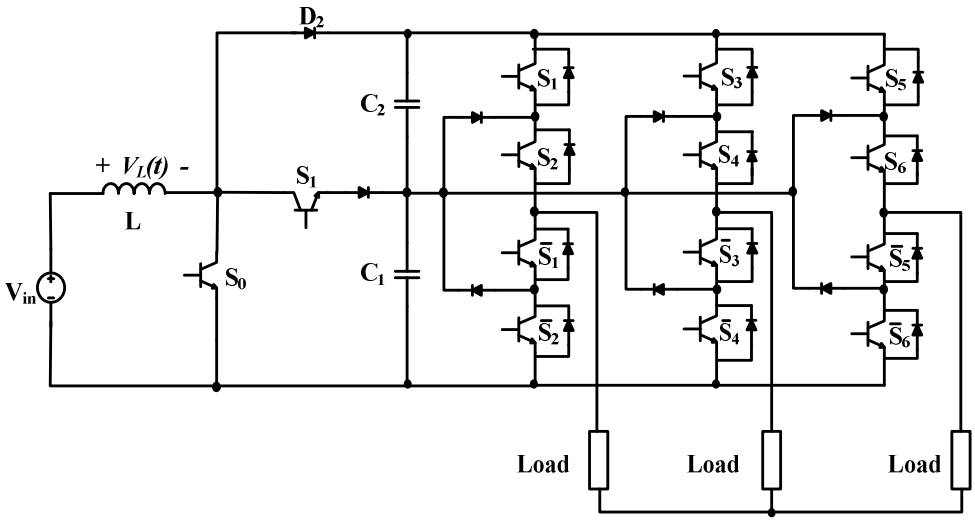


Fig.3. Three-level diode-clamped topology joint with double-output MOB converter

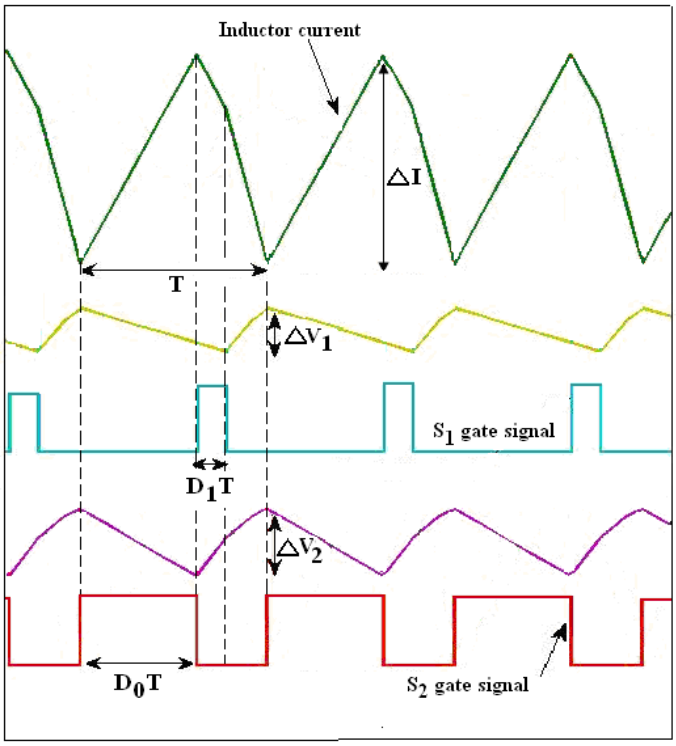


Fig.4. Inductor current and switching signals with corresponding output voltages during steady state operation in CCM

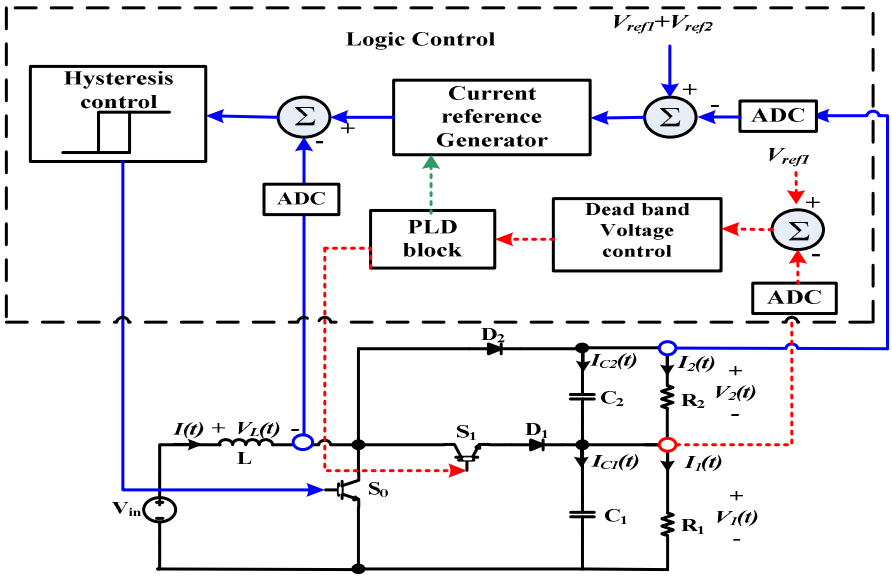
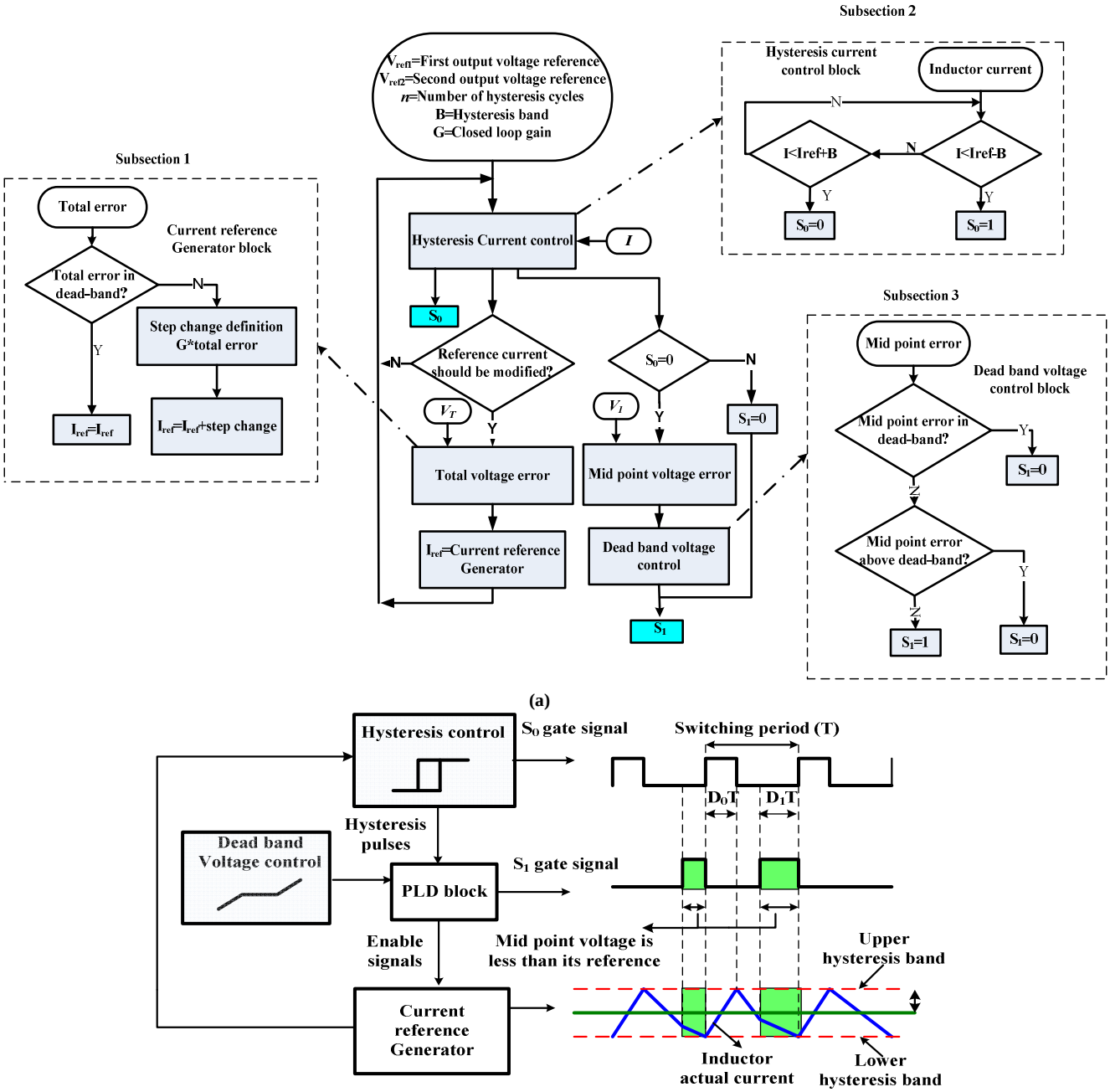


Fig.5. Block diagram of the proposed control system



(a)

(b)

Fig.6. (a) Flowchart of Control strategy for double-output MOB converter. (b) Switching pattern of S_0 and S_1 based on control strategy

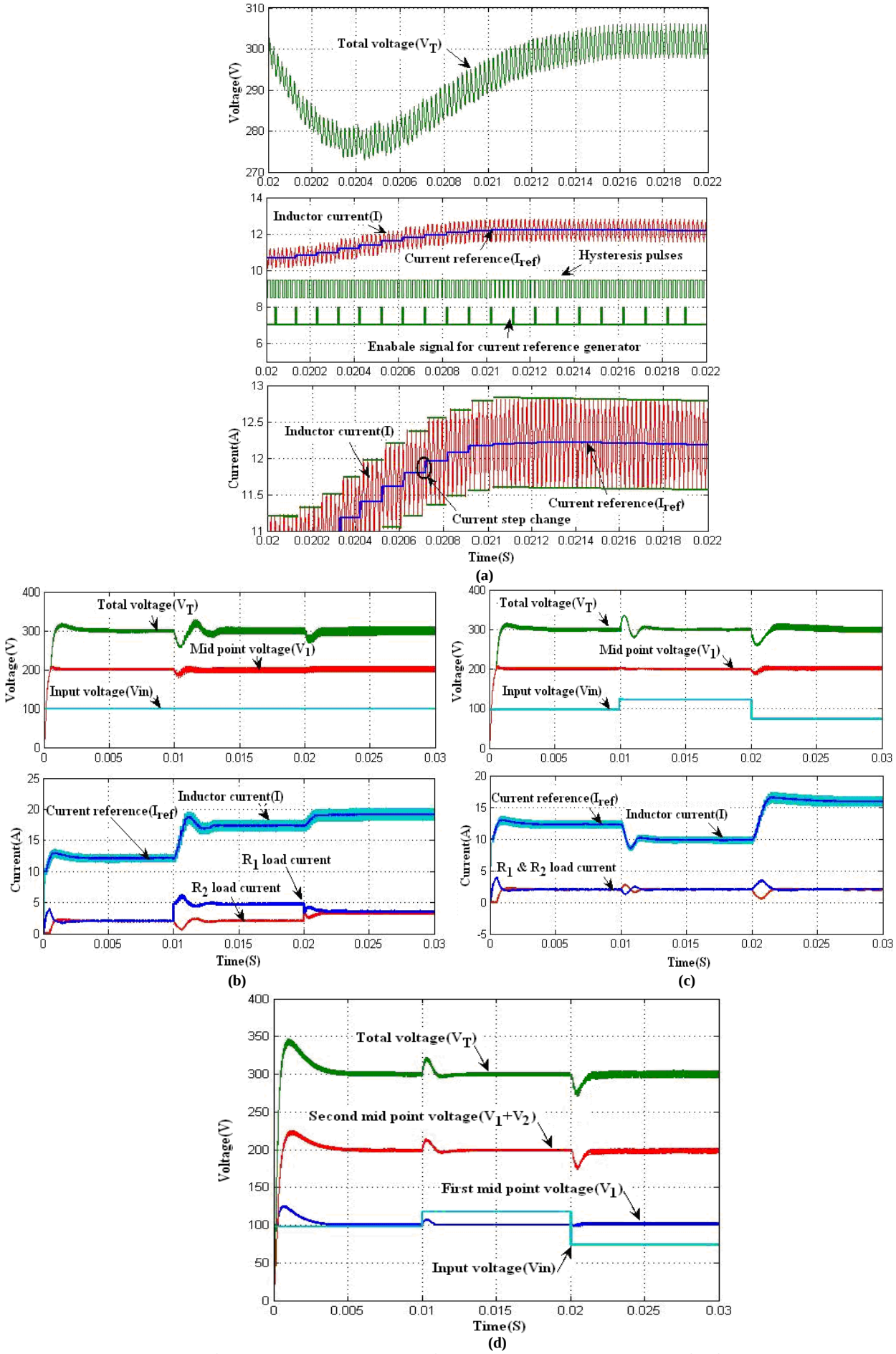


Fig.7. (a) Dynamic operation of controller to generate desired reference current (enable signals comes after five hysteresis cycle). (b) Dynamic response for load variation. R_1 and R_2 are changed from 50 Ω to 30 Ω at 0.01*s* and 0.02*s*, respectively. (c) Dynamic responses against of input voltage variation in double-output converter. (d) Dynamic responses against of input voltage variation in triple-output converter .Input voltage has change from 100 *V* to 125 *V* at *0.01s* and back to 75 *V* at 0.02*s*.

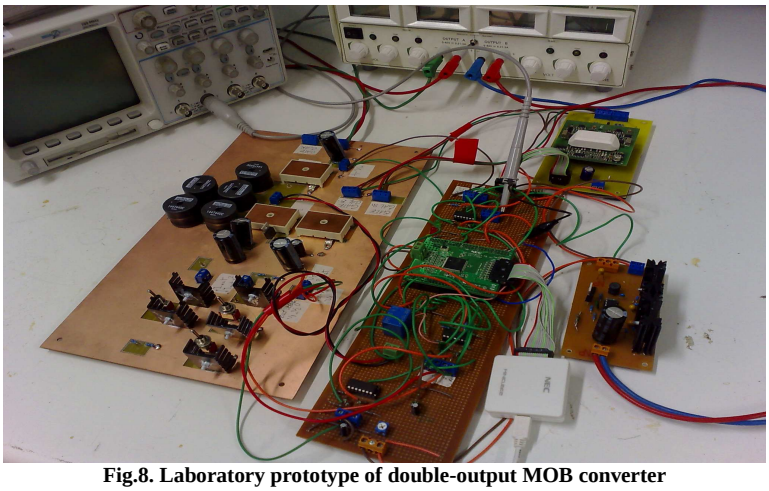
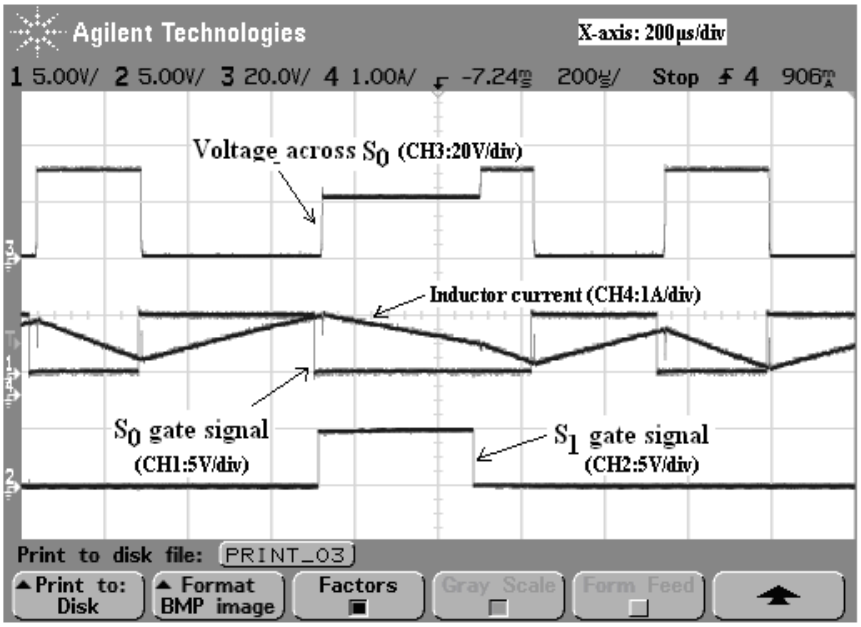
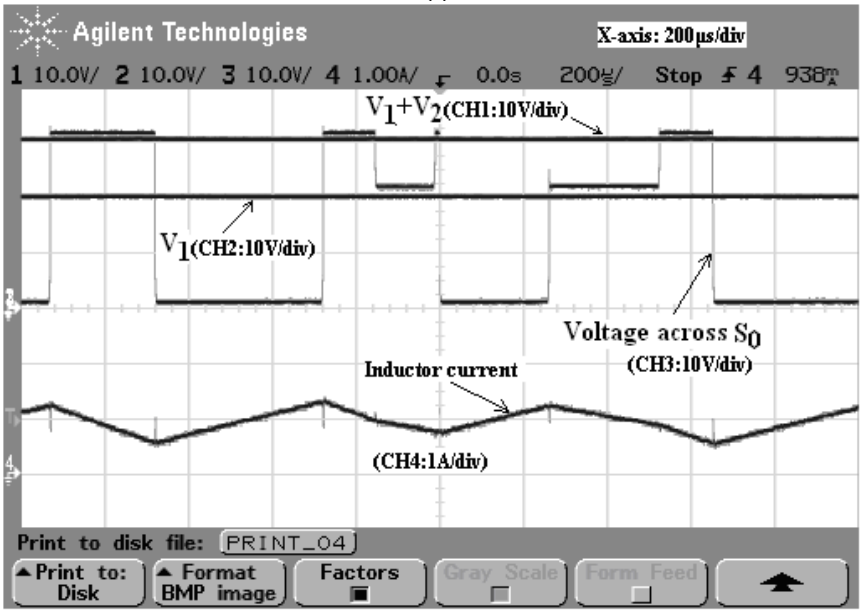


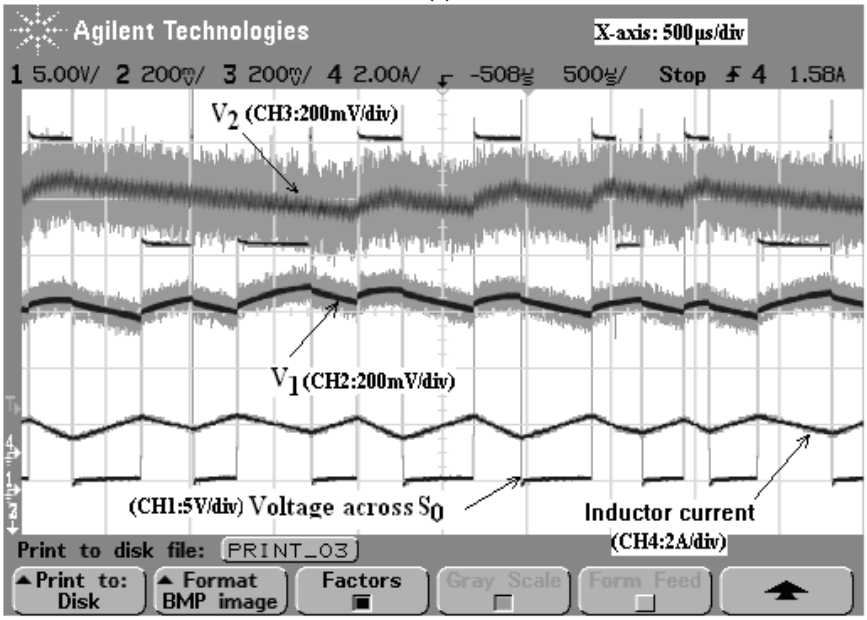
Fig.8. Laboratory prototype of double-output MOB converter



(a)

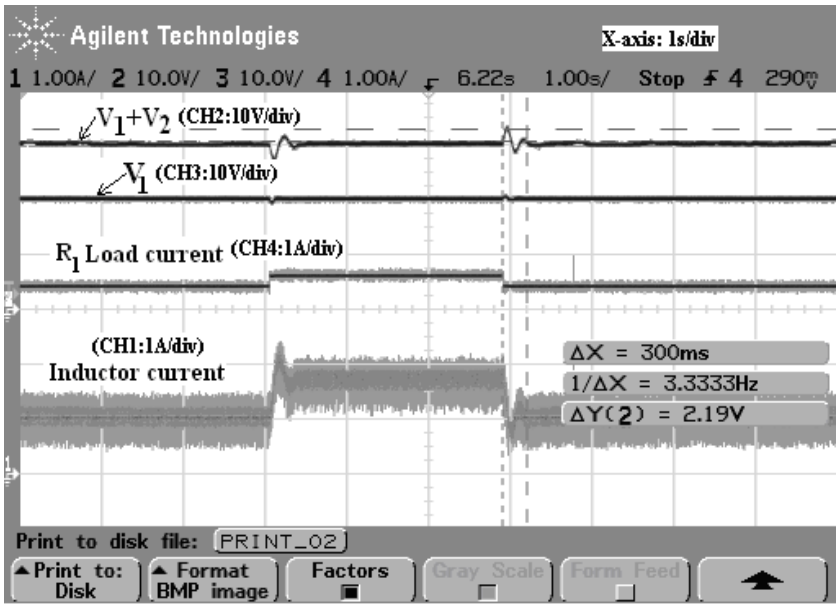


(b)

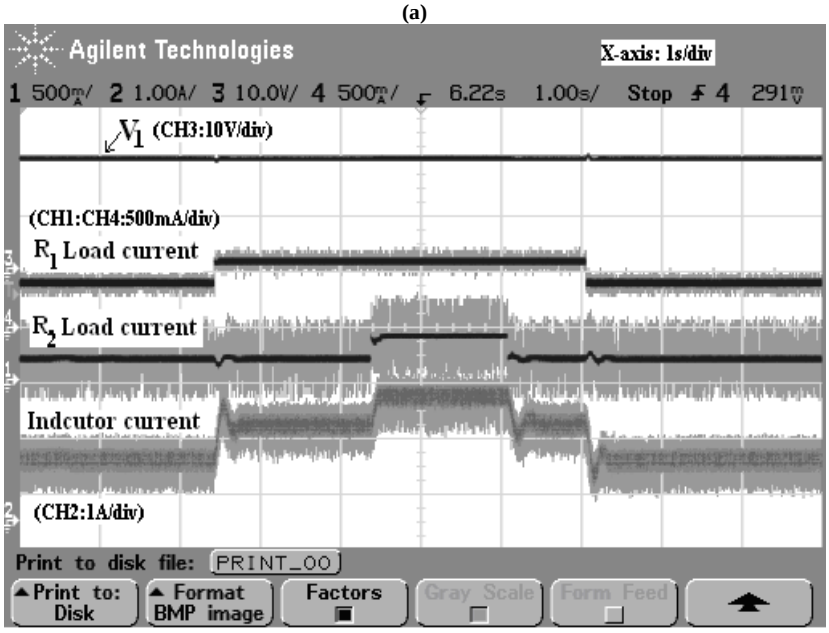


(c)

Fig.9. (a) Steady-state inductor current and switching pulses for the CCM operation (R_1 = 50 Ω and R_2=50 Ω). (b) Output voltages corresponding to (a). (c) Output voltages ripple regarding to switching states



(a)



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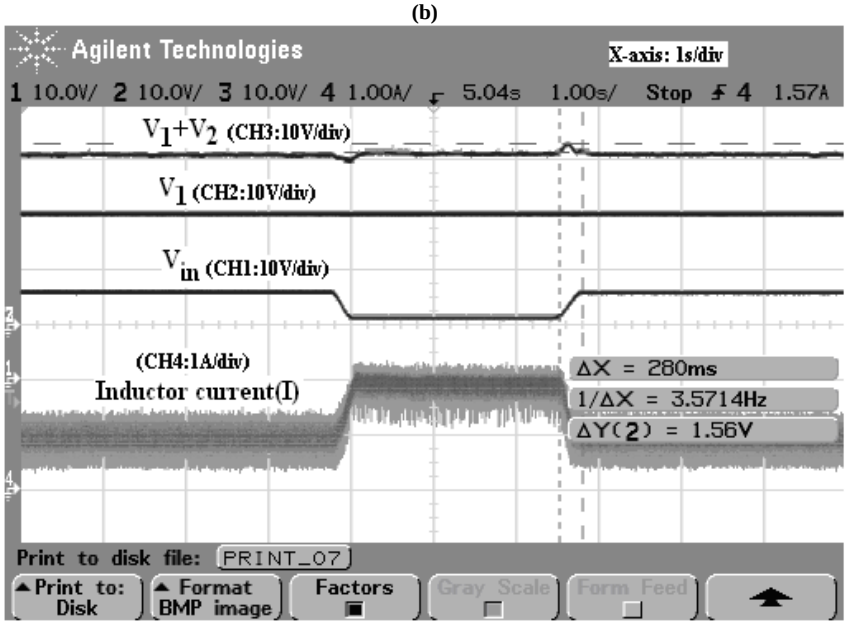

(c)

Fig.10. Waveforms during transient condition. (a)When R_1 *is* changed (b) When R_1 and R_2 *are* changed. (c) Output voltage during input voltage disturbance ***(R_1=R_2=50 Ω)*.**