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Multi-Port Multi-Cell DC/DC Converter Topology for Electric Vehicle's Power Distribution Networks

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***Abstract*—In today's electric vehicles (EV), power density is a key criterion for electrical systems, due to the strongly limited available space. Thereby, a high integration level of the electric distribution network is inevitable. In this paper, a novel multi-port multi-cell (MPMC) topology is proposed, which combines the features of two independent two-port converter systems, which are commonly used in state-of-the-art EVs. Consequently, this results in a higher overall power-density of the overall electric distribution system.**

The proposed converter comprises multiple identical sub-converters (cells), where each cell processes the same share of the total converter power. Furthermore, as will be shown in this paper, the multi-cell approach mitigates several technological design challenges arising in single-cell solutions, where, in contrast to the multi-port multi-cell approach, extremely high output currents and high step-down ratios are required. Finally, a MPMC control strategy is introduced, which guarantees stable operation and balanced cell powers in the converter for all operating points.

***Index Terms*—electric vehicle, battery charger, multi-cell, multi-port.**

I. Introduction

The continuously increasing emissions of carbon dioxide, combined with the finite fuel resources, intensified the search for alternative energy sources in the past decades. A reduction of fossil fuel combustion is inevitable to obtain a sustainable energy balance [1]. As the amount of environmental pollution caused by road transport substantially contributes to the global carbon emissions, the development of electric vehicles (EVs) increased in importance [2]. However, the limited storage capacity of today's EVs built-in LiIon batteries only enables confined electric ranges of the vehicles. For this reason, a comprehensive high-power charging infrastructure needs to be available to ensure suitability of daily use. Unfortunately, fast charging stations - typically supplied from the three-phase AC mains - are not yet widely accessible, slowing down the growth of the global EV market. In order to circumvent this limitation, an additional galvanically isolated medium-power single-phase on-board charger [3], consisting of an AC/DC PFC rectifier and a subsequent isolated HV-DC/DC converter, is installed in the EV, enabling the charging of the LiIon battery on the go, directly from the common single-phase AC mains (cf. **Fig. 1**).

Nevertheless, depending on the available infrastructure, the charging via high-power charging stations is usually preferred, due to its substantially reduced charging time compared to the one achievable with the additional single-phase charger. Consequently, from an economical point of view, the rare use of this auxiliary charging unit and the limited available space in EVs demand for extremely low costs and high power density of this system.

Besides the two battery chargers, an additional galvanically isolated DC/DC converter system is required, which feeds power from the high voltage (HV) DC-bus to the low voltage (LV) DC-bus (cf. **Fig. 1**). This LV bus supplies all the auxiliary electronics, as for example the board computer and automotive lights. Even though a small LV battery buffers this voltage bus, the main part of the required power needs to be delivered by the HV battery by means of the aforementioned DC/DC converter [4].

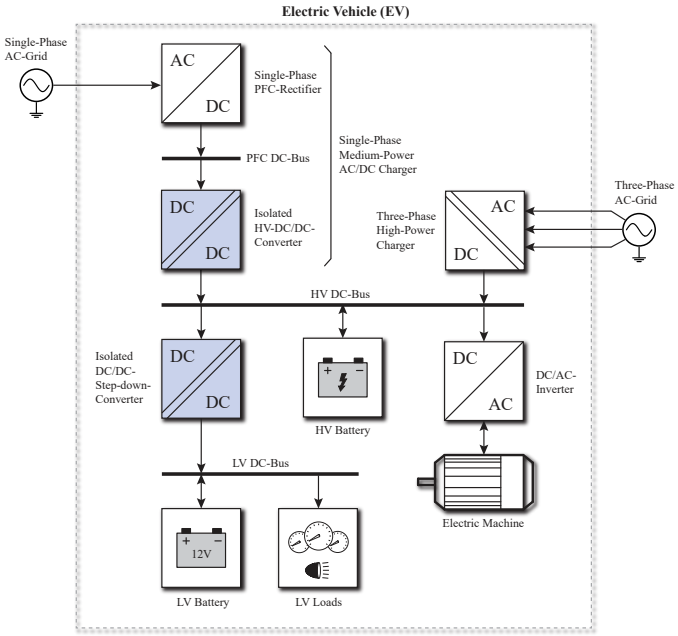

Fig. 1: Simplified block diagram of the electric distribution network in modern electric vehicles (EVs) with the two isolated DC/DC converter systems under consideration (blue-shaded).

As shown in **Fig. 1**, the entire electric distribution network comprises a large number of different converter systems [5]–[7], which are used to provide the required charging methods, the different voltage levels and the inevitable galvanic isolation between these voltage buses. This results in a complex, large and inefficient total power distribution system. In addition, certain parts of the system are only operated either during charging or in the drive mode, providing the possibility of integrating individual converter systems into a single converter unit, which then is operating in both, the charging and driving mode. For example, considering the two blue-shaded isolated DC/DC converter systems of **Fig. 1**, an integration of these two systems into a single galvanically isolated three-port DC/DC converter is possible, since in the charging mode only the isolated HV-DC/DC converter is operating while the isolated DC/DC step-down converter is idle, and in the driving mode the isolated step-down DC/DC converter is feeding power from the HV-bus to the LV-bus while the HV-DC/DC converter is unused.

As a result, the required total power capability of the new three-port isolated DC/DC converter is significantly lower compared to the one of the conventional two-stage solution. Assuming a $3.6\,\mathrm{kW}$ isolated single-phase AC/DC charger and a $3\,\mathrm{kW}$ isolated DC/DC step-down converter, which in total have a power capability of $6.6\,\mathrm{kW}$, the new three-port converter can provide the same required power distribution, with a total power capability of only $3.6\,\mathrm{kW}$. This yields a significant

improvement in terms of power density and manufacturing costs. To sum up, the new three-port isolated DC/DC converter needs to provide the following features:

- Bidirectional power flow capability at the HV bus port, since either power is fed into (charging mode) or drawn from (driving mode) the LiIon battery.
- Capability of handling large output currents in the LV bus (up to 200 A).

Besides these topological constraints, **Table I** lists the main electrical specifications for the proposed three-port isolated DC/DC converter system.

A versatile and very efficient topology, complying with the given requirements, can be found in [8] and [10], using a three-port version of a dual-active-bridge (DAB) converter [9], and therefore hereinafter is referred as triple-active-bridge (TAB) converter (cf. **Fig. 2**). The TAB converter features bi-directional power flow capability in each port, and the possible buck/boost operation allows for arbitrary power distributions independent of the actual port voltages. In **Section II**, this topology is shortly revisited in terms of converter operation and power flow control. Afterwards, the occurring design challenges for the TAB converter with the given specifications are discussed, which lead to the novel multi-port multi-cell (MPMC) converter presented in **Section III**. Compared to the TAB converter, the proposed MPMC topology facilitates the converter design, and allows to connect multiple voltage buses with high voltage ratios and large output currents in an efficient way. Subsequently, the control scheme of the MPMC converter is discussed and verified by simulation in **Section IV**. Finally, **Section V** concludes the findings of this paper.

II. Three-Port DC/DC Converter

In the three-port triple-active-bridge (TAB) DC/DC converter [10], the full-bridges of each DC port are magnetically coupled through a single three-winding transformer, whose electric behaviour can be modelled by the three leakage inductances $L_{\sigma\mathrm{PFC}}$, $L_{\sigma\mathrm{HV}}$ and $L_{\sigma\mathrm{LV}}$ and the magnetizing inductance L_m (cf. **Fig. 2**). Each full-bridge generates one of the three rectangular voltage waveforms v_PFC, v_HV or v_LV, which is directly applied to the corresponding winding. In the following, the indices A, B and C are used for the PFC, HV and LV port, respectively. Consequently, the power transfer between the three ports can be controlled by adjusting the three duty cycles $D_\mathrm{A}, D_\mathrm{B}, D_\mathrm{C}$ as well as two of the three phase shifts $\varphi_\mathrm{AB}, \varphi_\mathrm{AC}, \varphi_\mathrm{BC}$ between the three rectangular voltage waveforms. The simplified equivalent circuit of the TAB is shown in **Fig. 3**, whereby the magnetizing inductance L_m usually can be neglected for the switching cycle analysis, due to its much higher impedance compared to the one of the three leakage inductances $L_{\sigma\mathrm{A,B,C}}$. Furthermore, since all components are transformed to the side of port A in order to eliminate the galvanic isolation, the transformer turns ratios n_AB and n_AC have to be considered for v_B and v_C. As a result, the power flow and the current waveforms in a TAB depend on the port voltages $v_\mathrm{A,B,C}$, the leakage inductances $L_{\sigma\mathrm{A,B,C}}$, the switching frequency f_s and the five control parameters D_A, D_B, D_C, φ_AB and φ_AC, as exemplarily shown in **Fig. 3**. Based on a first harmonic approximation [10], the powers P_A, P_B and P_C supplied from each port into the transformer can be calculated according to

$$P_\mathrm{A} = g(\mathrm{A},\mathrm{B},\varphi_\mathrm{AB}) + g(\mathrm{A},\mathrm{C},\varphi_\mathrm{AC}) \quad (1)$$

$$P_\mathrm{B} = g(\mathrm{A},\mathrm{B},-\varphi_\mathrm{AB}) + g(\mathrm{B},\mathrm{C},\varphi_\mathrm{AC}-\varphi_\mathrm{AB}) \quad (2)$$

$$P_\mathrm{C} = g(\mathrm{A},\mathrm{C},\varphi_\mathrm{AB}) + g(\mathrm{B},\mathrm{C},\varphi_\mathrm{AB}-\varphi_\mathrm{AC}), \quad (3)$$

TABLE I: Main electrical specifications for the investigated isolated three-port DC/DC converter system.

	PFC DC-Bus	HV DC-Bus	LV DC-Bus
Voltage Range	500 V	250...500 V	10.5...15 V
Maximum Current	7.2 A	12 A	200 A
Maximum Power	3.6 kW	3.6 kW	3 kW

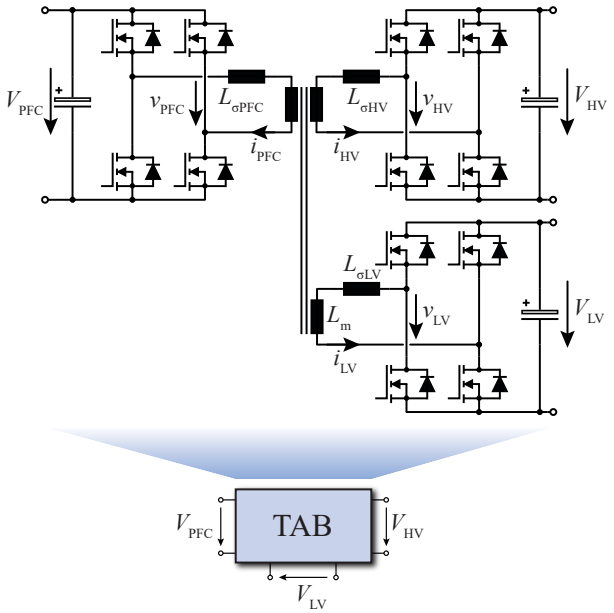

Fig. 2: Galvanically isolated three-port triple-active-bridge (TAB) DC/DC converter stage for omnidirectional power transfer and its substitute image (blue-shaded).

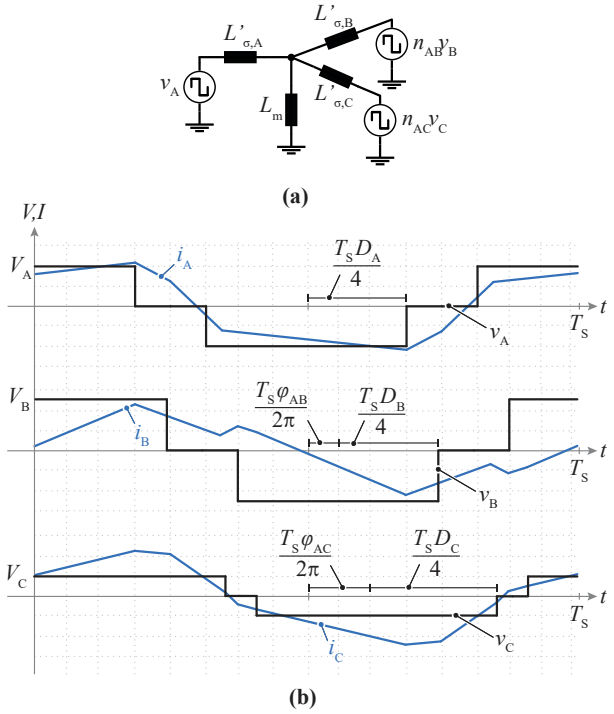

Fig. 3: **(a)** Equivalent circuit of a triple-active-bridge (TAB) converter and **(b)** corresponding voltage and current waveforms.

where

$$g(\mathrm{X},\mathrm{Y},\varphi_{\mathrm{XY}}) = \frac{4V_{\mathrm{X}}V_{\mathrm{Y}}}{\pi^3 f_s L}\sin\left(\frac{\pi}{2}D_{\mathrm{X}}\right)\sin\left(\frac{\pi}{2}D_{\mathrm{Y}}\right)\sin(\varphi_{\mathrm{XY}}), \quad (4)$$

and $X, Y \in \{A, B, C\}$.
Furthermore, assuming a lossless transformer, the average power injected into the transformer has to be zero. Hence, the following condition holds true

$$P_{\mathrm{A}} + P_{\mathrm{B}} + P_{\mathrm{C}} = 0. \quad (5)$$

Consequently, only the power of two ports can be chosen independently. Based on (1)-(3), however, the power levels $P_{\mathrm{A}}, P_{\mathrm{B}}$ and P_{C} are controlled with five control parameters, thus the system is under-determined and multiple sets of control parameters lead to the exactly same power distribution, even though the current waveforms are different. The optimal parameter set, however, can be found by means of numerical optimization, where also the zero-voltage-switching operation (switching losses) and the RMS currents (conduction losses) have to be considered.
The controller finally retrieves the most suitable parameter set for the given voltages $V_{\mathrm{A,B,C}}$ and the power levels $P_{\mathrm{A,B,C}}$ from a lookup table (LUT), which was created in advance by the aforementioned numerical optimization.

Even though this control strategy allows for soft switching operation of the converter, the large output currents in the LV-port together with the relatively small output capacitance of the switching devices result in very short commutation intervals t_{S} (cf. **Fig. 4**). Consequently, this leads to extremely high $\frac{\mathrm{d}i}{\mathrm{d}t}$ values and, according to

$$v_{\mathrm{S}} = \frac{L_{\mathrm{S}} I_{\mathrm{out,X}}}{t_{\mathrm{S}}}, \quad (6)$$

large voltages v_{S} across the parasitic inductances L_{S} in the commutation loop are induced (cf. **Fig. 4(a)**). In practical applications, v_{S} should be limited to a certain fraction α of the port voltage $V_{\mathrm{out,X}}$, to allow for using semiconductors with lower breakdown voltages and therefore beneficial $R_{\mathrm{DS,on}}$ properties. The maximum allowed over-voltage $\alpha V_{\mathrm{out,X}}$ and the characteristic impedance $Z_{\mathrm{out,X}}$ of the converter port, directly define the maximum allowable parasitic inductance in the commutation loop according to

$$L_{\mathrm{S}} \leq t_{\mathrm{S}} \alpha Z_{\mathrm{out,X}} \qquad Z_{\mathrm{out,X}} = \frac{V_{\mathrm{out,X}}}{I_{\mathrm{out,X}}}. \quad (7)$$

This limitation of L_{S} is illustrated in **Fig. 4(b)** for different commutation intervals t_{S} and a maximum allowed voltage overshoot of $\alpha = 10\,\%$.
In the application at hand, the characteristic impedance of the LV-port with a value of only $Z_{\mathrm{out,LV}} = 52\,\mathrm{m\Omega}$ is extremely small. Based on **Fig. 4(b)**, this would definitely demand a power loop inductance below $1\,\mathrm{nH}$, which is hardly achievable in a real circuit design, due to the inevitable parasitic inductances of the semiconductor packages, the DC link capacitor and the PCB tracks. For this reason, a significant over-voltage has to be expected. As a consequence, the employment of MOSFETs with high breakdown voltages and therefore higher $R_{\mathrm{DS,on}}$ per chip area is unavoidable, resulting in either substantial conduction losses or a large total required silicon area A_{Si}.

In contrast to the characteristic impedance $Z_{\mathrm{out,LV}}$ of the LV-port, the characteristic impedances of the two remaining ports (HV and PFC) are relatively high, as both ports are connected to high voltages

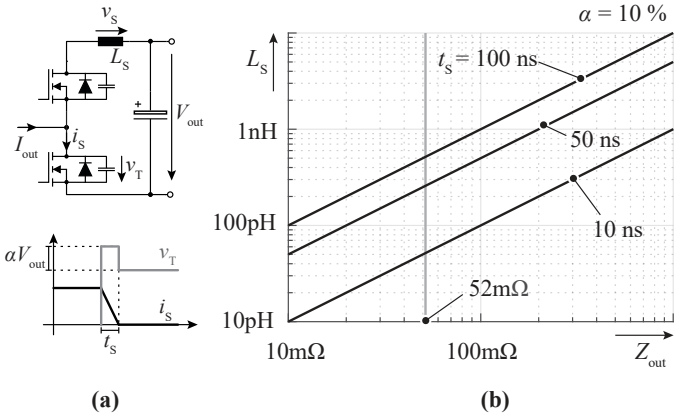

Fig. 4: **(a)** Schematic of a half bridge circuit with the considered parasitic power loop inductance L_{s}, and the corresponding voltage v_{T} and current waveform i_{s} during a switching transition. **(b)** Maximum allowed parasitic power loop inductance L_{s} for a certain output impedance $Z_{\mathrm{out,LV}}$, switching time t_{s} and a maximum allowed voltage overshoot α of $10\,\%$ [11].

and carry a comparably low current. Even though a high characteristic impedance is beneficial regarding over-voltage issues, during the switching transients in soft-switching applications, a large current is required in order to charge and discharge the MOSFET's parasitic output capacitances C_{oss} within a reasonably short time interval t_{S}

$$Q_{\mathrm{oss}} = C_{\mathrm{oss}} \cdot V_{\mathrm{DS}} \rightarrow t_{\mathrm{S}} = \frac{C_{\mathrm{oss}} \cdot V_{\mathrm{DS}}}{I_{\mathrm{out}}} = C_{\mathrm{oss}} \cdot Z_{\mathrm{out}}. \quad (8)$$

As can be noticed, the duration of the soft-switching transition t_{S} is proportional to Z_{out}, which means that for high voltage ports with high characteristic impedances a large amount of the port current is only needed to achieve soft-switching, resulting in a substantial amount of reactive power flow in the converter. Consequently, soft-switching operation in a converter port with a high characteristic impedance can only be achieved at the expense of significantly increased conduction losses.

Besides these disadvantages, for the isolated TAB converter, also the combination of low and high characteristic output impedances Z_{out} implies an additional converter performance limitation in terms of transformer design. The huge difference between the port voltages demands for a high turns-ratio in the transformer, and therefore limits the HV windings to a large minimum number of turns, even though the LV-winding is realized with a single turn. This limitation yields sub-optimal transformer designs with either high conduction losses or low power density.
Therefore, in the following section, a novel multi-port multi-cell (MPMC) topology is introduced, which can be used to overcome the aforementioned drawbacks of the single-cell TAB converter.

III. Multi-Port Multi-Cell Converter

The proposed multi-port multi-cell (MPMC) converter structure is shown in **Fig. 5**. It comprises n identical TAB cells (blue-shaded), whose ports are all connected either in series or in parallel, depending on the level of the applied bus voltage. Hence, the ports connected to the high voltage buses V_{PFC} and V_{HV} are connected in series, while the low voltage ports are connected in parallel.
The series connection of multiple TAB-cells equally distributes the bus voltage between the cell-internal HV-ports, which means that the characteristic impedances of the cell-internal HV-ports are

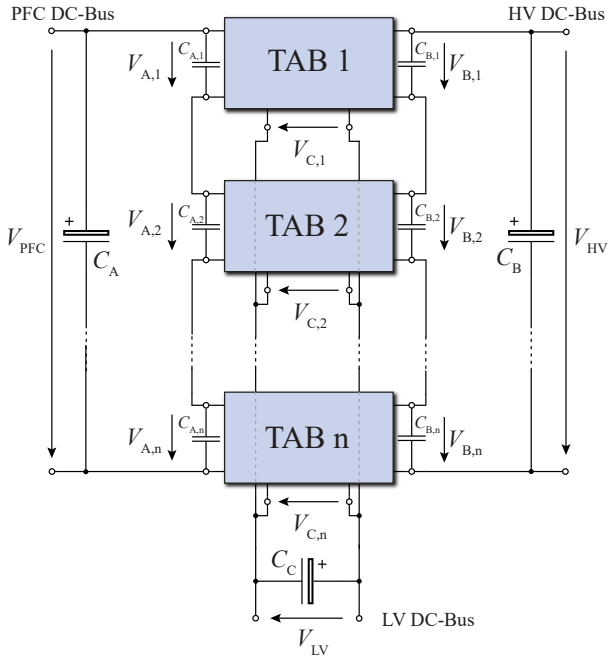

Fig. 5: Structure of the proposed multi-port multi-cell (MPMC) converter system with n identical TAB cells.

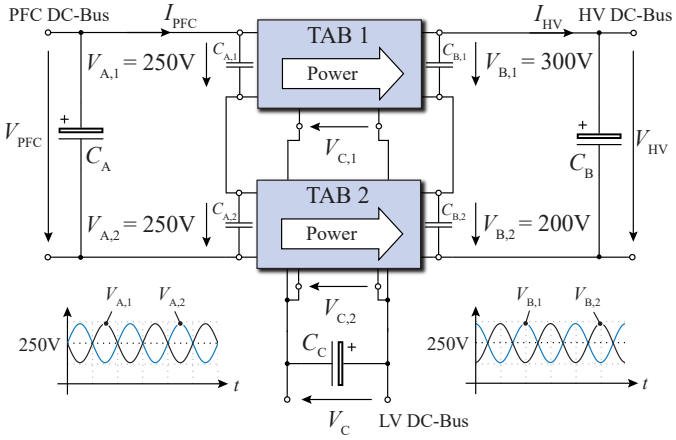

Fig. 6: Example of an asymmetric port voltage distribution in a three-port two-cell converter with the port voltage oscillations induced by a common duty cycle control.

reduced. Accordingly, soft-switching operation can be achieved with a much lower commutation current, providing reduced conduction losses in the converter. In addition, the required breakdown voltage of the switching devices can be reduced, which offers the possibility of using alternative semiconductor technologies with beneficial properties regarding conduction and switching losses (figure-of-merit).

Furthermore, the series connection of multiple TAB-cells at the HV ports reduces the cell-internal port voltage ratios by a factor of n, which means that with the number of cells n a further degree of freedom is introduced. For this reason, the design space of the transformer is considerably enlarged, which can result in transformer designs with higher efficiency and/or power density.

Similarly, the parallel connection of multiple ports enables an equal distribution of the LV output current between the cell-internal LV-ports, thus their characteristic impedance is increased, and the commutation loop related over-voltage can be substantially reduced. Accordingly, semiconductors with low breakdown voltages and therefore beneficial $R_{\mathrm{DS,on}}$ values can be used again.

Furthermore, in order to reduce the current ripple in the DC link capacitors $C_{\mathrm{A,B,C}}$, the TAB-cells can be operated in an interleaved fashion by phase shifting the switching cycles of the individual TAB-cells by $\varphi_{\mathrm{cell}} = \frac{2\pi}{n}$, which results in an effective switching frequency of nf_{s}. This also reduces the required DC link capacitance for a certain allowed voltage ripple and lowers the volume of these components.

The proposed multi-cell approach for multi-port converter systems has already been investigated for two-port converter systems in telecom applications, where, due to the aforementioned benefits, a significant improvement in terms of efficiency and power density was achieved [12]. However, while for two-port converter systems, e.g. in input-series output-parallel (ISOP) configuration, natural voltage and current balancing is guaranteed, for three-port converter systems, the voltage and current sharing need to be actively controlled. Therefore, in the following subsection, a new control strategy to guarantee equal power distribution in multi-cell multi-port converters is presented.

A. MPMC Converter Control

Due to the natural voltage and current balancing of two-port converter systems e.g. with ISOP structure, a simple modulation scheme with common duty cycles and phase shifts for all individual converter cells can be applied [12]. The advantage of this control strategy is the minimization of the complexity and computation effort of the control, as a single controller can be used to calculate the common control parameter set D_{A}, D_{B}, D_{C}, φ_{AB} and φ_{AC} for all converter cells. Hence, each cell is controlled with the same gate drive signals, whereby a cell-internal control can be omitted and the controller hardware and software effort is reduced to the same amount as required in a single-cell converter. Unfortunately, this natural balancing is lost in multi-port ($n > 2$) systems, as it is exemplarily shown in **Fig. 6** for a three-port two-cell converter system. Initially, it is assumed that the port voltages $V_{\mathrm{B,1}}$ and $V_{\mathrm{B,2}}$ are not balanced and that a certain power P_{B} is supplied from the PFC DC-bus to the HV DC-bus.

For example, after a load step, such an asymmetric voltage distribution is a likely scenario. Due to component tolerances and aging effects, in a real system, typically the capacitance values of the cell internal capacitors $C_{\mathrm{A,k}}$ and $C_{\mathrm{B,k}}$ are different and therefore result in a series connection of dissimilar capacitances in the PFC and HV converter ports. Consequently, during a load step at e.g. the HV DC-bus, the cell-internal capacitors $C_{\mathrm{B,1}}$, $C_{\mathrm{B,2}}$ to $C_{\mathrm{B,n}}$ are discharged by the same load current, which in case of unequal capacitance values leads to different voltage drops across the cell-internal capacitors and therefore to an asymmetric voltage distribution.

Applying now the aforementioned common duty cycle/phase shift control modulation scheme to the example of the three-port two-cell converter system shown in **Fig. 6**, this results in a further destabilization of the port voltages, as the cell-internal port powers $P_{\mathrm{B,1}}$ and $P_{\mathrm{B,2}}$ are directly proportional to the momentary port voltages $V_{\mathrm{B,1}}$ and $V_{\mathrm{B,2}}$ according to (2) and (4). Consequently, the higher port voltage $V_{\mathrm{B,1}}$ leads to a larger cell-internal power $P_{\mathrm{B,1}}$, whereas the lower port voltage $V_{\mathrm{B,2}}$ yields a smaller cell-internal power $P_{\mathrm{B,2}}$. This difference between the cell-internal port power values $P_{\mathrm{B,1}}$ and

$P_{B,2}$ in turn also causes an asymmetry in the port voltages $V_{A,1}$ and $V_{A,2}$ due to the unequal power demand from the two cell converters TAB 1 and TAB 2, which finally result in a hardly damped port voltage oscillation between port A and port B according to **Fig. 6**. Consequently, in order to avoid unbalanced voltage distributions and unequal power sharing among the converter cells, an individual control of each cell is inevitable in MPMC converter systems. Ideally, due to the arising conduction losses, the total converter power should be equally distributed among the converter cells. However, as will be shown in **Section IV**, an equal distribution of the aforementioned converter power among the individual converter cells cannot balance out asymmetries in the voltage distribution and consequently leads again to an unstable converter operation. For this reason, a more sophisticated controller needs to be employed.

In the following, the structure of a suitable MPMC controller is presented, which guarantees the appropriate power distribution P_A, P_B and P_C between the three DC buses, while at the same time the port voltages can be balanced for all operating points. Thereby, the set-points $P_{A,set}$, $P_{B,set}$ and $P_{C,set}$ of the aforementioned power distribution P_A, P_B and P_C are calculated by a superordinate battery charge controller and forwarded as reference values to the central MPMC master controller, which is the main focus of this subsection. Based on the actual cell-internal port voltages $V_{A,k}$ and $V_{B,k}$, $k \in \{1,..,n\}$, and the given power set-points $P_{A,k,set}$, $P_{B,k,set}$ and $P_{C,k,set}$, the central MPMC master controller then calculates the cell-dependent power set-points $P_{A,k,set}$, $P_{B,k,set}$ and $P_{C,k,set}$, $k \in \{1,..,n\}$ in such a way that a symmetric voltage distribution among the individual converter cells is achieved (cf. **Fig. 7**).

Afterwards, these cell-dependent power set-points $P_{A,k,set}$, $P_{B,k,set}$ and $P_{C,k,set}$ are forwarded to the cell-internal controllers of the individual TAB cells, which then calculate the appropriate duty cycles $D_{A,k}$, $D_{B,k}$, $D_{C,k}$ and phase shifts $\varphi_{AB,k}$ and $\varphi_{AC,k}$, according to **Section II**, in order to process the demanded power values $P_{A,k}$, $P_{B,k}$ and $P_{C,k}$. Hence, each converter cell operates as an individual TAB converter, whose reference values $P_{A,k,set}$, $P_{B,k,set}$ and $P_{C,k,set}$ are given by the central MPMC master controller.

Thereby, actually only two of the three set-point values $P_{A,k,set}$, $P_{B,k,set}$ and $P_{C,k,set}$ have to be provided by the central MPMC master controller, since the third power set-point can be calculated based on (5). Furthermore, in the proposed MPMC topology only the series connected ports A_k and B_k can lead to unbalanced voltage distributions among the cell converter ports, hence, only the power values of these two ports need to be actively controlled. However, in order to be able to redistribute power between series connected ports, in the proposed MPMC topology at least one parallel port is needed, because a direct power transfer between series connected ports, e.g. from port B_1 to B_2, as would be desired for the example in **Fig. 6**, is not possible. In this case, for example, TAB 1 would have to transfer the excess energy stored in $C_{B,1}$ to the parallel port C, while TAB 2 retrieves the needed amount of energy from port C to recharge the capacitor $C_{B,2}$. Hence, in addition to providing the required port power P_C, the parallel connected port is also used to compensate for possible voltage asymmetries in the power distributions of the series connected converter ports A_k and B_k.

For the calculation of the cell-dependent power set-points $P_{A,k,set}$ and $P_{B,k,set}$, the proposed MPMC master controller uses a two-step approach, where in a first step, the required power levels $P_{A,B,C}$ are equally distributed among the individual converter cells, and in a second step, parts of these cell-internal powers are redistributed between the different cells to achieve the required voltage balancing without affecting the total converter output power values $P_{A,B,C}$. In the following, both calculation steps are explained in more detail. For the sake of clarity, since the set-points $P_{A,k,set}$ and $P_{B,k,set}$ of both series connected ports A and B are calculated in the same manner, in the following description only the nomenclature for port A is used.

1) Common Power Share: In a first step, the central MPMC master controller equally distributes the received power set-point $P_{A,set}$ among the converter cells by dividing the total power $P_{A,set}$ by the number of converter cells n according to **Fig. 7(a)**. Thus, the MPMC controller assigns the same nominal port power $P_{A,nom} = \frac{P_{A,set}}{n}$ to each cell-port A_k. Therefore, this common power distribution strategy guarantees that the power requirement $P_{A,set}$ is met, as

$$\sum_{k=1}^{n} P_{A,k,set} = \sum_{k=1}^{n} P_{A,nom} = P_{A,set}. \tag{9}$$

As already mentioned, in order to be able to balance the individual cell converter's port voltages $V_{A,k}$, a part of the common power share $P_{A,nom}$ has to be redistributed among the different cells, which means that each individual port power $P_{A,k,set}$ is modified by a certain voltage balancing power share $P_{A,k,diff}$.

$$\sum_{k=1}^{n} P_{A,k,set} = \sum_{k=1}^{n} P_{A,nom} + P_{A,k,diff} = \underbrace{\sum_{k=1}^{n} P_{A,nom}}_{=!P_{A,set}} + \underbrace{\sum_{k=1}^{n} P_{A,k,diff}}_{=!0} \tag{10}$$

Consequently, based on (9) and (10), the sum of the power shares $P_{A,k,diff}$, used for the voltage balancing, has to be zero such that the total converter power value $P_{A,set}$ is not affected. The detailed calculation method of the individual power shares $P_{A,k,diff}$ is explained in the following.

2) Voltage Balancing Power Share: The objective of the voltage balancing power share $P_{A,k,diff}$ is to balance all port voltages $V_{A,k}$ to the same voltage level. Therefore, the reference voltage $V_{A,nom}$ corresponds to the average of the port voltages $V_{A,k}$ and can be calculated based on the sum of the port voltages divided by the number of individual converter cells n according to

$$V_{A,nom} = \sum_{k=1}^{n} \frac{V_{A,k}}{n}. \tag{11}$$

and as shown in **Fig. 7**. For the balancing of the port voltages this basically means that for a too high port voltage $V_{A,k}$ the corresponding DC link capacitor $C_{A,k}$ has to be discharged by a certain current $I_{A,k,cap}$, or in other words, that a certain power $P_{A,k,diff} = I_{A,k,cap} \cdot V_{A,nom}$ has to be extracted from this capacitor. On the other hand, for a too low port voltage $V_{A,k}$, the DC link capacitor needs to be charged by a certain current $I_{A,k,cap}$, or again by analogy, a certain power $P_{A,k,diff} = I_{A,k,cap} \cdot V_{A,nom}$ has to be delivered to this capacitor. Hence, according to a conventional voltage controller, the charging/discharging current $I_{A,k,cap}$ can be determined by means of a proportional controller, which scales the difference between the reference voltage $V_{A,nom}$ and the actual port voltage $V_{A,k}$ by a proportional gain K_P (cf. **Fig. 7**). Finally, the power share $P_{A,k,diff}$, which basically corresponds to the momentary power flowing into or out of the capacitor, can be calculated by multiplying the charging/discharging current $I_{A,k,cap}$ with the reference voltage $V_{A,nom}$ (cf. **Fig. 7**) according to

$$P_{A,k,diff} = \frac{V_A}{n} \cdot I_{A,k,cap} = \frac{V_A}{n} \cdot K_P \cdot \left(\frac{V_A}{n} - V_{A,k} \right). \tag{12}$$

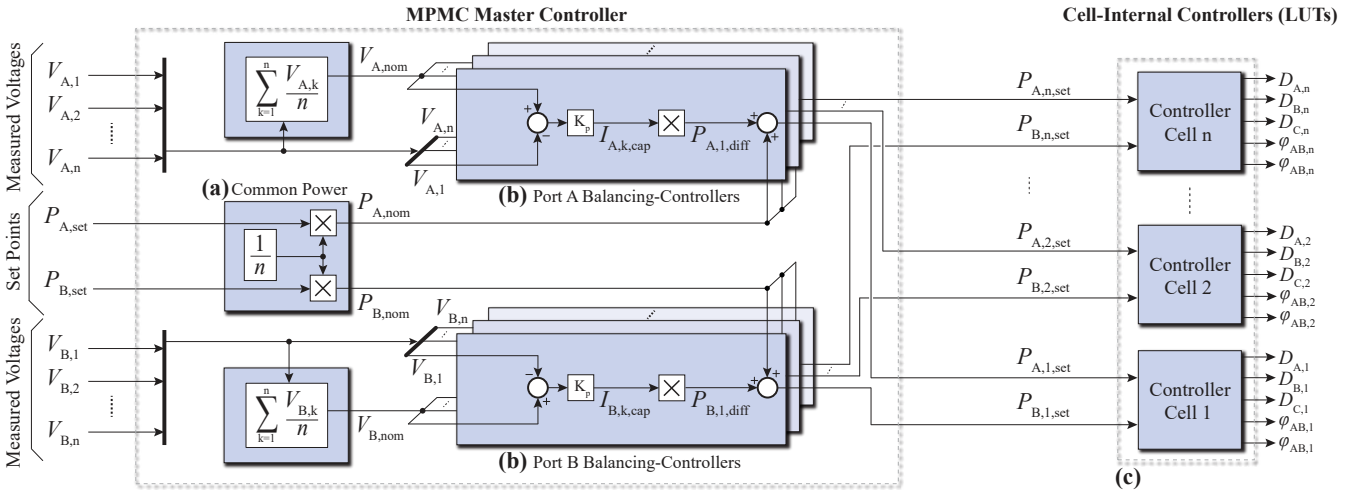

Fig. 7: Complete control scheme of the MPMC converter, comprising the different sub-controllers and the cell-internal look-up-tables (LUTs).

It is important to note, that based on (12) the sum of all voltage balancing power shares $P_{\mathrm{A,k,diff}}$ equals zero

$$\sum_{k=1}^{n} P_{\mathrm{A,k,diff}} = \frac{V_{\mathrm{A}} K_{\mathrm{P}}}{n} \left(\underbrace{\sum_{k=1}^{n} \frac{V_{\mathrm{A}}}{n}}_{=V_{\mathrm{A}}} - \underbrace{\sum_{k=1}^{n} V_{\mathrm{A,k}}}_{=V_{\mathrm{A}}} \right) = 0 \qquad (13)$$

and therefore the condition of (10) is always fulfilled. Consequently, the redistribution of the power shares $P_{\mathrm{A,k,diff}}$ does not affect the total power P_{A}.

For the sake of completeness, instead of a P-controller with a proportional gain K_{P}, a PI-controller could be used for the voltage controller. However, in this case, (10) would not be fulfilled anymore at any point in time, which means that e.g. during load transients, the momentary total power P_{A} does not coincide with the power set-point $P_{\mathrm{A,set}}$ given from e.g. the superordinate battery charge controller.

In a last step, the different power shares $P_{\mathrm{A,nom}}$ and $P_{\mathrm{A,k,diff}}$ are added up, resulting in the cell-dependent power set-points $P_{\mathrm{A,k,set}}$ as shown in **Fig. 7**.

As mentioned in the beginning, exactly the same calculation method is applied to the cell ports $\mathrm{B_k}$ in order to calculate their respective power set-points $P_{\mathrm{B,k,set}}$. Finally, the set-points $P_{\mathrm{A,k,set}}$ and $P_{\mathrm{B,k,set}}$ are forwarded to the cell-internal TAB controllers, which for their part calculate the optimal duty-cycles $D_{\mathrm{A,B,C}}$ and phase shifts φ_{AB} and φ_{AC} according to **Fig. 7(c)** and **Section II**.

The following section verifies the operating principle of the proposed MPMC controller by means of simulations, and points out the necessity of a voltage balancing controller in this type of converter.

IV. MPMC Simulation

In order to prove the proposed control concept and to show the performance of the MPMC master controller in balancing the port voltages, the example of **Fig. 6** with initially unbalanced port voltages $V_{\mathrm{B,1}}$ and $V_{\mathrm{B,2}}$, and initial power levels according to **Table II** is used. Hence, constant power values P_{A}, P_{B} and P_{C} are drawn from/delivered to the converter ports in this simulation, while the MPMC master controller solely balances out the asymmetry between $V_{\mathrm{B,1}}$ and $V_{\mathrm{B,2}}$ by using the aforementioned redistribution of the power shares $P_{\mathrm{B,k,diff}}$. As already mentioned, since a direct power

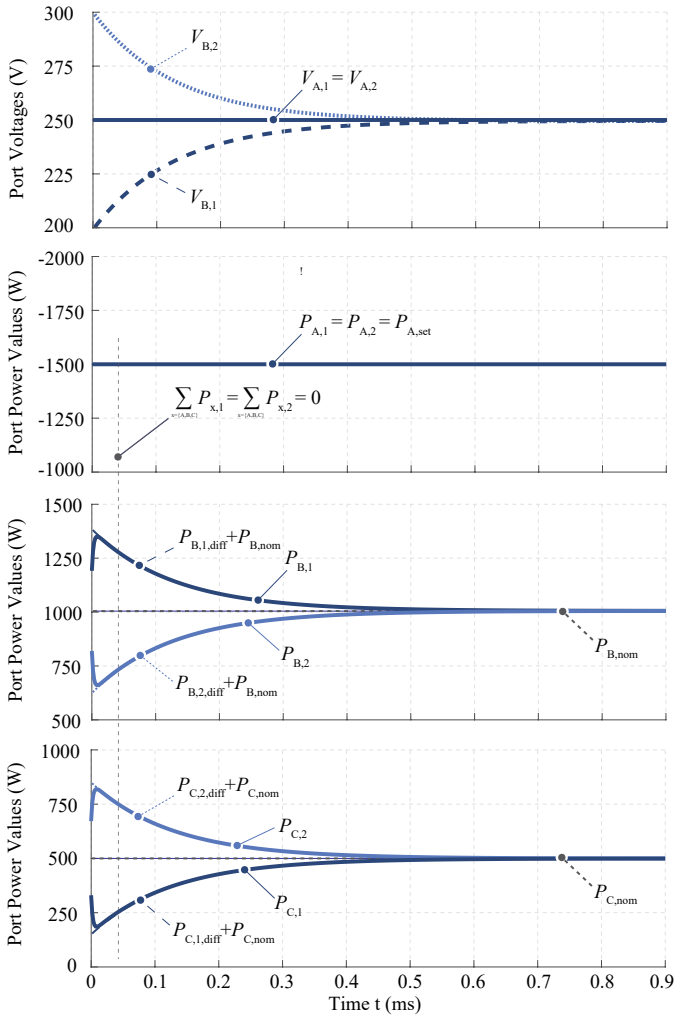

Fig. 8: Simulation results of the cell-dependent power set-points $P_{\mathrm{A,k,set}} = P_{\mathrm{A,k,diff}} + P_{\mathrm{A,nom}}$, $P_{\mathrm{B,k,set}} = P_{\mathrm{B,k,diff}} + P_{\mathrm{B,nom}}$ and $P_{\mathrm{C,k,set}} = P_{\mathrm{C,k,diff}} + P_{\mathrm{C,nom}}$ as well as the actual power values $P_{\mathrm{A,k}}$, $P_{\mathrm{B,k}}$ and $P_{\mathrm{C,k}}$ for the application of the MPMC master controller in the example of **Fig. 6**.

TABLE II: Initial conditions of the simulation of **Fig. 6** and the corresponding waveforms of **Fig. 8**.

P_A	P_B	P_C	$V_{A,1}$	$V_{A,2}$	$V_{B,1}$	$V_{B,2}$	V_C
$-3\,kW$	$2\,kW$	$1\,kW$	$250\,V$	$250\,V$	$200\,V$	$300\,V$	$15\,V$

transfer between series connected ports B_1 and B_2 is not possible, TAB 1 transfers the excess energy stored in $C_{B,1}$ to the parallel port C ($P_{B,1,diff} > 0$ and $P_{C,1,diff} < 0$), while TAB 2 retrieves the needed amount of energy from port C to recharge the capacitor $C_{B,2}$ ($P_{B,2,diff} < 0$ and $P_{C,2,diff} > 0$). Hence, during the step response, not only the port power levels $P_{B,k,set}$, but also the port power levels $P_{C,k,set}$, differ from the nominal power levels $P_{B,nom}$ and $P_{C,nom}$, respectively. The power levels $P_{A,k,set}$, however, stay constant ($P_{A,k,diff} = 0$), since there it is assumed that the voltages $V_{A,1}$ and $V_{A,2}$ are nicely balanced. The resulting port voltages $V_{B,1}$ and $V_{B,2}$, the power set-points $P_{A,k,set}$, $P_{B,k,set} = P_{B,k,diff} + P_{B,nom}$ and $P_{C,k,set} = P_{C,k,diff} + P_{C,nom}$, as well as the actual port power values $P_{A,k}$, $P_{B,k}$ and $P_{C,k}$ are shown in **Fig. 8**.

As expected from the P-controller of **Fig. 7(b)**, the two port voltages $V_{B,1}$ and $V_{B,2}$ exponentially converge to their nominal value $V_{B,nom}$. The same behavior can be found for $P_{B,1,diff}$ and $P_{B,2,diff}$, as they are directly proportional to the voltage error $V_{B,nom} - V_{B,k}$ according to (12). It can be seen, that the simulated output power values $P_{B,k}$ smoothly follow their reference values $P_{B,k,set} = P_{B,k,diff} + P_{B,nom}$, yielding the desired voltage balancing of $V_{B,1}$ and $V_{B,2}$.

Furthermore, the power transfer between $P_{B,1}$ and $P_{B,2}$ can only be performed through the parallel port C, and the sum of the cell-internal port power values always has to be zero (cf. **Fig. 8**), the power levels $P_{C,k,diff}$ has to equal $-P_{B,k,diff}$ during the complete simulation time.

In order to analyze the system behavior of a complete EV distribution network, a PI voltage controller emulating the superordinate battery charge controller is added to the simulation according to **Fig. 9**, which in reality calculates the required total converter power set-points $P_{HV,set}$ and $P_{LV,set}$ based on the momentary port voltages V_{HV} and V_{LV}.

This voltage controller in combination with the proposed MPMC master controller is applied to the same two-cell three-port converter as depicted in **Fig. 6**, however, in this simulation example, it is assumed that, due to component tolerances, the capacitor connected to the HV-port of TAB 1 has a lower capacitance than the one connected to TAB 2 (cf. **Fig. 10**). Hence, the employment of the proposed MPMC master controller becomes essential, as will be shown in the following by means of the simulated, primary side referred port voltages and power waveforms.

Initially, the converter is in steady-state with a HV-output power P_{HV} of $3\,kW$, a LV-output power P_{LV} of $600\,W$ and a symmetric port voltage distribution between the series connected converter ports as shown in **Fig. 10**. This is the most common situation during charging operation, as the major part of the system power is used to recharge the large HV battery and only a small share of the power is used to recharge the small LV battery. At the time t_{st}, a load step occurs in both, the HV as well as the LV port, which is caused when a high power LV load, e.g. turning-on the air conditioning, is activated during charge operation. The load step in the HV port results from the input power limitation in the PFC port of $3.6\,kW$, since now more power has to be delivered to the LV port, and therefore only the remainder of $P_{PFC} - P_{LV}$ can be used to recharge the HV battery. These load steps activate the superordinate battery charge controller as well as the central MPMC master controller, which try to regulate the output voltages of the converter.

The general shapes and magnitudes of the individual port power values $P_{HV,1}$, $P_{HV,2}$, $P_{LV,1}$ and $P_{LV,2}$, shown in **Fig. 10**, are dominated by the step response of the battery voltage controller (cf. **Fig. 9**), since its time constant is much higher than the one of the central MPMC master controller. However, a certain difference between the two port power values $P_{HV,1}$ and $P_{HV,2}$ can be observed (blue-shaded), which are induced by the MPMC master controller by generating a certain voltage balancing power share $P_{HV,k,diff}$, based on the voltage difference $V_{HV,1} - V_{HV,2}$ in order to keep the port voltages at the HV DC-Bus $V_{HV,1}$ and $V_{HV,2}$ balanced. Accordingly, the same power difference between $P_{LV,1}$ and $P_{LV,2}$ is visible, due to the indirect power transfer between series connected cells via port C. As a result of the MPMC master controller, which features a much higher

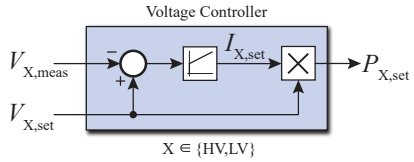

Fig. 9: Voltage PI-controller used to control the power set-point values of the MPMC converter.

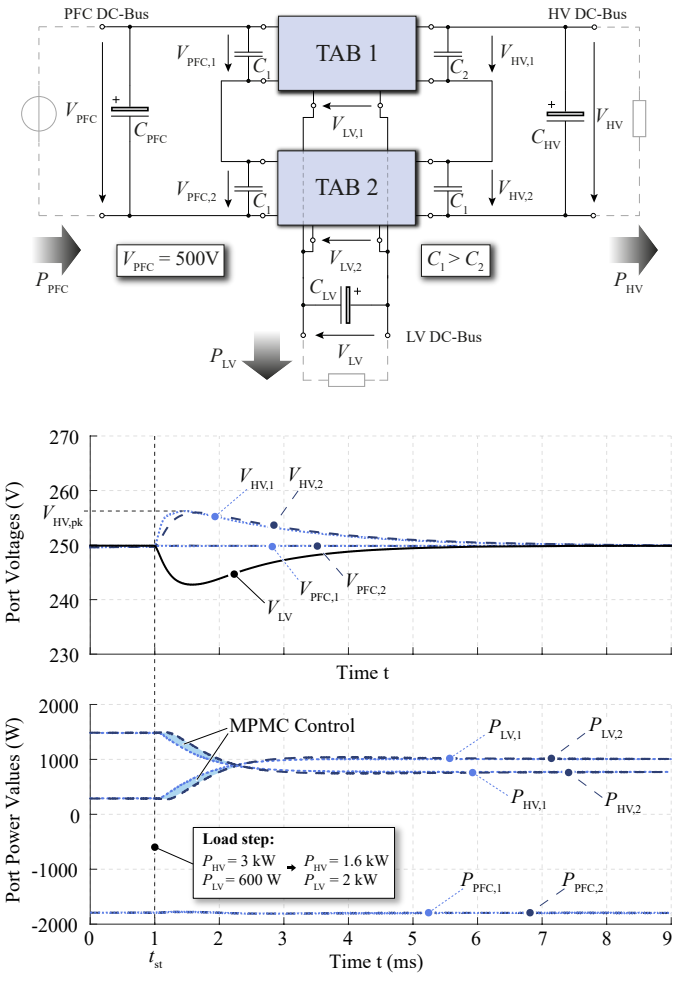

Fig. 10: Simulation results of a two-cell three-port converter system with different capacitor values in the series connected HV ports and a load step at the time t_{st}.

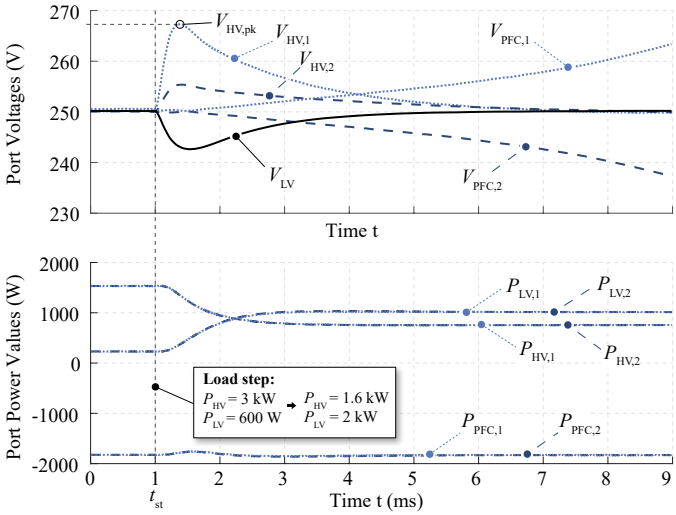

Fig. 11: Simulation results of a two-cell three-port converter system with different capacitor values in the series connected HV ports and a load step at the time t_{st} with deactivated voltage balancing controller.

controller bandwidth than the battery charge controller, these voltage differences remain small, hence excessive overvoltages across the series connected converter ports can be avoided, even though the DC link capacitor values are different.

Finally, due to the aforementioned active port voltage balancing control, the PFC-sided voltages $V_{PFC,1}$ and $V_{PFC,2}$ are perfectly balanced and are therefore not affected by the asymmetric voltages in the HV ports.

In order to show the importance and the benefits of the proposed controller, the same simulation was done for the system without the MPMC master controller, which means without the voltage balancing power share $P_{HV,k,diff}$. In this case, the port power is equally distributed among the different converter cells, irrespective of the particular port voltages. It is important to note that in contrast to the previously mentioned common duty cycle control, this common power control does not lead to equal duty cycles in all individual cells, since in this case the individual cell-internal duty cycles also depend on the individual cell voltages. The resulting waveforms are shown in **Fig. 11**, where two key differences to **Fig. 10** immediately become apparent: On the one hand, a large voltage overshoot in the HV port of TAB 1 can be observed, arising from the asymmetry of the capacitance values of the series connected capacitors. However, at least after a certain time the voltages at the HV port are balanced again.

On the other hand, the far greater evil, is that at the PFC port the system is unstable, as the PFC-sided voltages end up in a runaway situation.

These simulation results clearly show the importance of the proposed MPMC master control strategy in order to ensure a stable converter operation with balanced voltage and power distribution among the individual converter cells.

V. Conclusion

In this paper, a novel multi-port multi-cell (MPMC) topology has been presented, which allows to overcome the arising design challenges for converter systems in applications with highly different input and output voltage levels. Among other advantages, the MPMC topology reduces the cell-internal port voltage ratios, and therefore leads to beneficial characteristic impedances of the converter ports. The matching of these characteristic impedances enables the design of highly efficient converter systems, even for extremely high step-down ratios.

Finally, a new control strategy for the MPMC converter was presented, which balances asymmetrical voltage distributions in the series connected cell ports, and at the same time delivers the total required bus power values to the respective converter outputs. Consequently, semiconductors with lower breakdown voltages can be employed, which reduce the overall conduction losses due to their beneficial figures-of-merit.

Simulations were shown to verify the operation principle and the necessity of the proposed MPMC control strategy.

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