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Multi-Port Multi-Directional Converter with Multi-Mode Operation and Leakage Energy Recycling for Green Energy Processing

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Abstract: In this article, a novel multi-port multi-directional converter (MPMDC) is proposed. Even though the power stage of the MPMDC belongs to a single-stage structure, it can control power flow direction handily among ports and achieve converter operation in up to five modes. The MPMDC has the feature of galvanic isolation and can obtain a high voltage conversion ratio even under the adoption of only one inductor and one transformer. The leakage energy of the transform can be recycled to improve overall efficiency. Once the MPMDC is applied to deal with renewable energy, battery, and bus energy, the advantage of multi-directional control of power flow can advance an energy storage system to perfectly function power conditioning feature. In addition to the discussion of converter operation, voltage gain, voltage stress, current stress, and inductance design are analyzed theoretically. Comparisons with some of the latest similar converters are also carried out. A 200-W prototype is built and measured. According to the practical results, it is verified that the hardware measurements meet the theoretical derivations and the MPMDC is validated. The maximum efficiency of the converter is up to 94%.

Keywords: multi-port multi-directional converter; galvanic isolation; high conversion ratio; leakage energy recycling; single stage

Citation: Shen, C.-L.; Chen, L.-Z.; Chen, G.-Y.; Yang, C.-M. Multi-Port Multi-Directional Converter with Multi-Mode Operation and Leakage Energy Recycling for Green Energy Processing. *Energies* **2022**, *15*, 5629. https://doi.org/10.3390/en15155629

Academic Editors: Jenn-Jong Shieh, Yeu-Torng Yau and Kuo-Ing Hwu

Received: 17 June 2022
Accepted: 29 July 2022
Published: 3 August 2022

1. Introduction

Recently, with the purpose of retarding global warming and climate change, the generation and application of renewable power have been developing rapidly, and especially focusing on solar power [1–4] and wind turbines [5,6]. However, the usage of these kinds of expeditiously growing energy is highly confined by some problems, such as weather, intermittence, and unstableness. To overcome the problems, incorporating an energy storage system (ESS) to function as the feature of energy conditioning is an effective solution [7–9]. The ESS can save the generation power exceeding during periods of light loading and afterwards release its stored energy during periods of heavy loading. The reliability of a power system can accordingly be increased and the imbalance between renewable power supply and load demand can also be alleviated. In addition, owing to the significant growth and expansion of the electrical automobile industry [10,11], the capability and performance of lithium cells have been improving more and more, which enriches the EES market and its related applications as well. It is highly expectable that hybrid-generation systems that combine green energy, a storage system, and utility will be in demand and developed. In this article, a novel power converter is therefore proposed to deal with multiple types of energy sources.

Figure 1a is a conventional PV power system, in which a battery is incorporated to serve as energy backup. Since the PV panels and the battery are both low-voltage sources, for DC-bus connection the system requires two converters to process power individually.

One is the unidirectional high-step-up converter (UHSC), which boosts PV voltage to a much higher level [12–14], and the other is the bidirectional converter (BC), which performs battery charging and discharging [15–17]. However, the traditional structure has disadvantages, such as low total conversion efficiency, high cost, and huge size. To combine the two individual converters into a single one, a multi-port converter (MPC) was developed and has become the current trend. As illustrated in Figure 1b, an MPC, in general, integrates two DC–DC converters into a single-stage structure. In [18,19], the power stages of the MPCs in a single-stage structure are mainly the combination of basic converters. Having a simple structure is their merit, but no isolation and low voltage gain are drawbacks. In [20], the MPC can gain a high conversion ratio, however, in which an input port is in a floating connection. The three ports can be in common connection to yield an easier design of a control circuit [21–23]. Nevertheless, these converters still exist with the disadvantage of no galvanic isolation. In [24], the converter is derived by fundamental boost and buck structures to obtain an MPC, in which the power stage is simple but galvanic isolation still cannot be achieved. The converter in [25] incorporates a single core to fulfill the feature of multi-port and to accomplish a variety of operation modes, but it cannot possess the isolation feature and is unable to deal with two different kinds of input energy, limiting its application field toward renewable generation system. The converter utilizes two magnetic devices to carry out multi-port energy processing and can accomplish many operation modes [26]. However, its voltage gain is lower than most structures of MPCs. The MPC can be realized with a lower account of power devices to lower cost [27], nevertheless, in which the input port will influence the function of battery charging. Besides, the input port is floating. The MPCs in [28–33] adopt transformers and/or coupled inductors to diminish the problems of non-isolation and low conversion gain. However, it is unavoidable that the converters still have different kinds of shortcomings. The voltage gain of the converter in [28] is low; besides, more magnetic components and active switches have to be required. Even though high voltage gain can be completed in [29,30], the DC bus is incapable of charging the battery. In [31], the converter lacks the function of battery charging from the DC bus and exists the demerit of low voltage gain. Concerning [32], more active power switches must be employed and voltage gain is not as high as expected, both of which are shortcomings.

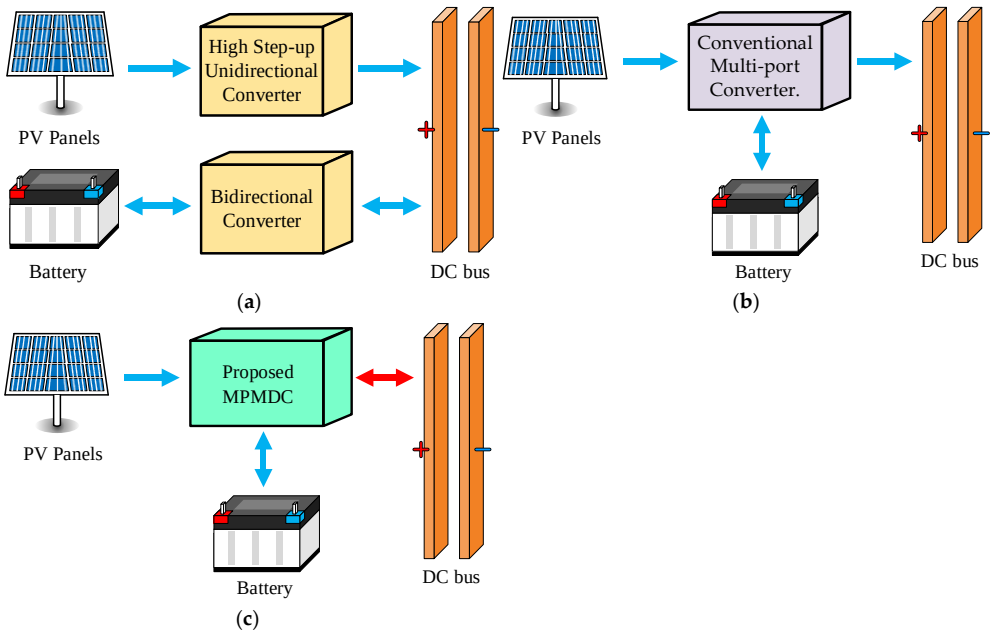


Figure 1. A brief diagram to depict a PV power system along with a battery and to indicate power flow direction: (**a**) the traditional one employs two converters, (**b**) the conventional multi-port converter, and (**c**) the proposed MPMDC.

In order to thoroughly solve all the aforementioned disadvantages, this article proposes a novel multi-port multi-direction converter (MPMDC), as shown in Figure 1c, which has the merits of high voltage-conversion ratio, the feature of galvanic isolation, leakage energy recycling, battery charging/discharging, and multi-direction energy controlling. The MPMDC is aiming at power processing for a microgrid system, not only for a UPS. A microgrid system that incorporates PV panels and battery and then connects to DC bus needs isolation between the PV and battery/bus, but not necessarily between battery and bus. Therefore, the proposed converter is designed without isolation between the battery and the DC bus. The MPMDC can accomplish a variety of system operation modes as many as up to five modes. The power flow direction of each mode is indicated in Figure 2 and described as follows.

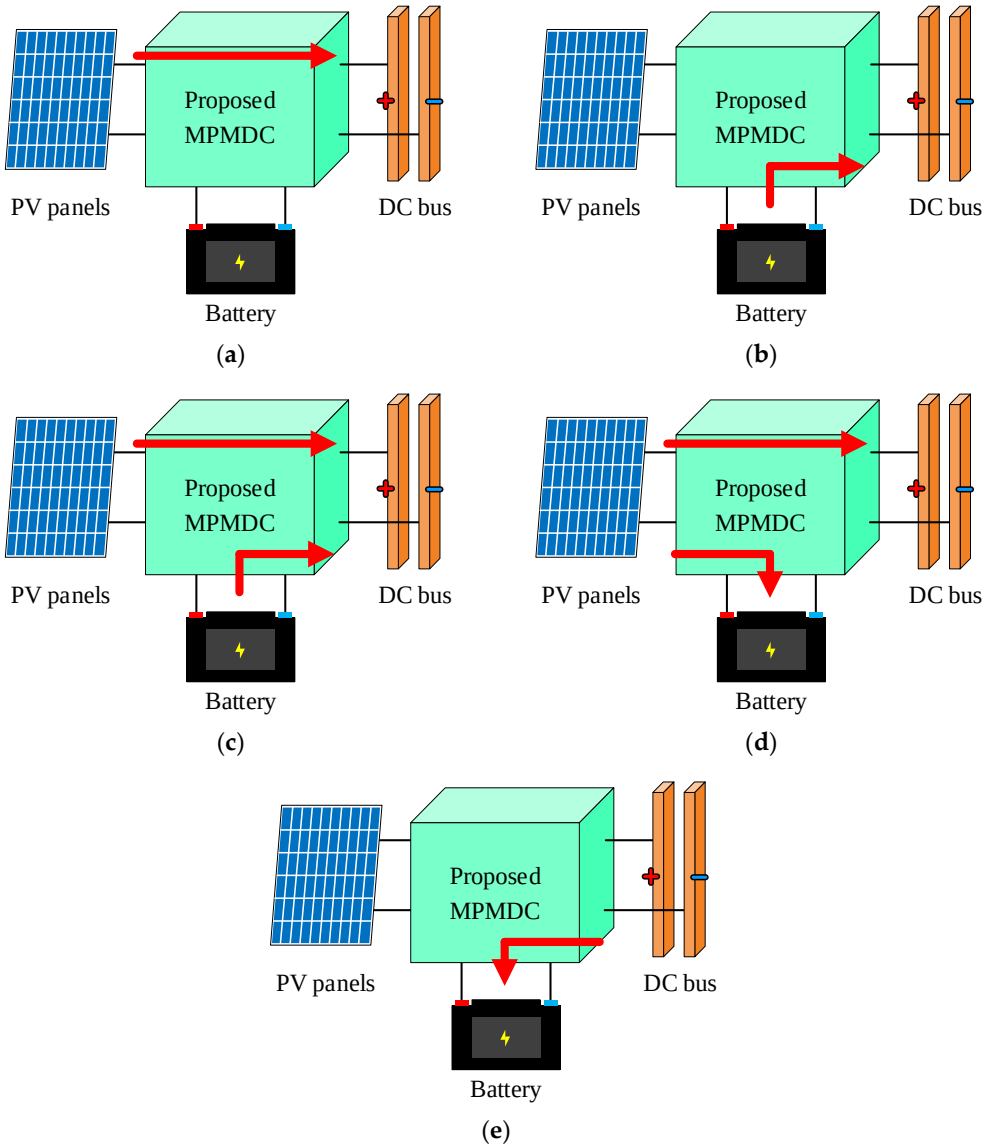


Figure 2. Five operation modes of the proposed converter: (**a**) SISO-PV mode; (**b**) SISO-battery mode; (**c**) DISO mode; (**d**) SIDO mode; and (**e**) BF mode.

1. Single input and single output for PV power processing (SISO-PV mode): Only the PV panels forward power to the DC bus, as shown in Figure 2a. In this mode, the battery has been fully charged and PV panels inject all the generated solar power into the DC bus;

2. Single input and single output for battery-energy providing (SISO-battery mode): As referred to in Figure 2b, only the battery discharges toward the DC bus. This mode works at night or during a rainy day;
3. Dual-input single-output mode (DISO mode): During the heavy-load period, the DC bus must draw sufficient power from the generation system. To meet the load demand, the PV panels and battery will provide energy simultaneously, which is illustrated in Figure 2c;
4. Single-input dual-output mode (SIDO mode): The power flow is illustrated in Figure 2d. While in the period of intensive insolation, The PV panels can supply enough power to charge the battery and feed the DC bus as well;
5. Back-feeding mode (BF mode): As shown in Figure 2e, under the operation of BF mode, the MPMDC can draw energy from the DC bus to charge the battery.

2. Converter Structure and Operation Analysis

The power stage of the proposed MPMDC is depicted in Figure 3. What the components in Figure 3 stand for are described as follows: the V_{pv}, V_{bat}, and V_{bus} are the voltages of PV panels, battery, and DC bus, respectively; the S_1–S_5 are power switches, which inherently have body diodes D_{S1}–D_{S5} in turn and parasitic capacitances C_{S1}–C_{S5} as well; the D_1–D_5 denote as diodes; the C_1 and C_0 are capacitors, while L_1 expresses inductor; in addition, N_1 and N_2 represent the turns of the primary and secondary windings of the transformer, respectively, and L_m and L_k indicate the magnetizing inductance and leakage inductance of the transformer, respectively.

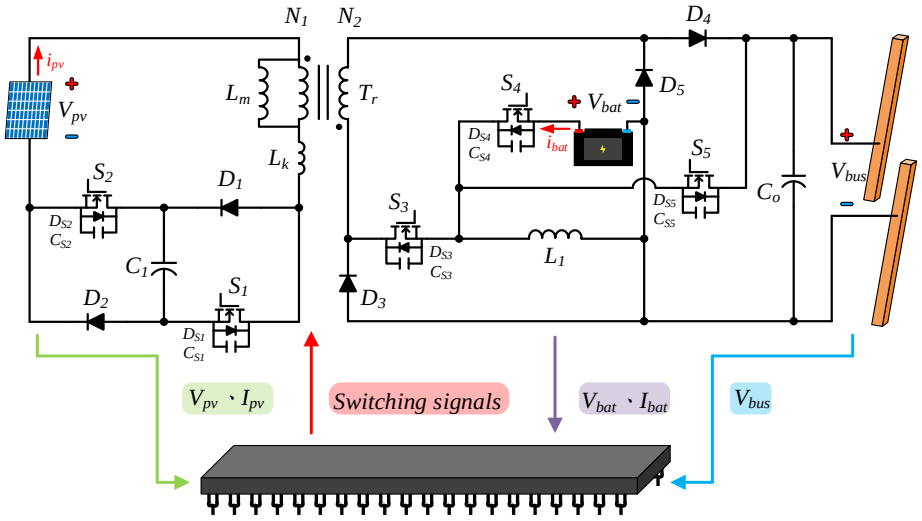


Figure 3. The power stage of the proposed multi-port multi-direction converter.

2.1. Operation Principle

The voltage polarity and current direction of the MPMDC are defined in Figure 4. For the analysis of the converter in steady state, some conditions are made as follows:

1. Capacitors C_1 and C_0 are large enough so that the voltage ripples on C_1 and C_0 can be neglected;
2. The diodes D_1–D_5 are considered ideal;
3. Parasitic capacitance in power switches is very small so that it can be reasonably omitted;
4. The leakage inductance L_k is much smaller than the magnetizing inductance L_m;
5. The duty ratios of switches S_1 and S_2 are all less than 0.5;
6. The turns ratio of the transformer T_r is defined as n and equal to $\frac{N_2}{N_1}$.

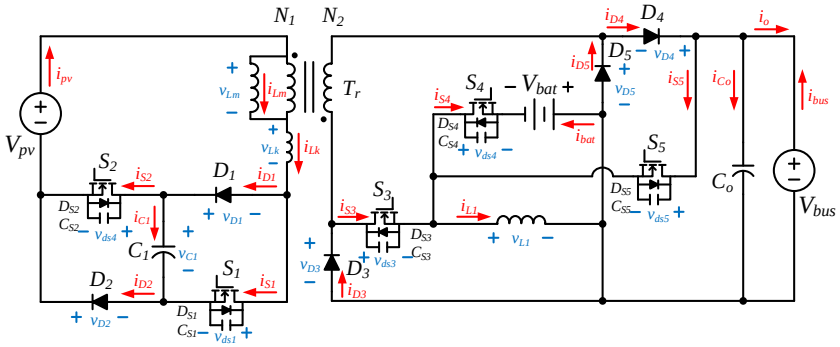


Figure 4. Definition of voltage polarity and current direction of the MPMDC.

2.1.1. SISO-PV Mode

In SISO-PV mode, switches S_1 and S_2 are controlled, that is, both of which are in charge of the role of main switches. While operating in this mode, both switches are turned on and off simultaneously and driven by an identical control signal. The converter operation can be mainly divided into two stages over one switching cycle. The key waveforms of the converter in SISO-PV are depicted in Figure 5. In addition, the corresponding equivalent stages are shown in Figure 6.

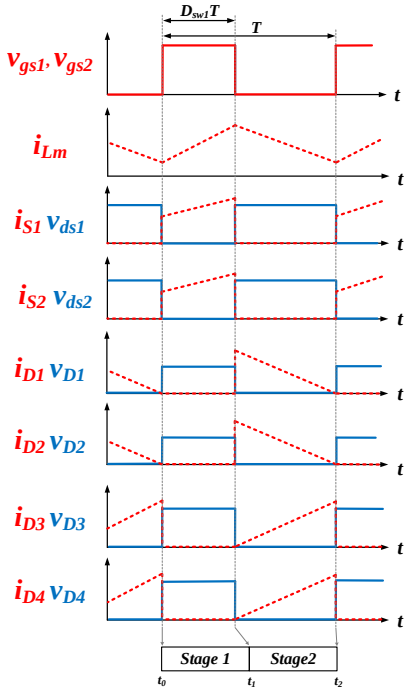


Figure 5. The key waveforms of the proposed converter while operating in SISO-PV mode.

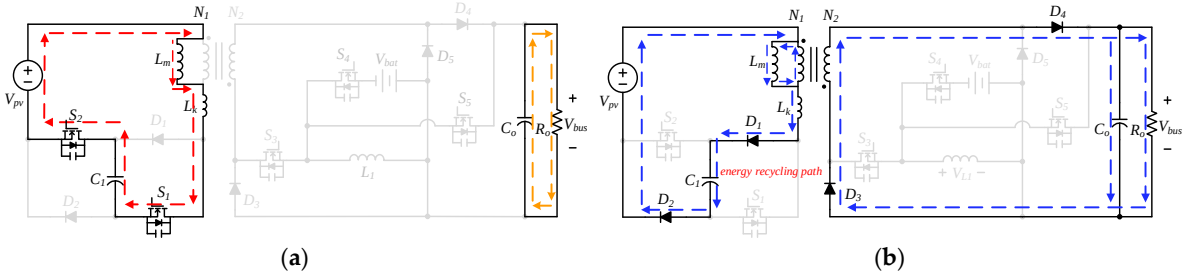


Figure 6. Equivalent stages of the converter while operating in SISO-PV mode: (**a**) stage 1; and (**b**) stage 2.

Stage 1 [t_0–t_1]

This stage starts at time $t = t_0$, as shown in Figure 6a. The switches S_1 and S_2 are turned on at the same time, and the diodes D_1–D_5 are all in OFF-state. Over the whole time interval t_0–t_1, that is, the ON-time period $D_{sw1}T$, the L_m and L_k both draw energy from PV panels and capacitor C_1. Meanwhile, the output capacitor C_o pumps its stored energy to the DC bus. Since switch S_3 and diode D_3 break the current path of the transformer, therefore, there is no current flowing through the transformer. This stage ends at the time switches S_1 and S_2 are turned off.

Stage 2 [t_1–t_2]

At $t = t_1$, as shown in Figure 6b, the switches S_1 and S_2 are turned off and diodes D_1–D_4 become in ON-state. The energy stored in L_m has therefore released to the DC bus via the transformer T_r. The PV panels and the magnetizing inductor L_m charge capacitor C_1 simultaneously. The energy of leakage inductance L_k is recycled to capacitor C_1. As switches S_1 and S_2 are turned on again, the operation of SISO-PV mode over period T completes.

2.1.2. SISO-Battery Mode

In SISO-battery mode, the main switches become S_4 and S_5, that is, both of which are turned on and off periodically and complementarily, while the other switches are kept in OFF-state. During this mode, the steady-state operation of the MPMDC can be mainly divided into two stages over one switching cycle. Figure 7 depicts the key waveforms of the converter and Figure 8 is the equivalent stage for each stage.

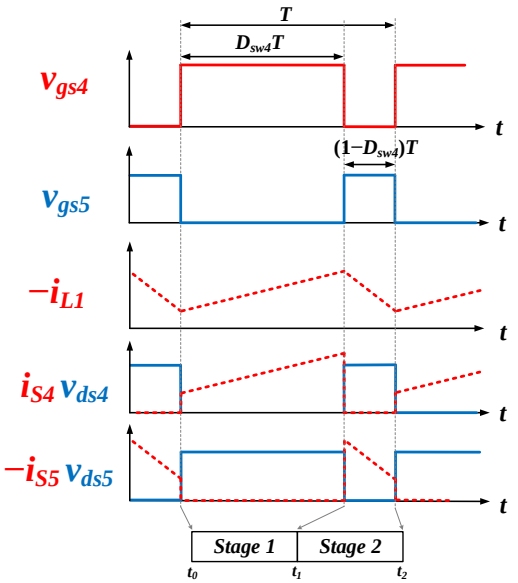


Figure 7. The key waveforms of the proposed converter while operating in SISO-battery mode.

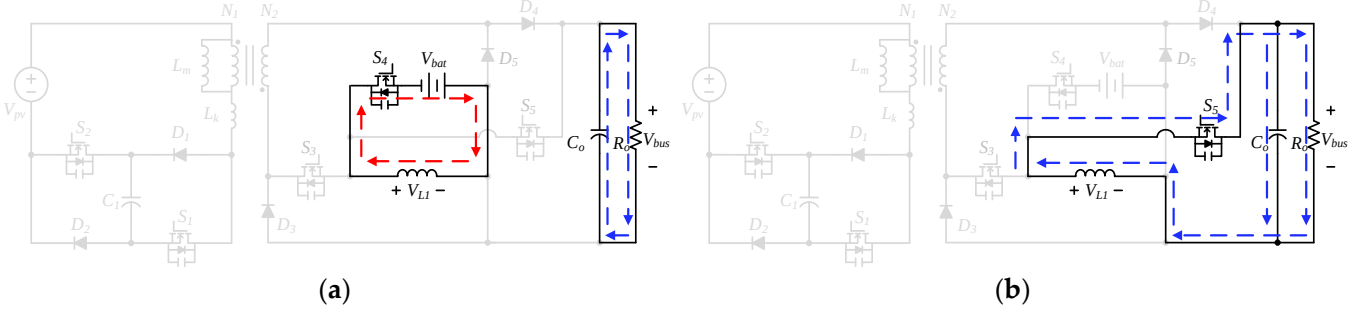


Figure 8. Equivalent stages of the proposed converter in SISO-battery mode: (**a**) stage 1; and (**b**) stage 2.

Stage 1 [t_0–t_1]

As shown in Figure 8a, this stage starts at the time $t = t_0$. In this stage, switch S_4 keeps closed, and thus the voltage across inductor L_1 will be V_{bat}. The current flowing through L_1 increases linearly. The capacitor C_o discharges its energy to the load R_o. When switch S_4 is turned off, this stage ends.

Stage 2 [t_1–t_2]

The time interval of this stage is from t_1 to t_2. The equivalent stage is shown in Figure 8b. During this time interval, switch S_5 is in ON-state, whereas S_4 is kept open. The energy stored in L_1 is released to the load R_o, and therefore its current decreases linearly. When S_5 is turned off and the switch S_4 is turned on again, this stage ends.

2.1.3. DISO Mode

In DISO mode, switches S_1, S_2 and S_4 serve as main switches, in which S_1 and S_2 are turned on and off simultaneously; meanwhile, the switch S_4 is also turned on at the same time as S_1 and S_2 but its ON-state will last for a longer time than S_1 and S_2. The operation of DISO can be mainly divided into four stages over one switching cycle. The key waveforms of DISO are depicted in Figure 9. In addition, the corresponding equivalent stage of each stage is illustrated in Figure 10.

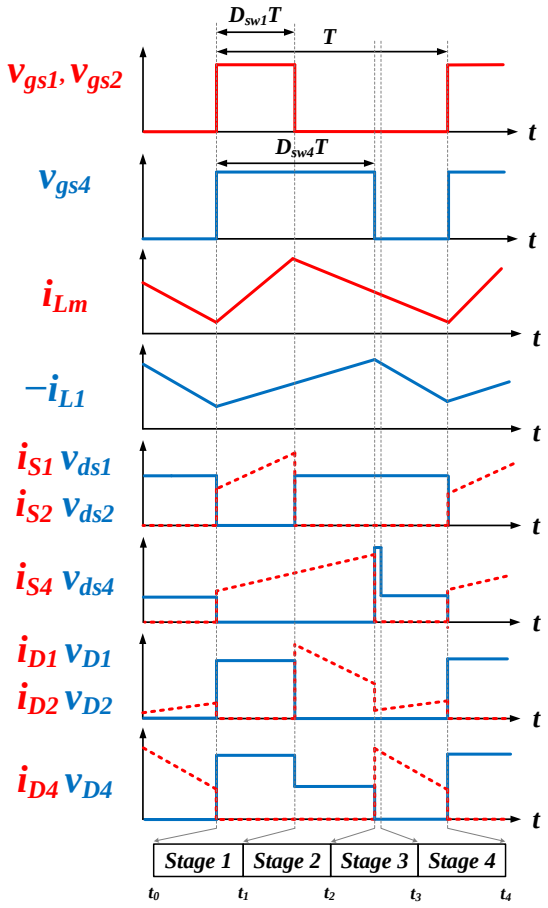


Figure 9. The key waveforms of the proposed converter in DISO mode.

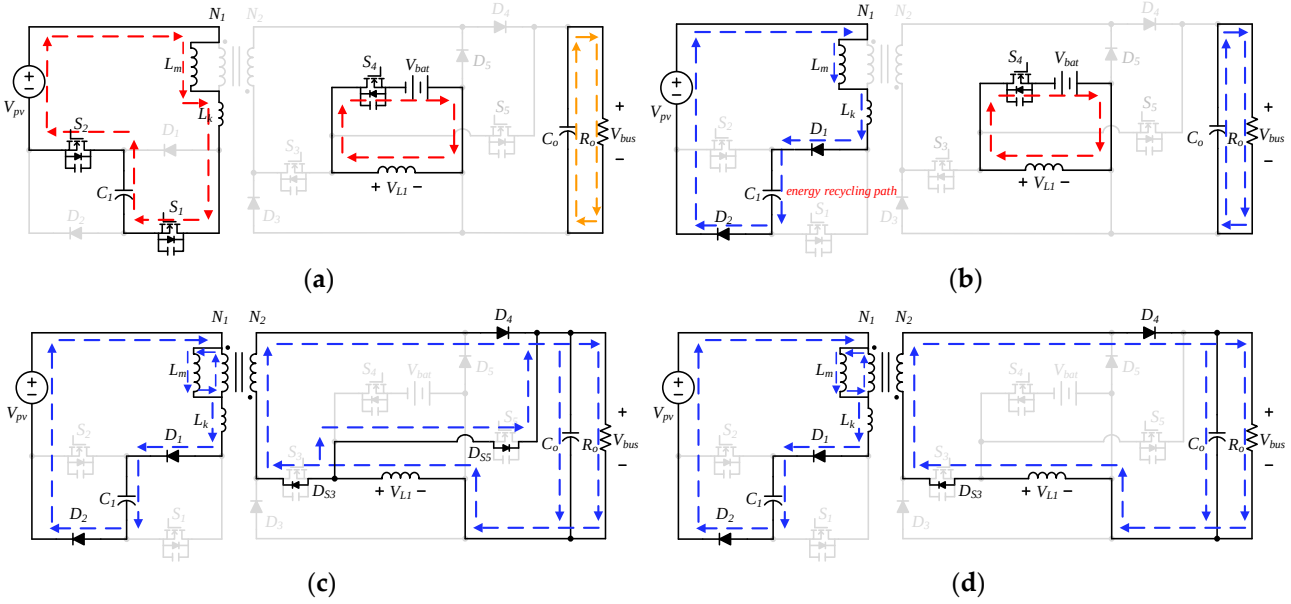


Figure 10. Equivalent stages of the proposed converter in DISO mode: (**a**) stage 1; (**b**) stage 2; (**c**) stage 3; and (**d**) stage 4.

Stage 1 [t_0–t_1]

This stage starts at the time $t = t_0$, of which the equivalent stage circuit is presented in Figure 10a. During the time interval t_0–t_1, switches S_1, S_2 and S_4 are closed and then the magnetizing inductance L_m and leakage inductance L_k absorb energy from the PV panels and capacitor C_1. The battery V_{bat} is across the inductor L_1 directly and the current flowing through L_1 increases linearly. The capacitor C_o discharges to the load R_o. When the switches S_1 and S_2 are turned off, this stage ends.

Stage 2 [t_1–t_2]

This stage lasts from t_1 to t_2 and Figure 10b is the equivalent stage circuit. Switch S_4 is still in ON-state and diodes D_1 and D_2 are forward biased. The PV panels along with magnetizing inductance L_m release energy to capacitor C_1. At the same time, leakage inductance L_k recycles its energy to capacitor C_1. The battery voltage V_{bat} is still charging the inductor L_1, and capacitor C_o supplies energy to the load R_o. Since switch S_3 and diode D_3 have broken the current path of the transformer, no current flows through the transformer. This operating stage ends when switch S_4 is turned off.

Stage 3 [t_2–t_3]

At the time t_2, the converter operation enters Stage 3. Figure 10c is the equivalent stage of this stage, in which diodes D_1, D_2, and D_4 are forward biased, and parasitic diodes D_{S3} and D_{S5} are also in ON-state. The inductor L_1 releases energy to the load R_o through D_4, D_{S3}, and D_{S5}. When parasitic diode D_{S5} is reversely biased, this stage ends.

Stage 4 [t_3–t_4]

The time interval of this stage is from t_3 to t_4. As shown in Figure 10d, diodes D_1, D_2, D_4, and parasitic diodes D_{S3} still keep conducting. The energy stored in L_m and L_1 is simultaneously released to the load R_o. This operation stage ends when switches S_1, S_2, and S_4 have been turned on again.

2.1.4. SIDO Mode

While in SIDO mode, the switches S_1, S_2, and S_3 act as the main switch. The S_1 and S_2 are turned on and off at the same time, that is, both of which are controlled by an identical switching signal. Concerning S_3, it is turned on synchronously as S_1 and S_2 but

asynchronously at turn-off time. The converter operation in SIDO can be divided into four stages over one switching cycle. The key waveforms are shown in Figure 11, while the equivalent stages are illustrated in Figure 12.

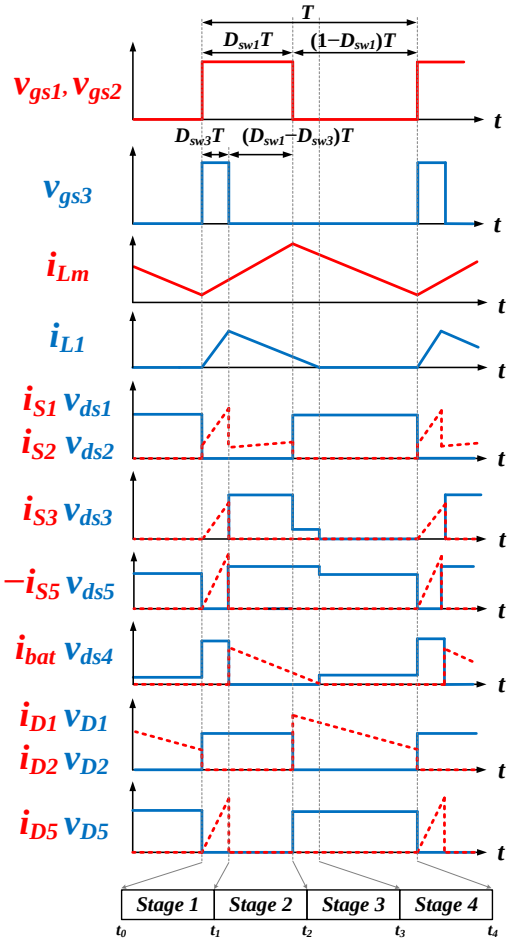


Figure 11. The key waveforms of the proposed converter in SIDO mode.

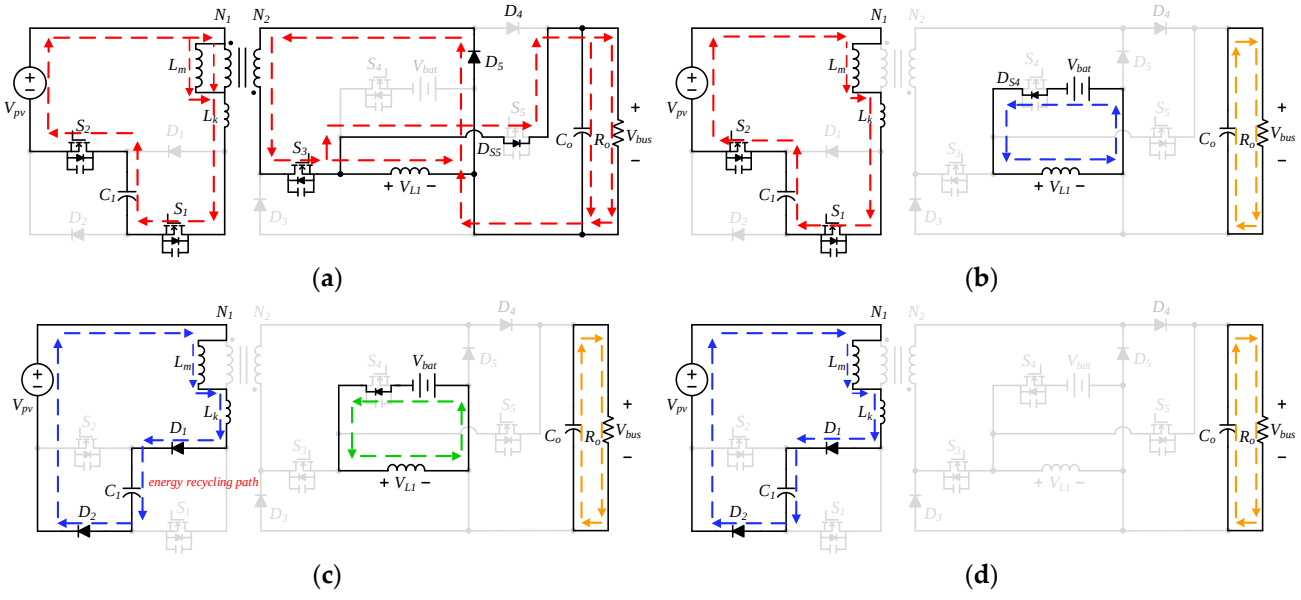


Figure 12. Equivalent stages of the proposed converter in SIDO mode: (**a**) stage 1; (**b**) stage 2; (**c**) stage 3; and (**d**) stage 4.

Stage 1 [t_0–t_1]

This stage starts at $t = t_0$. Figure 12a is the equivalent stage circuit, in which switches S_1, S_2, and S_3 are turned on at the same time. The series voltage of V_{pv} and V_{C1} is connected to L_m and L_k, and thus the currents i_{Lm} and i_{Lk} increase linearly. The secondary of the transformer forwards energy to the inductor L_1 and the load R_o. When the switch S_3 is turned off and the body diode of switch S_4, D_{S4}, is forward biased, this stage ends.

Stage 2 [t_1–t_2]

The time interval of this stage is from t_1 to t_2, as shown in Figure 12b, in which S_3 is OFF while S_1 and S_2 are still ON. The PV panels and capacitor C_1 keep charging the L_m and L_k. The inductor L_1 releases its stored energy to charge the battery, and capacitor C_o supplies the load R_o. In this state, the current path of the transformer will be broken by switch S_3 and diode D_3. This stage ends when both switches S_1 and S_2 are turned off.

Stage 3 [t_2–t_3]

At $t = t_2$, Stage 3 begins, whose equivalent stage is shown in Figure 12c. At the primary of the transformer, the diodes D_1 and D_2 become forward-biased, and the energy stored in the L_m and L_k is released to capacitor C_1. There is the same circuit behavior at the secondary of the transformer, in which the inductor L_1 is still charging the battery, and capacitor C_o supplies the load R_o. When the current of inductor L_1 decreases to zero, this stage ends.

Stage 4 [t_3–t_4]

The time in this stage is from t_3 to t_4, as shown in Figure 12d. During this time interval, diodes D_1 and D_2 are still conducted. The magnetizing inductor L_m is continuously charging capacitor C_1, and capacitor C_o supplies the load R_o. This operating stage ends when switches S_1, S_2, and S_3 have been turned on again.

2.1.5. BF Mode

In BF mode, the main switches are S_4 and S_5, which are controlled complementarily. The BF-mode operation has two main stages over one switching cycle. The key waveforms of BF mode are depicted in Figure 13; meanwhile, its corresponding equivalent stages are illustrated in Figure 14.

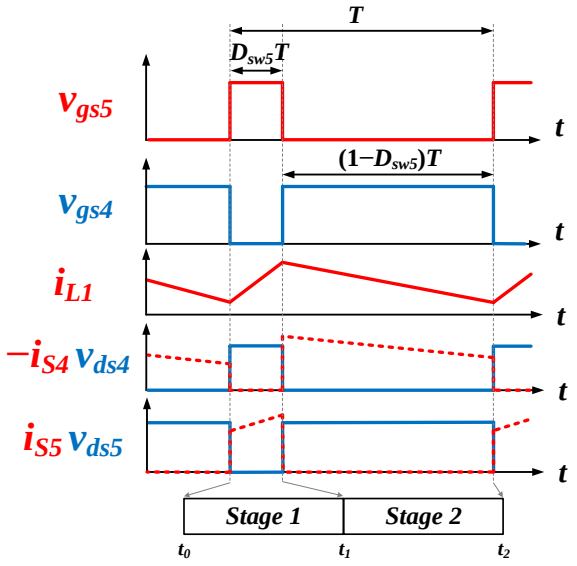


Figure 13. The key waveforms of the proposed converter in BF mode.

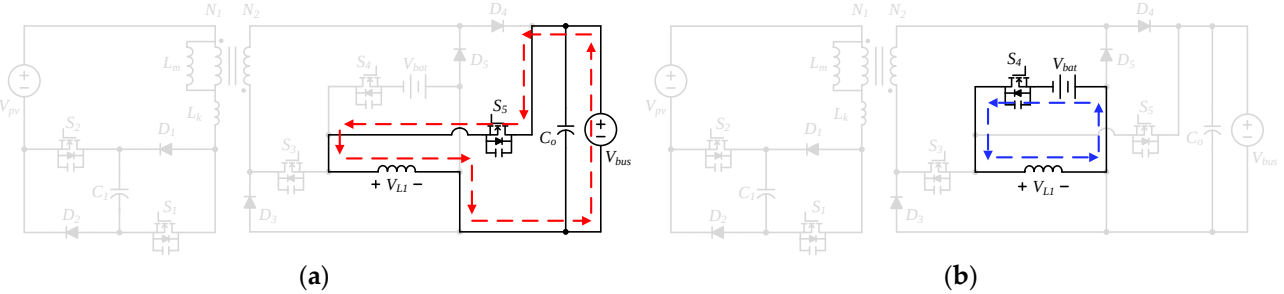


Figure 14. Equivalent stages circuits in BF mode: (**a**)sStage 1; and (**b**) stage 2.

Stage 1 [t_0–t_1]

As shown in Figure 14a, this stage lasts from t_0 to t_1, in which switch S_5 is ON-state. The voltage of C_o is applied to L_1 and therefore the current flowing through L_1 will increase linearly. This linearly increasing current stops raising at the time switch S_5 is turned off.

Stage 2 [t_1–t_2]

At the moment S_5 is turned off and S_5 is turned on, this stage starts. Stage 2 continues from t_1 to t_2, the equivalent stage of which is shown in Figure 14b. During this stage, the energy of inductor L_1 is released and then charges the battery. This operating stage ends when switch S_5 is turned on again.

3. Steady-State Analysis

To simplify the steady-state analysis of the proposed converter, the following assumptions are made:

- All components are considered ideal;
- All the values of capacitors are large enough to keep their voltage constant during one switching cycle;
- The turns ratio of the transformer T_r is expressed as $n = \frac{N_2}{N_1}$;
- The L_m of the Tr and the inductor L_1 both are operated in CCM.

3.1. Voltage Gain

The voltage-gain derivation toward the operation modes, that is, SISO-PV mode, SISO-battery mode, DISO mode, SIDO mode, and BF mode, are discussed one by one as follows.

3.1.1. Derivation for SISO-PV Mode

As referred to in Figure 6a, the switches S_1 and S_2 are ON, and the series voltage of V_{C1} and V_{pv} is connected to L_m. That is,

$$V_{Lm,SISO\text{-}PV} = V_{pv} + V_{C1} \tag{1}$$

When the switches S_1 and S_2 are OFF, as shown in Figure 6b, the difference voltage of V_{pv} and V_{C1} is applied to L_m. In addition, the secondary of the transformer is connected to the load through the diodes D_3 and D_4. Accordingly, the following relationships hold:

$$V_{Lm,SISO\text{-}PV} = V_{pv} - V_{C1} \tag{2}$$

and

$$nV_{Lm,SISO\text{-}PV} = -V_{bus} \tag{3}$$

Based on the volt-second balance criterion (VSBC), the voltage gain of bus voltage to PV voltage in SISO-PV mode, $M_{SISO\text{-}PV}$, is therefore concluded as:

$$M_{SISO\text{-}PV} = \frac{V_{bus}}{V_{pv}} = \frac{2nD_{sw1}}{1-2D_{sw1}}, \tag{4}$$

in which the D_{sw1} stands for the duty ratio of S_1. To further understand how the D_{sw1} affects the voltage gain $M_{SISO\text{-}PV}$, the curve to illustrate their relationship is depicted in Figure 15, in which the turns ratio, n, is set to be 1.5.

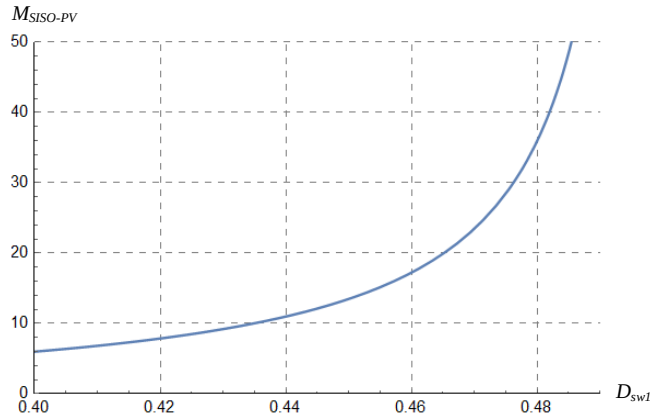


Figure 15. The voltage gain of the converter in SISO mode, $M_{SISO\text{-}PV}$, versus duty cycle D_{sw1}.

3.1.2. Derivation for SISO-Battery Mode

In Figure 8a, switch S_4 is closed, and the battery is directly connected to inductor L_1. Then,

$$V_{L1,SISO\text{-}Battery} = -V_{bat}. \tag{5}$$

While switch S_4 is open, the corresponding equivalent stage is shown in Figure 8b, in which the inductor L_1 pumps its stored energy to the bus. That is,

$$V_{L1,SISO\text{-}Battery} = V_{bus}. \tag{6}$$

Similarly, based on VSBC, the voltage gain of the converter in SISO-battery mode can be expressed as:

$$M_{SISO\text{-}battery} = \frac{V_{bus}}{V_{bat}} = \frac{D_{sw4}}{1-D_{sw4}}. \tag{7}$$

In (7), the $M_{SISO\text{-}battery}$ denotes the ratio of bus voltage to battery voltage. The relationship between the voltage gain $M_{SISO\text{-}Battery}$ and duty cycle D_{sw4} is represented in Figure 16.

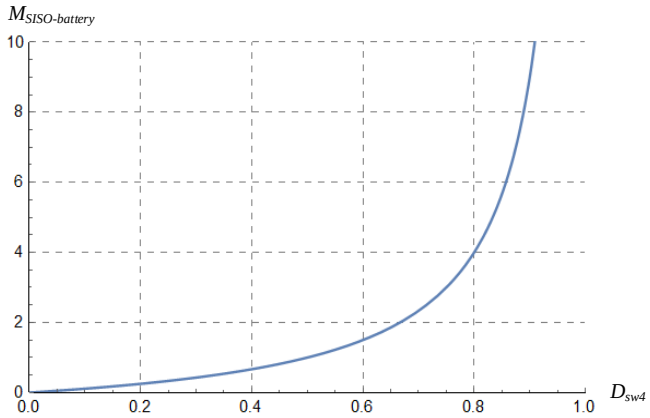


Figure 16. The voltage gain of the converter in SISO mode, $M_{SISO\text{-}battery}$, versus duty cycle D_{sw4}.

3.1.3. Derivation for DISO Mode

To derive the voltage gain of the converter in DISO mode, Figure 10 is referred to. In Figure 10a, switches S_1, S_2, and S_4 are closed. On the primary side of the transformer, magnetizing inductance L_m absorbs energy from the PV panels and capacitor C_1. On the secondary side, the battery charges the inductor L_1. Therefore,

$$V_{Lm,DISO} = V_{pv} + V_{C1}. \tag{8}$$

$$V_{L1,DISO} = -V_{bat}. \tag{9}$$

When switches S_1 and S_2 are turned off, as shown in Figure 10b, capacitor C_1 will be charged by the PV panels and the L_m. Therefore,

$$V_{Lm,DISO} = V_{pv} - V_{C1}. \tag{10}$$

When switch S_4 is turned off, referred to in Figure 10d, the energy stored in both inductors L_1 and L_m will be released to the load. The voltage across L_1 can be expressed as follows:

$$V_{L1,DISO} = V_{bus} + nV_{Lm,DISO} = V_{bus} + n\left(V_{pv} - V_{C1}\right). \tag{11}$$

Then, based on VSBC, the voltage gain of the converter while operating in DISO mode, M_{DISO}, is therefore found as:

$$M_{DISO} = \frac{V_{bus}}{V_{pv} + V_{bat}} = \frac{2nV_{pv}D_{sw1}(1 - D_{sw4}) + V_{bat}D_{sw4}(1 - 2D_{sw1})}{\left(V_{pv} + V_{bat}\right)(1 - 2D_{sw1})(1 - D_{sw4})}. \tag{12}$$

In (12), it can be observed that both duty cycles of S_1 and S_4 dominate the voltage gain in DISO mode. Figure 17 indicates the relationship between M_{DISO}, D_{sw1}, and D_{sw4}.

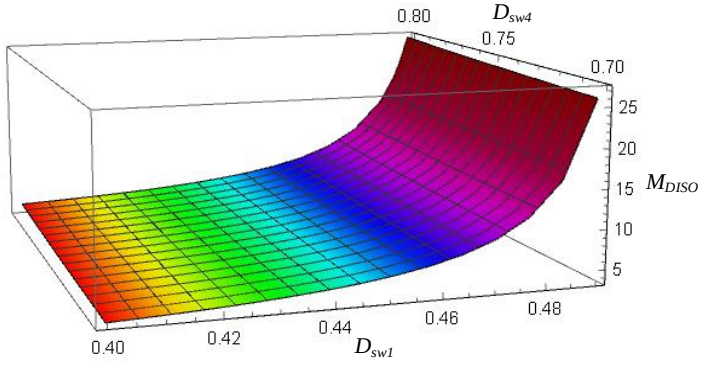


Figure 17. The relationship between M_{DISO}, D_{sw1}, and D_{sw4}.

3.1.4. Derivation for SIDO Mode

For the derivation of the voltage gain in SIDO, Figure 12a is referred to, in which the switches S_1, S_2 and S_3 are ON. The magnetizing inductor L_m stores energy from the PV panels V_{PV} and the capacitor C_1. The PV panels and the capacitor C_1 also supply power to inductor L_1 and the load R_o through the transformer. Therefore, the following relationships hold:

$$V_{Lm,SIDO} = V_{pv} + V_{C1}. \tag{13}$$

$$V_{L1,SIDO} = nV_{Lm,SIDO} = n(V_{pv} + V_{C1}) = V_{bus}. \tag{14}$$

When switches S_1 and S_2 are turned off, as shown in Figure 10c, the energy of the magnetizing inductor L_m is released to capacitor C_1. Inductor L_1 will charge the battery V_{bat}. Accordingly,

$$V_{Lm,SIDO} = V_{pv} - V_{C1}. \tag{15}$$

$$V_{L1,SIDO} = -V_{bat}. \tag{16}$$

With VSBC, the voltage gain is concluded as:

$$M_{SIDO} = \frac{V_{bat}}{V_{pv}} = \frac{2nD_{sw3}(1 - D_{sw1})}{(1 - 2D_{sw1})(1 - D_{sw3})}. \tag{17}$$

Figure 18 indicates the voltage gain M_{SIDO} versus duty cycles D_{sw1} and D_{sw3}.

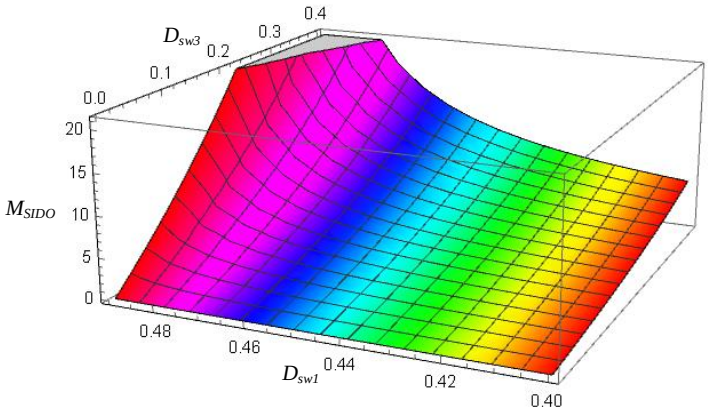


Figure 18. Voltage gain M_{SIDO} of the SIDO mode versus duty cycle D_{sw1} and D_{sw3}.

3.1.5. Derivation for BF Mode

In BF mode, since the energy is reversely drawn from the DC bus to charge the battery, the voltage gain becomes the ratio of V_{bat} to V_{bus}. Referring to Figure 14a, it can be found that because the switch S_5 is closed, the voltage across the inductor L_1 is equal to the bus voltage. That is,

$$V_{L1,BF} = V_{bus}. \tag{18}$$

After switch S_5 is turned off, as shown in Figure 14b, the energy stored in inductor L_1 is released to charge the battery. That is,

$$V_{L1,BF} = -V_{bat}. \tag{19}$$

The circuit behavior of the BF mode resembles that of a buck converter. Applying VSBC to the durations of switch-ON and switch-OFF can yield

$$M_{BF} = \frac{V_{bat}}{V_{bus}} = \frac{D_{sw5}}{1 - D_{sw5}}, \tag{20}$$

in which the M_{BF} and D_{sw5} indicate the voltage gain of BF mode and duty cycle of switch S_5. Figure 19 depicts this voltage gain versus its related switch cycle.

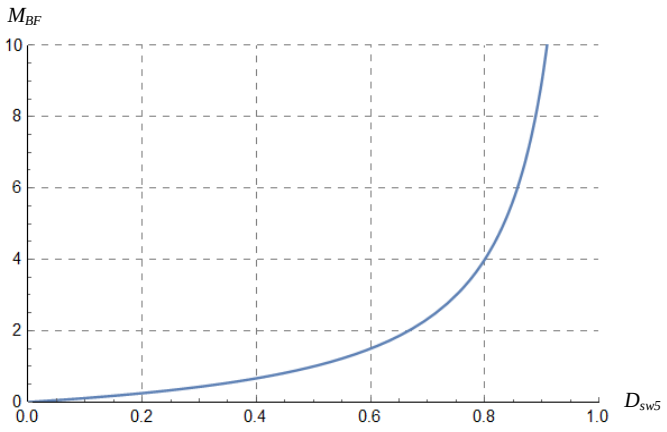


Figure 19. Voltage gain M_{BF} of the BF mode versus duty cycle D_{sw5}.

To clarify the voltage gain of the converter in different modes, Table 1 summarizes the expression of $M_{SISO\text{-}PV}$, $M_{SISO\text{-}battery}$, M_{DISO}, M_{SIDO}, and M_{BF}.

Table 1. Voltage gains of the proposed converter in different modes.

Mode	Voltage Gain
SISO-PV mode	$M_{SISO-PV} = \frac{V_{bus}}{V_{pv}} = \frac{2nD_{sw1}}{1-2D_{sw1}}$
SISO-battery mode	$M_{SISO-Battery} = \frac{V_{bus}}{V_{bat}} = \frac{D_{sw4}}{1-D_{sw4}}$
DISO mode	$M_{DISO} = \frac{V_{bus}}{V_{pv}+V_{bat}} = \frac{2nV_{pv}D_{sw1}(1-D_{sw4})+V_{bat}D_{sw4}(1-2D_{sw1})}{(V_{pv}+V_{bat})(1-2D_{sw1})(1-D_{sw4})}$
SIDO mode	$M_{SIDO} = \frac{V_{bat}}{V_{pv}} = \frac{2nD_{sw3}(1-D_{sw1})}{(1-2D_{sw1})(1-D_{sw3})}$
BF mode	$M_{BF} = \frac{V_{bat}}{V_{bus}} = \frac{D_{sw5}}{1-D_{sw5}}$

3.2. Voltage Stresses on the Semiconductors

All semiconductor devices will sustain different levels of voltage and current in different operation modes. The maximum sustained voltage and current among the five modes should be treated as the power rating of a selected semiconductor device. In the following, the estimation of the maximum voltage stress for all semiconductor devices is first carried out, followed by the determination of the maximum current stress in the next subsection.

The S_1, S_2, D_1, and D_2 in the power stage will block the same voltage in the modes of SISO-PV, DISO, and SIDO. This blocking voltage is higher than that in the other modes of the converter. Therefore, to calculate the voltage rating of S_1, S_2, D_1, and D_2, one of the SISO-PV, DISO, and SIDO modes will be considered. According to Figure 6, the blocking voltage is equal to the voltage across C_1. Therefore,

$$V_{S1,stress} = V_{S2,stress} = V_{D1,stress} = V_{D2,stress} = V_{C1} = \frac{V_{pv}}{1-2D_{sw1}}. \quad (21)$$

The switch S_3 will block a maximum voltage in DISO mode and SIDO mode as well. From the equivalent stage in Figure 12b, this blocking voltage is calculated and given below:

$$V_{S3,stress} = n(V_{pv} + V_{C1}) + V_{bat} = nV_{pv}\left(1 + \frac{1}{1-2D_{sw1}}\right) + V_{bat}. \quad (22)$$

Considering S_4 and S_5, both switches have the highest voltage stress in DISO mode. The voltage stresses of S_5 and S_4 can be determined in Figure 10a,c, respectively. Both voltage stresses are the same and can be given as

$$V_{S4,stress} = V_{S5,stress} = V_{bus} + V_{bat}. \quad (23)$$

To determine the voltage stress of diode D_3, SIDO mode is considered and the equivalent stage in Figure 12c is utilized, from which it can be concluded that

$$V_{D3,stress} = n(V_{pv} + V_{C1}) = n(V_{pv} + \frac{V_{pv}}{1-2D_{sw1}}). \quad (24)$$

The rest of the voltage-stress determination of the semiconductor component is for diodes D_4 and D_5. Diodes D_4 and D_5 endure the same maximum voltage in DISO mode. From Figure 10a, the voltage stresses of both diodes can be found as

$$V_{D4,stress} = V_{D5,stress} = V_{bus}. \quad (25)$$

3.3. Current Stresses on the Semiconductors

The semiconductor devices, S_1, S_2, D_1, and D_2, identically undergo maximum current stress in SISO-PV mode. Therefore, from Figure 6a, the current stresses of S_1 and S_2 can be derived as

$$I_{S1,stress} = I_{S2,stress} = \frac{n}{1-2D_{sw1}} I_o. \tag{26}$$

In addition, from Figure 6b, it can be found that the current flowing through the switches S_1 and S_2 will pass the diodes of D_1 and D_2. Therefore, the current stresses of D_1 and D_2 can be expressed as

$$I_{D1,stress} = I_{D2,stress} = \frac{n}{1-2D_{sw1}} I_o. \tag{27}$$

The current stresses of S_3, S_4, S_5, and diode D_5 can be determined in SIDO mode, in which these components will endure the highest current stresses. As Figure 12a is referred to, the current stresses of S_3, S_5, and D_5 can be calculated as

$$I_{S3,stress} = I_{S5,stress} = I_{D5,stress} = \frac{-1+2D_{sw1}-3D_{sw3}+2D_{sw3}^2}{(-2+2D_{sw1})D_{sw3}} I_o. \tag{28}$$

While referring to Figure 12b, it can be found that the switch S_4 endures the same current as that of switch S_5

$$I_{S4,stress} = \frac{-1+2D_{sw1}-3D_{sw3}+2D_{sw3}^2}{(-2+2D_{sw1})D_{sw3}} I_o. \tag{29}$$

The remaining part of the current-stress determination is for diodes D_3 and D_4. For diode D_3, SISO-PV mode is applied. Based on Figure 6b, the current stress of diode D_3 can be accordingly calculated and given as

$$I_{D3,stress} = \frac{1}{1-D_{sw1}} I_o. \tag{30}$$

Meanwhile, DISO mode is applied and then, the current stress of diodes D_4 can be obtained. According to Figure 10d, this current stress is given below:

$$I_{D4,stress} = \frac{nD_{sw4}}{1-2D_{sw1}} I_o. \tag{31}$$

3.4. Inductance Design

There are two magnetic devices utilized in the MPMDC, which are L_1 and T_r. The inductance of L_1 and the magnetizing inductance of L_m both have to be in good design for achieving better features of converter operation. The T_r will be used in SISO-PV, DISO, and SIDO modes, among which the SISO-PV is the major mode for the design of T_r. That is, the L_m in T_r will carry the largest amount of current among all converter modes. Therefore, the inductance design of L_m is based on SISO-PV mode. To ensure that the L_m can be in continuous conduction mode (CCM) over all the five converter modes, the minimum of the magnetizing current, $i_{Lm,min}$, is therefore estimated and expressed as

$$i_{Lm,\min} = I_{Lm,avg} - \frac{\Delta i_{Lm}}{2} = \frac{nI_o}{1-2D_{sw1}} - \frac{V_{pv}D_{sw1}}{2L_m f_s}. \tag{32}$$

At the boundary conduction mode (BCM), $i_{Lm,min}$ is set to be zero. Accordingly, the designed inductance of L_m has to be greater than the minimum inductance $L_{m,min}$ for CCM operation. The $L_{m,min}$ will be calculated as follows:

$$L_{m,\min} = \frac{(1 - D_{sw1})(1 - 2D_{sw1})R_o}{2n^2 f_s}. \tag{33}$$

For L_1 design, it will be used in the modes of SISO-battery, DISO, SIDO, and BF. The SISO-battery mode is the major mode because the L_1 will carry the largest amount of current in this mode. The minimum current of L_1, i_{L1}, can be derived as

$$i_{L1,\min} = I_{L1,avg} - \frac{\Delta i_{L1}}{2} = \frac{V_{bat} D_{sw4}}{R(1 - D_{sw4})^2} - \frac{V_{bat} D_{sw4} T}{2L_1}. \tag{34}$$

At boundary condition, the $i_{L1,\,min}$ is equal to zero. Then, calculating with (34) will yield the minimum value of L_1, $L_{1,min}$, to ensure the converter can be in CCM operation.

$$L_{1,\min} = \frac{(1 - D_{sw4})^2 R_o}{2f_s}. \tag{35}$$

3.5. Capacitance Design

How large the value of capacitance will affect the voltage fluctuation on a capacitor. The voltage variation of capacitor C_1, denoted as ΔV_{C1}, is determined by capacitor current i_{C1}, switching frequency f_s, and its capacitance. That is,

$$\Delta V_{C1} = \frac{i_{C1} \Delta t}{C_1}, \tag{36}$$

in which capacitor current i_{C1} can be estimated by

$$i_{C1} = \frac{1 - 2D_{sw1}}{2nD_{sw1}} I_o. \tag{37}$$

Therefore, the capacitance C_1 can be obtained as

$$C_1 = \frac{(1 - 2D_{sw1}) I_o}{2nD_{sw1} \Delta V_{C1} f_s}. \tag{38}$$

From the above relationship, it can be realized that the smaller ΔV_{C1} is required, the higher capacitance C_1 must be adopted. In addition, switch duty ratio D_{sw1}, switching frequency f_s, and the output current I_o will also influence the determination of the capacitance.

As for the other capacitor C_o, voltage fluctuation on it can be expressed as

$$\Delta V_{Co} = \frac{i_{Co} \Delta t}{C_o}. \tag{39}$$

Since the i_{Co} is equal to the output current I_o, capacitance C_o can thus be expressed as

$$C_o = \frac{I_o D_{sw1}}{\Delta V_{Co} f_s}. \tag{40}$$

The above relationship reveals that the capacitance C_o is inversely proportional to the voltage fluctuation on the output capacitor, ΔV_{Co}. In addition, output current I_o, the duty ratio of switch S_1, and switching frequency f_s will also dominate the determination of C_o, which is the same as the estimation of C_1.

4. Experimental Results

To verify the feasibility of the proposed MPMDC, a 200-W prototype is built and then tested. Figure 20 is the photograph of the prototype. The associated parameters and circuit components used in the main power stage are summarized in Table 2. In converter control, all the parameters at the terminals of the converter are detected to determine which operation mode will be selected, as illustrated in Figure 21. Then, associated sub-control blocks are called for to determine control signals for the corresponding operation of a selected mode. There are three sub-control blocks, as shown in Figure 22, which are the sub-control block of PV power injection (SCPVPJ), the sub-control block of battery discharge (SCBD), and the sub-control block of battery charge (SCBC). The SCPVPJ is in charge of the control of drawing PV power with maximum power point tracking (MPPT) and then, exports the PV power to output by controlling the active switches S_1 and S_2. The SCBD is responsible for the determination of the control signals for switches S_4 and S_5 so that the proposed converter can perform battery discharging. Meanwhile, the SCBC is for switches S_3, S_4 and S_5 to fulfill the battery charging of the converter.

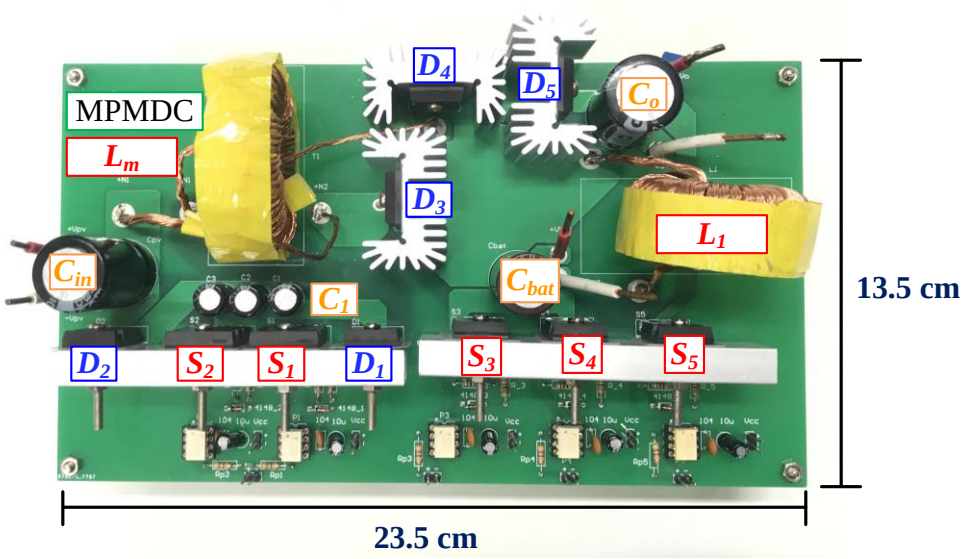


Figure 20. The photograph of the proposed converter.

Table 2. Circuit parameters and components used in the prototype.

Parameters	Values & Specifications
P_{bus} (DC-bus power)	200 W
P_{bat} (Battery power)	50 W
V_{bus} (DC-bus voltage)	200 V
V_{pv} (PV voltage)	24 V
V_{bat} (Battery voltage)	48 V
f_s (Switch frequency)	50 kHz
L_1 (Inductance)	300 µH
L_m (Magnetizing inductance)	270 µH
L_k (Leakage inductance)	3.6 µH
S_1 and S_2 (Power MOSFET)	IXTK90N25L2 (250 V/90 A)
S_3, S_4 and S_5 (Power MOSFET)	IXFH36N50P (500 V/36 A)
D_1 and D_2 (Diodes)	DSSK 60-02A (200 V/2 × 30 A)
D_3, D_4 and D_5 (Diodes)	DPG60C300HB (300 V/2 × 30 A)
C_1 (Electrolytic capacitor)	3 × 10 µF
C_o (Electrolytic capacitor)	100 µF
C_{bat} (Electrolytic capacitor)	68 µF
n (Transformer turns ratio)	43:65

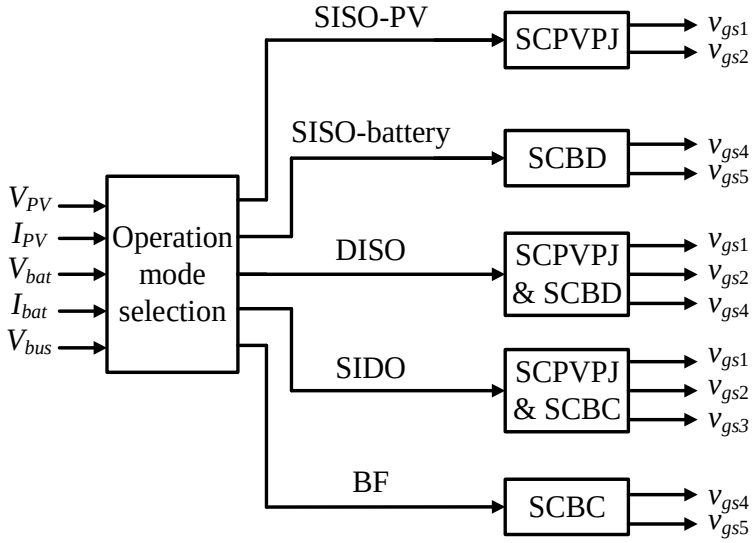


Figure 21. The main control block of the converter.

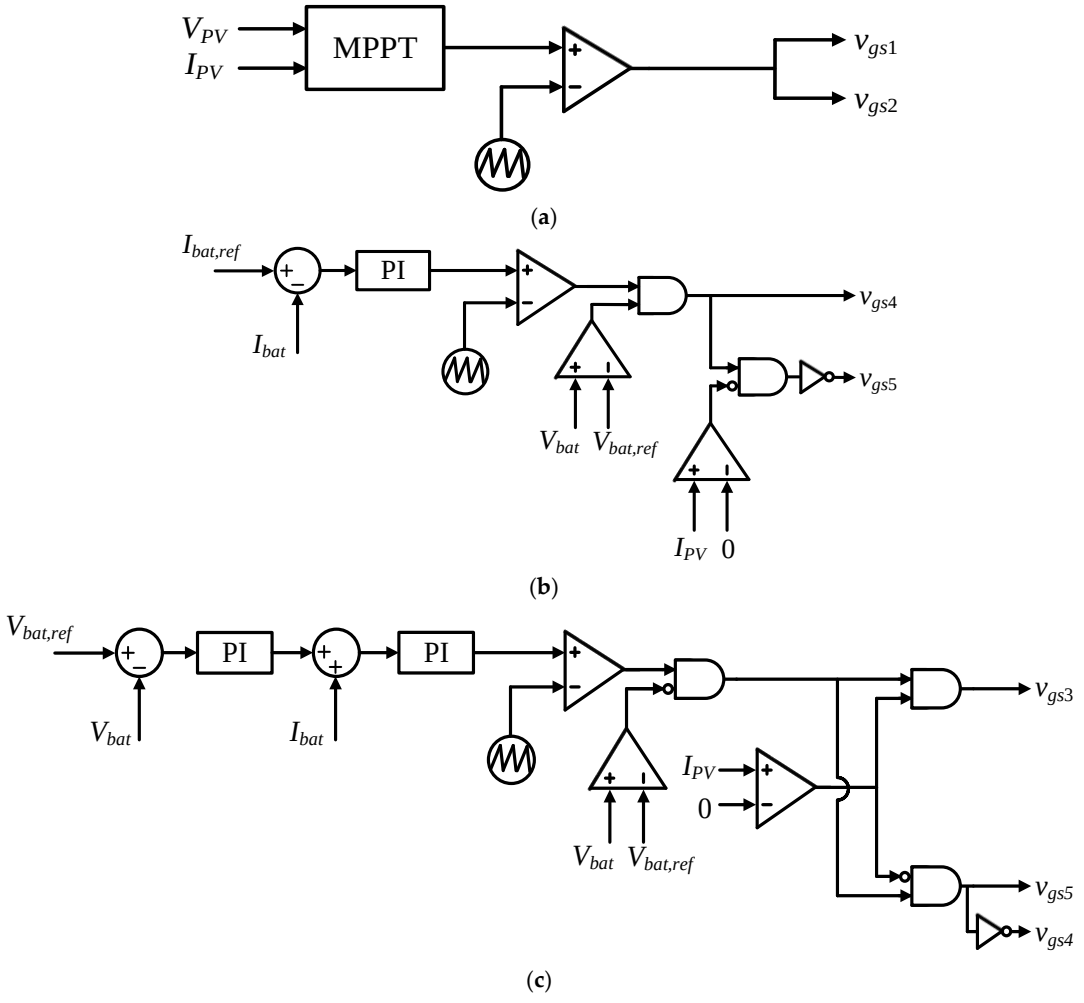


Figure 22. The three sub-control blocks of the converter: (**a**) SCPVPJ, (**b**) SCBD, and (**c**) SCBC.

4.1. SISO-PV Mode

While the MPMDC works in SISO-PV mode and at full load, Figure 23 shows associated experimental measurements. Figure 23a is the switch voltage of S_1 and S_2, along with the corresponding control signals, in which the blocking voltage of both switches is around

160 V. Figure 23b is the measured current waveform of switches S_1 and S_2. The current waveform reveals that the average current of both switches is about 9.92 A, which is close to the theoretical result of 9.87 A calculated from (26). The leakage current is illustrated in Figure 23c. In addition, the average current of diodes D_1 and D_2 is presented in Figure 23d, which is calculated as 9.89 A, and this value approaches the theoretical estimation of (27). Similarly, the measured current of D_3 is given in Figure 23e, and its average is about 1.77 A, which meets the calculating result from (30).

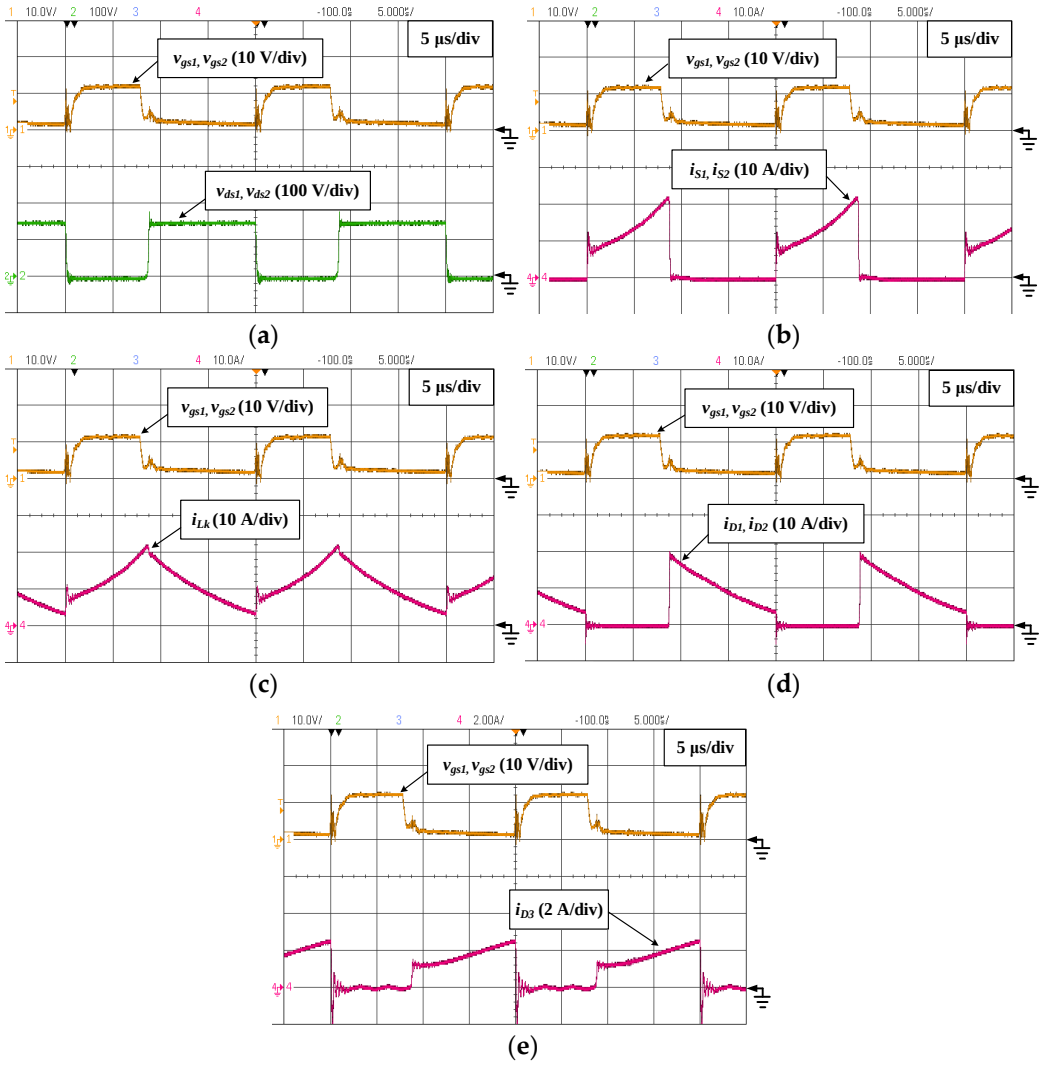


Figure 23. Measured waveforms of the MPMDC in SISO-PV mode: (**a**) switch voltages of S_1 and S_2; (**b**) switch currents of S_1 and S_2; (**c**) leakage-inductance current; (**d**) diode currents of D_1 and D_2; and (**e**) diode current of D_3.

4.2. SISO-Battery Mode

While the MPMDC works in SISO-Battery mode and at full load, Figure 24 shows the associated experimental measurements. Figure 24a is the switch voltage of S_4, along with the corresponding control signal, in which the blocking voltage of the switch is around 200 V. Figure 24b is the measured current waveform of switches S_4. This current waveform reveals that the average current of both switches is about 5.34 A. The inductor current i_{L1} is illustrated in Figure 24c. In addition, from Figure 24d, since the switch current i_{S5} is negative, the switch S_5 can be worked as a synchronous switch. In SISO-battery mode, the practical average current of S_5 is around 5.31 A.

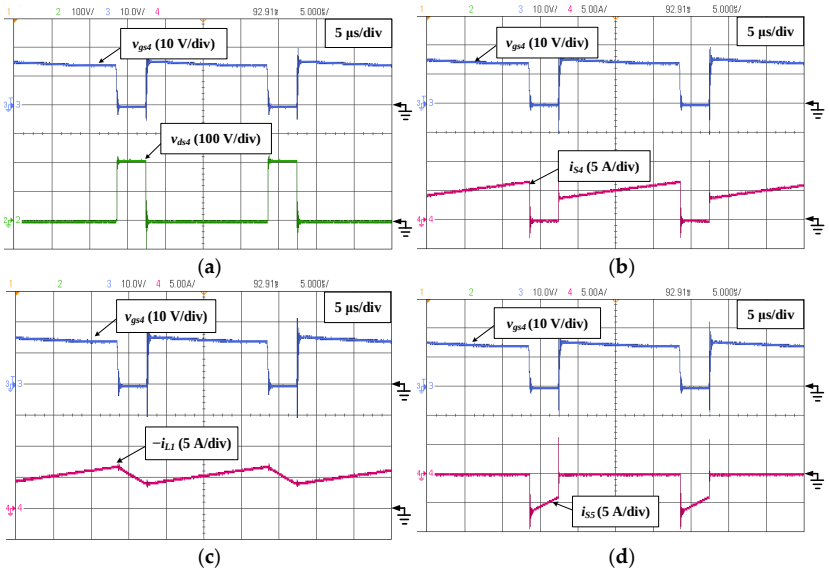


Figure 24. Measured waveforms of the MPMDC in SISO-Battery mode: (**a**) switch voltage of S_4; (**b**) switch current of S_4; (**c**) inductor current of L_1; and (**d**) switch current of S_5.

4.3. DISO Mode

To demonstrate the converter in DISO-mode operation, associated key measurements at full load are illustrated in Figure 25. Figure 25a is the switch current of S_4 and its control signal, in which the switch current is measured to be around 3.02 A. In Figure 25b, the inductor current i_{L1} increases or decreases linearly, which verifies that the voltage across inductor L_1 can be invariable during the periods of switch ON and switch OFF. That is, the capacitances adopted in the converter are valid for constant-voltage sustaining. Additionally, the i_{L1} is negative, which proves that battery energy can be fed to the DC-bus. The diode currents of D_1 and D_2 are shown in Figure 25c, the average of which is measured as 4.23 A. This value is lower than that in Figure 25d, which confirms that the diodes D_1 and D_2 endure a maximum current in SISO-PV mode. The measured current of D_4 is also given in Figure 25d, and its average is about 3.11 A, which meets the calculating result from (31).

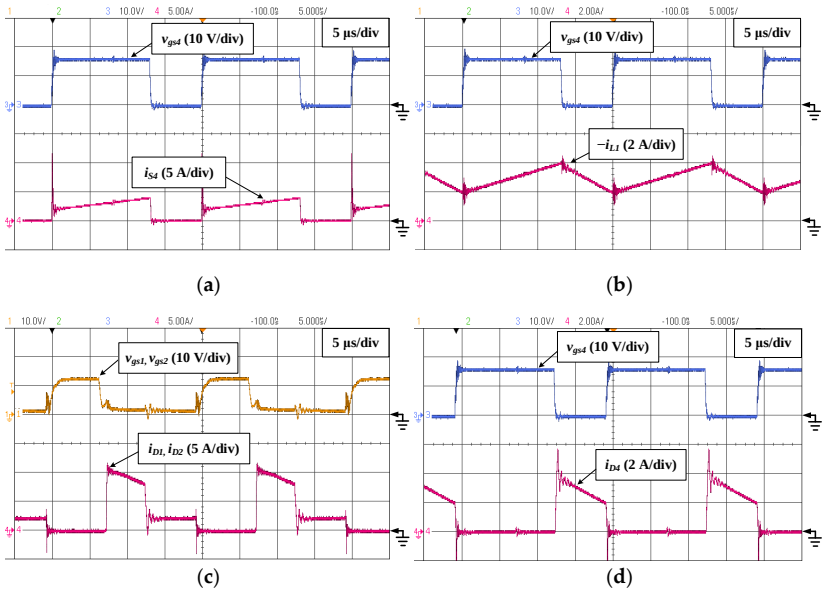
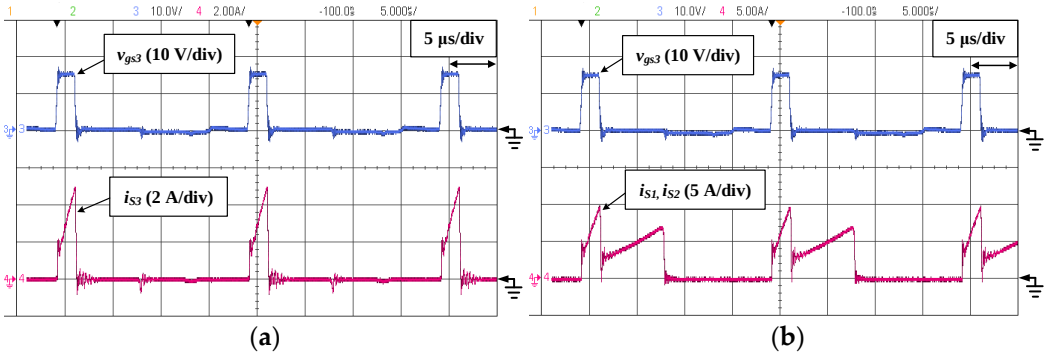


Figure 25. Measured waveforms of the MPMDC in DISO mode: (**a**) switch current of S_4; (**b**) inductor current of L_1; (**c**) diode currents of D_1 and D_2; and (**d**) diode current of D_4.

4.4. SIDO Mode

As for working in SIDO mode, Figure 26 is the related measurement of switch currents at full load. Figure 26a shows the switch current of S_3, from which it can be calculated that the average of this current is 3.21 A. This value is close to the theoretical estimation of 2.98 A according to (28). Figure 26b is the measured current waveform of S_1 and S_2, which reveals that the peak current of both switches is less than 10 A.

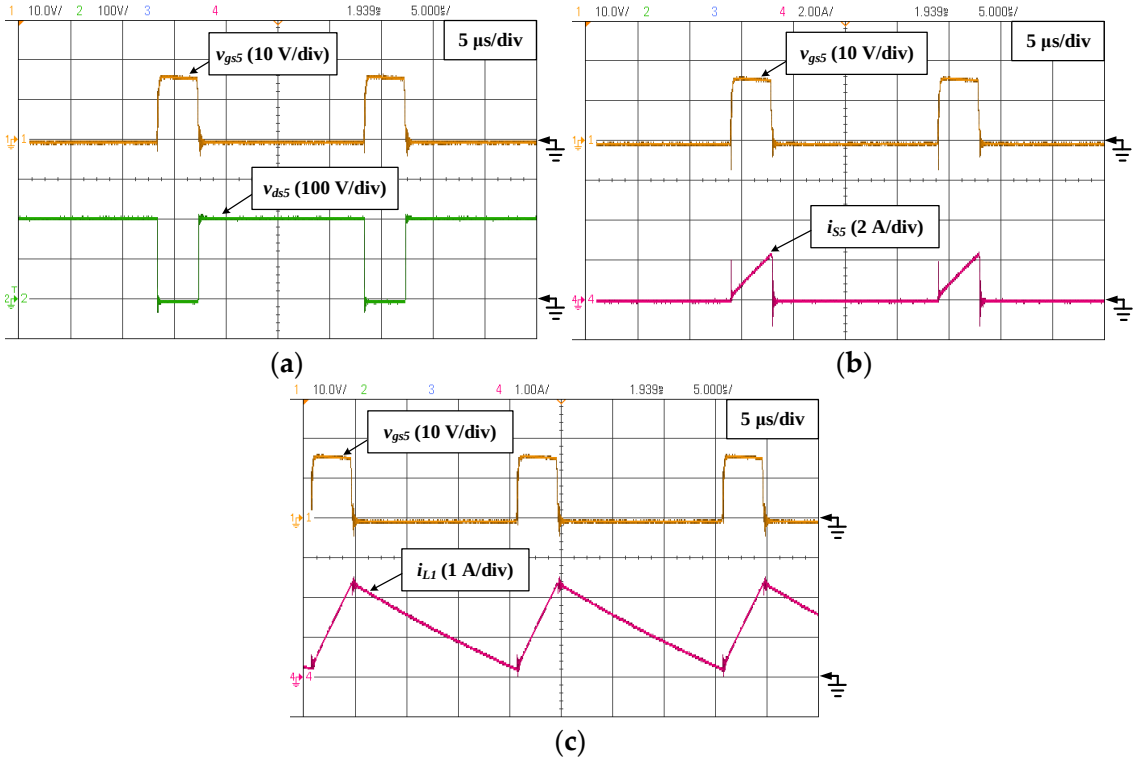


(**a**) (**b**)

Figure 26. Measured waveforms of the MPMDC in SIDO mode: (**a**) switch current of S_3; and (**b**) switch currents of S_1 and S_2.

4.5. BF Mode

While in BF mode, Figure 27 illustrates the experimental voltage and current waveforms. The switch S_5 serves as the main switch, and its voltage along with the control signal is shown in Figure 27a. Meanwhile, Figure 27b is the measured current waveform of S_5, according to which the average current of S_5 can be found and about 1.22 A. The inductor current i_{L1} is also measured and presented in Figure 27c, observed from which this current is always positive. That is, the DC bus charges the battery in this mode.



(**a**) (**b**) (**c**)

Figure 27. Measured waveforms of the MPMDC in BF mode: (**a**) switch voltage of S_5; (**b**) switch current of S_5; (**c**) inductor current of L_1.

As for the demonstration of a sudden change from an operation mode to another mode, the mode change from SISO-battery to DISO is carried out and the voltages of DC bus, PV panels, and battery are measured, which are shown in Figure 28. In this case, the DC-bus requires a specific power of 200 W, and at the beginning, the battery supplies this 200-W loading. Then, PV panels begin to inject energy into the DC bus to share the power supply and will provide half of the load at the end. Accordingly, the providing power of the battery will drop to 100 W. Figure 28 illustrates that the converter can achieve system stability over the mode change. Figure 29 depicts the converter efficiency of the prototype from light load to full load. This measurement reveals that the DISO possesses higher efficiency than the other operation modes and its peak efficiency can be up to 94%. The converter efficiency will vary with which operation mode to select and how much power to be dealt with. Among the five operation modes, in terms of average efficiency from light load to full load, the converter will obtain the best efficiency in DISO mode and the worst in SIDO mode. The reason is that conduction losses dominate conversion efficiency. At a specific power, the PV port will carry a still higher current in SIDO than that in DISO, which results in lower efficiency in SIDO. The power budget of the converter in DISO mode and SIDO mode at rated power is illustrated in Figures 30 and 31, respectively, from which it can be observed that switch losses and diode losses will dominate the converter efficiency. In DISO mode, switch losses and diode losses count for 26% and 47%, respectively. Meanwhile, in SIDO mode, count for 37% and 30%, respectively. To improve efficiency, a soft-switching mechanism and power semiconductor devices with better performance and low forward voltage can be considered.

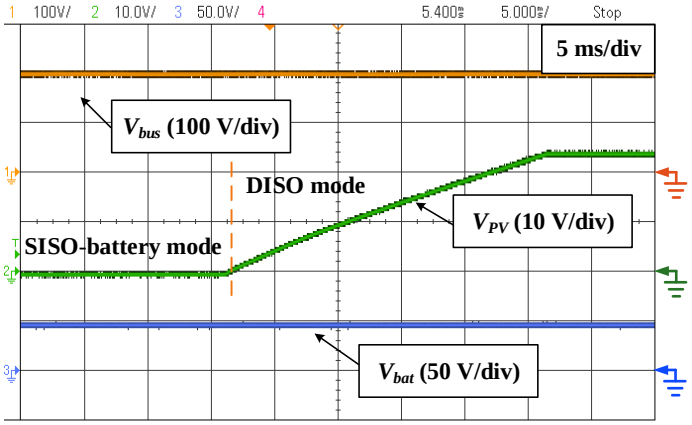


Figure 28. Experimental waveforms to illustrate the mode change of the converter from SISO-battery to DISO.

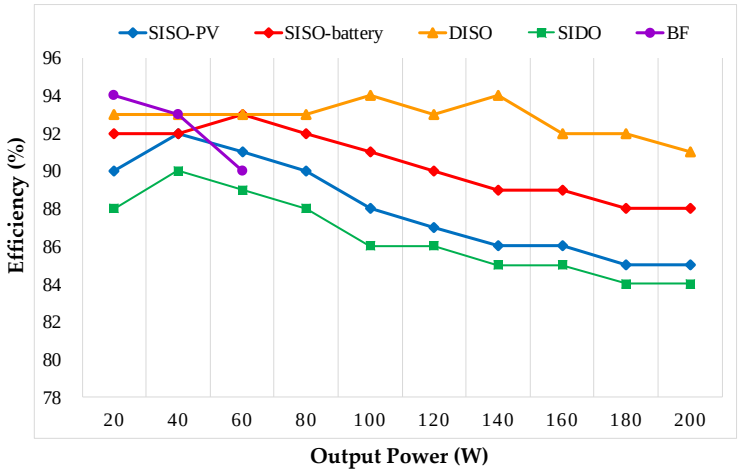


Figure 29. The measured efficiency of the prototype.

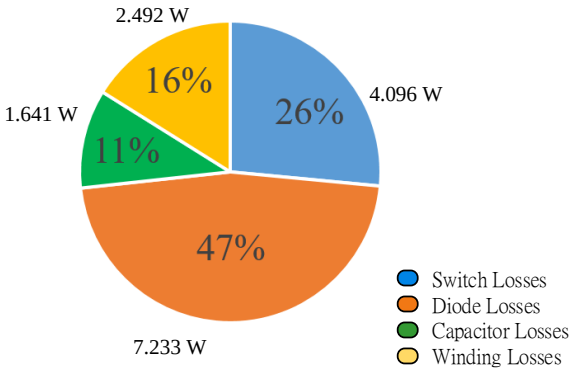


Figure 30. The power budget at rating power while the converter works in DISO mode.

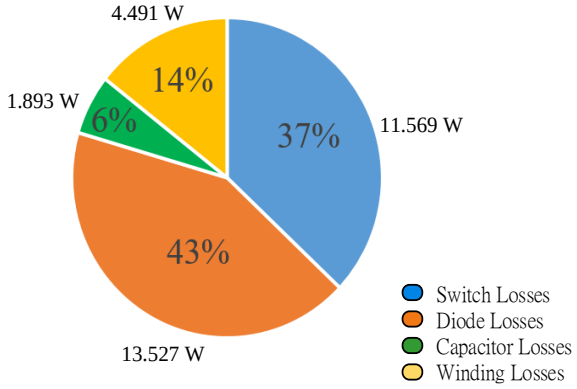


Figure 31. The power budget at rating power while the converter works in SIDO mode.

5. Performance Comparison

The comparison of the proposed converter with other latest isolated three-port converters is summarized in Table 3. The comparison items mainly include the number of power switches, diodes, capacitors, magnetic elements, and operation modes. Besides, the ability of leakage-energy recycling, the turns ratio of the transformer, and converter specification are also listed. Table 3 shows that the obvious advantages of the MPMDC include: the feature of leakage-energy recycling, with the most diverse operation modes, the least number of magnetic components in addition to a minimum number of capacitors required, and no need for a high turn ratio of the transformer. Based on these advantages, the MPMDC is very suitable for green power processing.

Table 3. Performance comparison between the proposed converter and other recently proposed topologies.

Ref.	[21]	[29]	[30]	[31]	Proposed
Input voltage	60 V	30 V	20–40 V	50 V	24 V
Battery voltage	72 V	24 V	60 V	50 V	48 V
Output voltage	200 V	400 V	760 V	100 V	200 V
Rated power	600 W	200 W	500 W	1000 W	200 W
MOSFETs	12	3	6	14	5
Diodes	0	3	4	0	5
Capacitors	3	6	8	1	3
Magnetic elements	5	4	3	2	2
Operational mode	4	3	2	2	5
Turns ratio (n)	2	5	2	2	1.5
Isolation	Yes	Yes	Yes	Yes	Yes
Leakage energy recycling	No	Yes	No	Yes	Yes
Voltage gain (bus voltage)	$V_{pv}\frac{n_2(D_2-D_4)}{1-D_2}+V_{bat}\frac{\frac{n_2}{1-n_1}D_4}{1-D_2}$	$V_{pv}\frac{n}{1-D_1}+V_{bat}\frac{nD'_2}{D_1}$	$\frac{V_{pv}}{D}$ or $6nV_{bat}$	$\frac{nR_L}{2f_s}\left[\frac{V_{dc1}D_{13}(1-D_{13})}{L_{f1}}+\frac{V_{dc1}D_{23}(1-D_{23})}{L_{f2}}\right]$	$V_{pv}\frac{2nD_1}{1-2D_1}+V_{bat}\frac{D_4}{1-D_4}$

6. Conclusions

A multi-port multi-directional converter is proposed, which can accomplish a variety of power flow controls to perfectly function clear-energy management in a single-stage structure. The converter operation modes can be up to five, which surpass other similar converters in power processing. In addition, the proposed converter possesses galvanic isolation and can achieve a high voltage-conversion ratio even only utilizing an inductor and a transformer. The energy stored in the leakage inductance of the transform can be recycled. To demonstrate the feasibility and verify the theoretical analysis of the converter, a 200-W prototype is built and then tested. From the measurements, it is confirmed that all the practical results can be consistent with the theoretical discussion and the converter is very suitable to deal with various clean-energy sources. At full-load conditions, the conversion efficiency of the converter in SISO-PV, SISO-battery, DISO, SIDO, and SISO are 85%, 88%, 91%, 84%, and 90%, respectively.

Author Contributions: Conceptualization, C.-L.S. and L.-Z.C.; methodology, G.-Y.C.; validation, C.-M.Y. and L.-Z.C.; formal analysis, L.-Z.C., G.-Y.C. and C.-M.Y.; investigation, G.-Y.C. and C.-M.Y.; resources, C.-L.S.; writing—original draft preparation, C.-L.S. and L.-Z.C.; writing—review and editing, C.-L.S. and L.-Z.C.; visualization, L.-Z.C.; supervision, C.-L.S.; project administration, L.-Z.C. All authors have read and agreed to the published version of the manuscript.

Funding: This study is supported by the Research Assistantships funded by the Ministry of Science and Technology, Taiwan, under grant number: MOST 110-2622-E-992-019, to C.-L.S.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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