Multi-Step Extended-Counting Analog-to-Digital Converters

C.-H. Chen, Y. Jung, J. L. Ceballos and G. C. Temes

Extended-counting A/D converters are proposed which achieve a high accuracy by performing the conversion in several cycles. During the first cycle, the circuit performs as an incremental ADC, while during the remaining ones it acts as a multi-slope counting converter. With only one opamp and a single-slope ADC, the accuracy is comparable to that of a second-order incremental ADC. A three-step A/D converter using only a single opamp and a two-slope ADC achieves an accuracy comparable to that of a third-order incremental ADC, but with much higher power efficiency.

Introduction: Incremental ADC is useful for high-accuracy conversion of signals at DC or with low bandwidth [1]. To enhance the conversion speed, a higher-order modulator or extended counting may be used [2-4]. In this paper, we propose an incremental ADC with an added single- or multi-slope ADC to perform the extended counting. With only one opamp used, the accuracy is only 1 bit less than that of a second-order incremental ADC requiring 2 or 3 opamps. The conversion speed can be further extended by a third cycle with a reconfigured feedback DAC coefficient. The accuracy of the proposed three-step ADC is comparable to that of a third-order incremental ADC, which needs 3 or 4 opamps. The new circuits save circuit complexity and power, and it is easy to reconfigure them with a simple timing control.

Incremental and Extended-Counting ADCs: Fig. 1 shows a first-order incremental ADC (IADC1) with extended counting and its timing diagram. The IADC1 by itself requires 2^N clock periods to achieve *N*-bit accuracy, which is usually too long. To reduce the conversion time, a higher-order modulator may be used. Alternatively, an additional ADC can be used to sample the residue voltage before resetting the integrator [2] [3], and perform *extended counting* (Fig. 1).

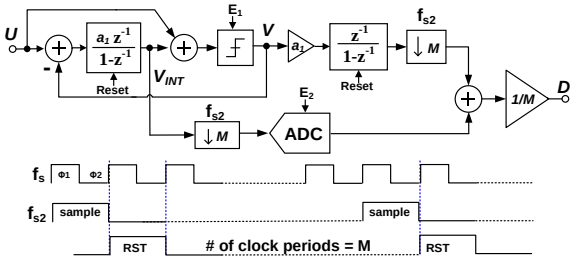


Fig. 1 *A 1st-order incremental ADC with extended-counting*

The Proposed Extended-Counting ADC with a Single-Slope ADC: Fig. 2 shows the proposed IADC1 using a single-slope ADC to perform the extended-counting. During the first M_1 clock periods, the circuit is configured as a IADC1 as shown on Fig. 3(a), and the feedback DAC capacitor C_{DAC} is equal to C_F. The internal quantizer can be multi-level in order to lower the integrator's output swing and have a wide non-overloaded range. After the M_1 [th] clock period, the residue voltage is held by the integrator (V_{INT}). Now the IADC1 is re-configured as a single-slope ADC, as shown on Fig. 3(b). The feedback DAC capacitor C_{DAC} is now reconfigured as $C_F/(M_2-1)$, so the integration coefficient is $1/(M_2\text{-}1)$. After M_2 clock periods, $|V_{INT}| < V_{FS}/(M_2-1)$. Hence, the input voltage can be estimated from eq.(1), and the transfer function of the decimation filter is given by the right-hand-side of (1). Here, V_1 and V_2 are the loop outputs during the first and second cycles, respectively. The quantization error can be estimated from eq. (2):

$$\overline{V_{IN}} \approx \frac{1}{M_1-1}\left[\sum_{i=1}^{M_1-1} V_1[i] - \frac{1}{M_2-1}\sum_{j=1}^{M_2-1} V_2[j]\right] \qquad (1)$$

$$E_{ADC} \le \frac{V_{FS}}{(M_1-1)(M_2-1)};\ \ ENOB \approx log_2(M_1 \cdot M_2) \qquad (2)$$

If the two steps are assigned the same number of clock periods ($M/2$), then the quantization error is around $V_{FS} \cdot 2^2/M^2$. The error is only one bit more than that of a 2nd-order IADC. In the system of Fig.1 only one opamp is required, and thus it has improved power efficiency.

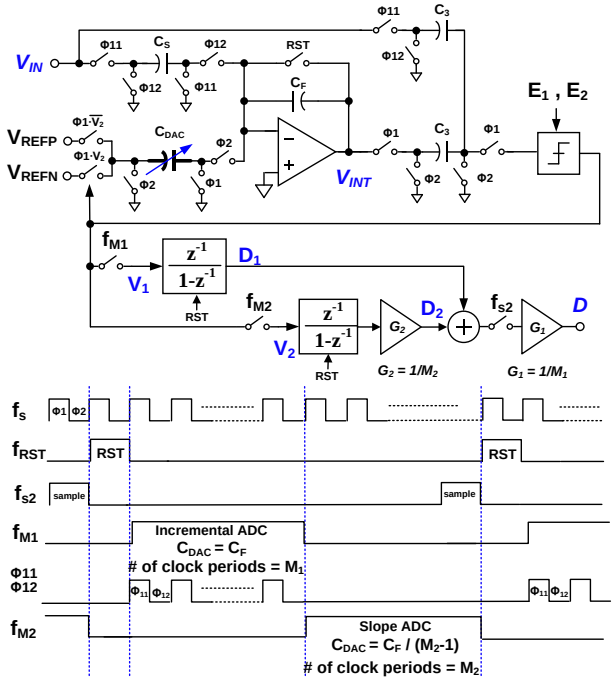
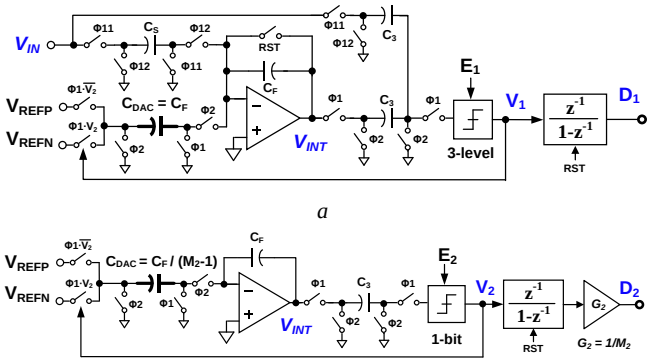


Fig. 2 *The proposed incremental ADC with a single-slope ADC performing the extended counting.*



a

b

Fig. 3 *Operation of the proposed extended-counting incremental ADC.*
a IADC operation during the first M_1 clock periods.
b Extended counting during the next M_2 clock periods. .

The Proposed Extended-Counting ADC with a Multi-Step ADC: The extended-counting operation can also be performed by a multi-step slope ADC. The total number of clock periods *M* is then divided into three parts: IADC operation (M_1clock periods); coarse single-slope A/D conversion (M_2 clock periods); and fine single-slope A/D conversion (M_3 clock periods). Fig. 4 shows the circuit schematic and its timing diagram. The first and second steps are the same as for the extended-counting ADC of Fig.2. During the third step, the feedback DAC capacitor C_2 is reconfigured to realize an integrator coefficient of $1/[(M_2-1)(M_3-1)]$. The estimate of the input voltage is given in (3), and the quantization error estimate in (4):

$$\overline{V_{IN}} \approx \frac{1}{M_1-1}\left[\sum_{i=1}^{M_1-1} V_1[i] - \sum_{j=1}^{M_2-1}\frac{V_2[j]}{M_2-1} - \sum_{k=1}^{M_3-1}\frac{V_3[k]}{(M_2-1)(M_3-1)}\right] \qquad (3)$$

$$E_{ADC} \le \frac{V_{FS}}{(M_1-1)(M_2-1)(M_3-1)};\ ENOB \approx log_2(M_1 \cdot M_2 \cdot M_3) \qquad (4)$$

If the three steps are assigned the same number of clock periods ($M/3$), the quantization error is around $V_{FS} \cdot 3^3/M^3$. The accuracy of the proposed ADC is thus comparable to that of a third-order IADC. However, it needs only one opamp. As can be seen from equations (3) and (4), by changing the number of clock periods assigned to each step, the SQNR performance can be changed. To realize the small coefficient of the feedback DAC during the third step, it can be implemented in a number of ways: (1) a resistor ladder may be used to derive the references V_{REFP} and V_{REFN}. (2) a capacitive T-network or ladder may be used [4]. (3) a combination of the capacitive T-network and the resistor ladder can be implemented.

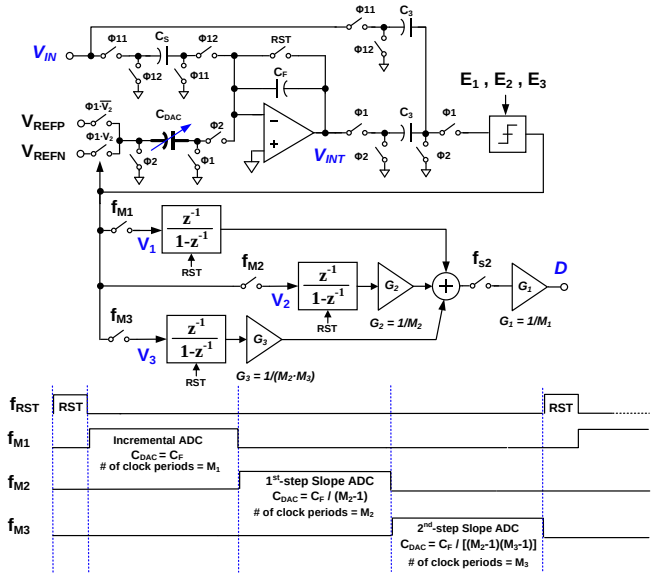


Fig. 4 *Proposed incremental ADC with a 2-step single-slope ADC to perform extended-counting. ϕ_{11}, ϕ_{12} and f_{s2} are as same as shown on Fig. 3.*

Simulation Results: The two proposed ADCs were simulated for a signal bandwidth of 40 Hz sampled at 8 kHz frequency. Within each conversion cycle, the equivalent oversampling ratio (OSR) was 100 (corresponding to 100 clock periods). The simulated PSDs with -3 dBFS signal amplitude are shown on Fig. 5. For the extended-counting single-slope ADC, 50 of the 100 clock periods were assigned to both the IADC and extended-counting operations. The resulting simulated accuracy was 11 bits (5.5-bits/step). For the extended counting ADC with twp-step residue cancellation 96 clock periods were divided equally among the three steps (OSR=32). The simulated accuracy was then 15 bits (5-bits/step). With the same OSR, the accuracy of a 2nd-order IADC is 12 bits, and that of a 3rd-order IADC is 17 bits. The two proposed multi-step ADCs can thus achieve high accuracy, comparable to that of 2nd- and 3rd-order IADCs, but with much less power consumption.

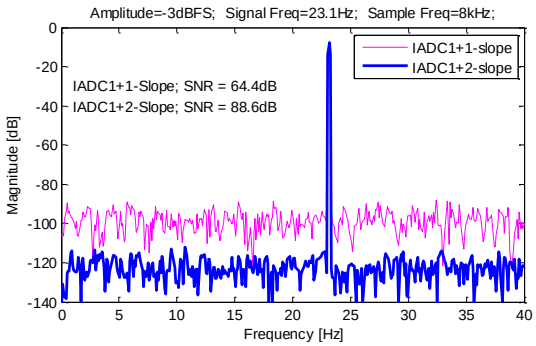


Fig. 5 *Simulated PSD with a -3 dBFS signal amplitude.*

Conclusions: Incremental ADCs with extended counting, using single- or dual-slope residue cancellation, were proposed. The design equations show, and simulations confirm that the proposed extended-counting ADC with only one opamp can achieve accuracy comparable to a second-order IADC if single-slope residue cancellation is used. The dual-slope ADC achieves accuracy comparable to a third-order IADC. The proposed ADCs are very power efficient. They can also be easily reconfigured with simple timing control.

Acknowledgement: This work was supported by Infineon Technologies.

C.-H. Chen, J. Jung and G. C. Temes (School of EECS, Oregon State University, Corvallis, OR, 97330, USA)
E-mail: chench@eecs.oregonstate.edu
J. L. Ceballos (Infineon Technologies Austria AG, Siemensstrasse 2, 9500 Villach, Austria)
E-mail: joseluis.ceballos@infineon.com

References

1 J. Markus, J. Silva, and G. C. Temes, "Theory and applications of incremental ΔΣ converters," *IEEE Trans. Circuits Syst. I*, vol. 51, pp. 678–690, Apr. 2004.

2 R. Harjani and T. A. Lee, "FRC: A method for extending the resolution of Nyquist rate converters using oversampling," *IEEE Trans. Circuits Syst. II*, vol. 45, no. 4, pp. 482–494, Apr. 1998.

3 P. Rombouts, W. De Wilde, and L. Weyten, "A 13.5-b 1.2-V micropower extended counting A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 2, pp. 176–183, Feb. 2001.

4 R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters: IEEE Press, 2005, p. 307.