Multi-threshold Threshold Logic Circuit Design Using Resonant Tunneling Devices

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Abstract:

This Letter presents a novel and extremely compact circuit topology able to implement a generalized threshold logic function with two thresholds. The circuit consists of resonant tunnelling diodes (RTDs) and heterostructure field effect transistors (HFETs).

Introduction:

Resonant tunneling devices are nowadays considered the most mature type of quantum-effect devices. They are already operating at room temperature and the existence of a III-V large scale integration process allows us to explore novel circuit architectures [1]. Resonant tunneling diodes (RTDs) exhibit a negative differential resistance (NDR) region in their current-voltage characteristics which can be exploited to significantly increase the functionality implemented by a single gate in comparison to MOS and bipolar technologies. In particular, a number of Threshold Gates (TGs) based on RTDs monolitically integrated with three-terminal devices which implement complex logic functions have been fabricated and have demonstrated high speed and robust operation [1].

Threshold gates allow a direct implementation of linearly separable boolean functions: from a geometrical point of view, a TG with n inputs can be seen as an hyperplane cutting the boolean n-cube. It evaluates a function f in the sense that $f^{-1}(1)$ lies on one side of the plane, and $f^{-1}(0)$ on the other. If the boolean function is not linearly separable, a TG network is required to implement it. Multi-threshold threshold gates (MTTGs) are a generalization of the conventional TGs in which k thresholds $(k = 1, 2, \ldots)$ rather than the usual single threshold are used to separate $f^{-1}(1)$ from $f^{-1}(0)$. So, any arbitrary boolean (nonlinearly separable) function can be realized by a single MTTG having a sufficiently large k. Hardware implementation of MTTGs has been studied and some circuits proposed but they have obtained no success to date.

In this paper we propose the use of resonant tunnel diodes to implement multi-threshold threshold gates. We provide detailed analysis on circuit design and simulation of MTTGs using the HSPICE models developed within the LOCOM european project [2] for InP-based RTD and HFET devices which have been extensive and experimentally validated.

Multi-threshold threshold logic:

A threshold gate (TG) is defined as a logic gate with n binary input variables, x_i, $(i = 1, \ldots, n)$, one binay output y, and for which there is a set of $(n + 1)$ real numbers: threshold T and weights $w_1, w_2, \ldots, w_n$, such that its input-output relation is defined as $y = 1$ *iff* $\sum_{i=1}^{n} w_i x_i \geq T$ and $y = 0$ otherwise. Sum and product are the conventional, rather than the logical, operations.

The concept of a threshold gate can be generalized to multi-threshold threshold gates [3] and so, a k-threshold TG is a logic element with n binary input variables, x_i, $(i = 1, \ldots, n)$, one binay output y, and for which there is a set of $(n + k)$ real numbers: thresholds T_i, $(i = 1, \ldots, k)$, and weights $w_1, w_2, \ldots, w_n$, such that its input-out-

put relation is defined as $y = 1$ *iff* $T_{2j-1} \leq \sum_{i=1}^{n} w_i x_i < T_{2j}$, with $T_{j+1} > T_j$, $(j = 1, 2, \ldots, k/2)$ for k being an even number (if k is not an even number, then the last double-sided inequality is simplified to $T_k \leq \sum_{i=1}^{n} w_i x_i$). Output y is equal to zero otherwise. The set of weights and thresholds can be denoted in a more compact vector notation way by $[w_1, w_2, \ldots, w_n; T_1, \ldots, T_k]$.

Operating principle of an MTTG:

Circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE) [4]. The MOBILE is a rising edge triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage (V_{bias}). When V_{bias} is low both RTDs are in the on-state (or low resistance state) and the circuit is monostable. Increasing V_{bias} to a proper maximum value, only the device with the lowest peak current switches (*quenches*) from the on-state to the off-state (the high resistance state). Logic functionality is achieved by embedding an input stage which modifies the peak current of one of the RTDs. There are different options for the implementation of the MOBILE input stage, being the series connection of an RTD with a heterojunction field-effect transistor (HFET) in parallel to the driver (or load) RTD the one selected to increase the fan-in [1]. Figure 1a shows an inverter circuit implemented following this principle. During a critical period when V_{bias} rises, the voltage at the output node V_{out} goes to one of the two stable states (low or high), corresponding to “0” and “1” in binary logic, depending on whether the external input signal V_{in} is “1” or “0” since this determines which NDR device has the lowest current.

Threshold gates implemented with RTDs are based on the same current controlled switching principle of the MOBILE [1]. Figure 1b shows the RTD/HFET implementation of a generic threshold gate defined as $y = 1$ *iff* $w_1x_1 + w_2x_2 - w_3x_3 - w_4x_4 \geq T$,

and 0 otherwise. The RTD areas determine the weigths $w_i, (i = 1, \ldots, 4)$ and the threshold T. Input stages controlled by external inputs are placed in parallel to RTD_2 or RTD_1 depending on whether the associated weight is positive or negative, allowing to modify the peak currents of both RTDs.

The circuit structure we propose for implementing MTTGs extends the concept of RTD/HFET-based MOBILE to a circuit consisting of three or more (depending on the number of thresholds) RTDs in series [5]. The key concept to understand the operation of such circuits is the controlled quenching of their series-connected NDR devices [6]. The RTD is in a low-voltage state before and in a high-voltage state after the quenching. The switching sequence in series-connected RTDs begins always with the RTD with a smallest peak current. If this peak current can be controlled by external inputs, this sequence can be varied and different functions are obtained.

Circuit structure for an MTTG

Figure 2 depicts the proposed circuit topology for a generic MTTG defined by $[w_1, w_2, w_3; T_1, T_2]$, *i.e.*, three inputs and two thresholds. As it has two thresholds, three series-connected RTDs are needed. The specific function implemented by such circuit depends only on the areas of the RTDs if the transistors behave as switches. In order to demonstrate the ability of the controlled quenching of series-connected RTDs to implement such MTTG, we have selected the nonlinearly separable Boolean function $f(x_1, x_2, x_3) = x_1 \oplus x_2 x_3$ which can be expressed as the MTTG $[2, 1, 1; 2, 4]$. The table enclosed in Figure 2 shows the output logic function and the RTD which must be quenched for each input combination in order to obtain the desired functionality. Last column in the table gives the implied area relations among the different RTDs assuming $A_{12} = A_{13} = AJ_1$, $A_{22} = A_{23} = AJ_2$, $A_{11} = 2AJ_1$, and $A_{21} = 2AJ_2$. So, 5 dif-

ferent areas must be considered: areas of RTD_i (A_i, i = 0, 1, 2), and the other two ones before mentioned (AJ_1 and AJ_2). The set of inequalities can be easily solved and a solution with $\{A_0 = 2.2, A_1 = 0.9, A_2 = 1.2\}$ and $\{AJ_1 = 0.5, AJ_2 = 0.3\}$ has been selected taking into account fabrication and robustness considerations. The RTD models have a standard area of $10\mu m^2$ [2], so the actual areas are obtained multiplying by this factor. Figure 3 shows the simulation results for this MTTG. Correct operation is observed for every input combination. In addition, performance has been validated through extensive Monte Carlo simulations of a chain of these gates.

Conclusions

An extremely compact implementation of MTTGs which is based on the concept of controlled switching of series-connected RTDs has been presented. This topology extends even more the functionality of the structures based on the MOBILE principle.

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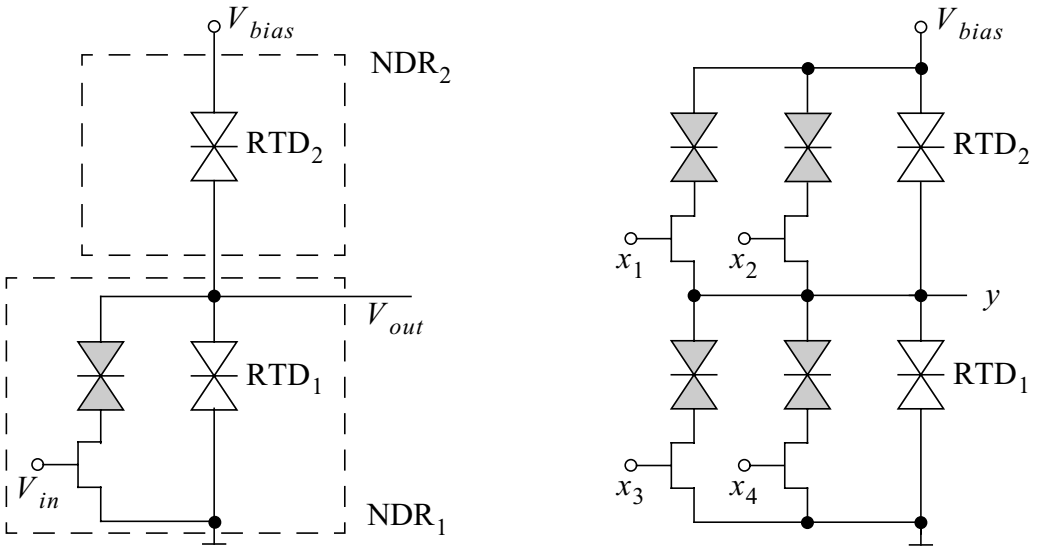
Captions to the figures:

Figure 1: a) circuit configuration of a MOBILE implementing an inverter

b) MOBILE circuit implementing the TG which is y=1 iff (x_1+x_2−x_3−x_4≥T)

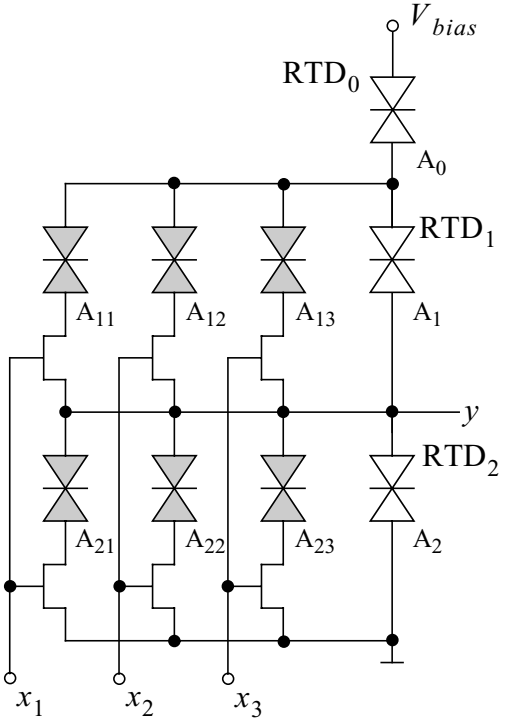
Figure 2: MOBILE circuit implementing the MTTG defined as [2, 1, 1; 2, 4]

Figure 3: Simulation results for the [2, 1, 1; 2, 4] MTTG



(a) (b)

Figure 1



x_1	$x_2 \mid x_3$	y	RTD quenched	Area relations
0	0	0	RTD$_1$	$\begin{cases} A_1 < A_0 \\ A_1 < A_2 \end{cases}$
0	1	0	RTD$_1$	$\begin{cases} A_1 + AJ_1 < A_0 \\ A_1 + AJ_1 < A_2 + AJ_2 \end{cases}$
0	2	1	RTD$_2$	$\begin{cases} A_2 + 2AJ_2 < A_0 \\ A_2 + 2AJ_2 < A_1 + 2AJ_1 \end{cases}$
1	0	1	RTD$_2$	$\begin{cases} A_2 + 2AJ_2 < A_0 \\ A_2 + 2AJ_2 < A_1 + 2AJ_1 \end{cases}$
1	1	1	RTD$_2$	$\begin{cases} A_2 + 3AJ_2 < A_0 \\ A_2 + 3AJ_2 < A_1 + 3AJ_1 \end{cases}$
1	2	0	RTD$_0$	$\begin{cases} A_0 < A_1 + 4AJ_1 \\ A_0 < A_2 + 4AJ_2 \end{cases}$

(a) (b)

Figure 2

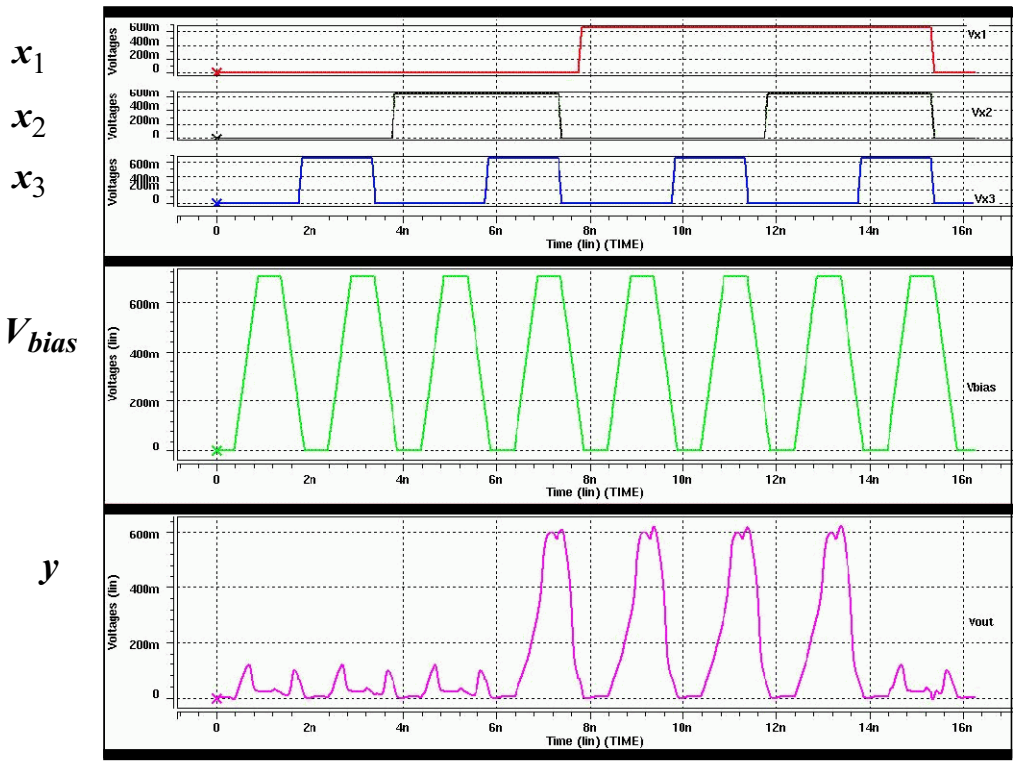

x_1
x_2
x_3
V_{bias}
y
Voltages
Vx1
Vx2
Vx3
Vbias
Vout
Voltages (lin)
Time (lin) (TIME)
0
2n
4n
6n
8n
10n
12n
14n
16n
600m
400m
200m

Figure 3