Multi-User MIMO Testbed

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ABSTRACT

This paper provides an overview of a real-time multi-user multiple-input multiple-output (MIMO) communication testbed designed for demonstration and assessment of real-world wireless communication aspects. The testbed is built on a modular hardware platform consisting of three different boards, and it incorporates a MIMO-OFDM-based physical (PHY) layer, an embedded media access controller (MAC), and an Ethernet interface. The modular design of the testbed permits both real-time and offline processing experiments under realistic conditions.

Categories and Subject Descriptors: C.2.1 [Network Architecture and Design]: Real-time multi-user MIMO testbed for wireless communication

General Terms: Algorithms, Design, Experimentation, Measurement

1. INTRODUCTION AND MOTIVATION

Many design ideas for improving and extending MIMO wireless communication systems are presented in the open literature (e.g., [1]). However, not all of them are feasible for practical implementation, or have already shown the promised gains in practice. From a simulation point of view, it is often difficult to estimate whether a certain concept or algorithm will perform well in real systems, hence practical assessment of implementation and real-world aspects is required. This complemental insight, which goes beyond theoretical simulations, can only be obtained from testbeds or a similar prototyping infrastructure. Testbeds offer the ability to assess and understand real-world performance and implementation aspects, and they enable to practically explore design trade-offs.

2. HARDWARE OVERVIEW

Our multi-user MIMO testbed consists of five individual terminals. A single terminal is shown in Fig. 1. Three different hardware components are required for a terminal:

VAMP: As base of the testbed platform, this board is the largest component. It contains two large XILINX Virtex-II Pro FPGAs with embedded PowerPC CPUs, external SRAM and SDRAM memory, a Gigabit Ethernet interface, a PCI interface, dedicated power supplies, FPGA configuration logic, and digital IO connectors for additional daughter boards.

BAT: This board is smaller than the VAMP board.It contains a XILINX Virtex-4 FPGA, SRAM memory, dedicated high-speed interconnects for attachment of up to four RF boards, configuration logic, and USB connectivity for user control. The BAT board provides the interface between the VAMP board and the WING boards.

WING: This board contains a complete RF chain for wireless transmission and reception. It consists of an analog-digital/digital-analog conversion chip, a RF dual-band transceiver, and a front-end module for filtering and amplification. Four WING boards are required for a terminal with four-stream MIMO communication capability.

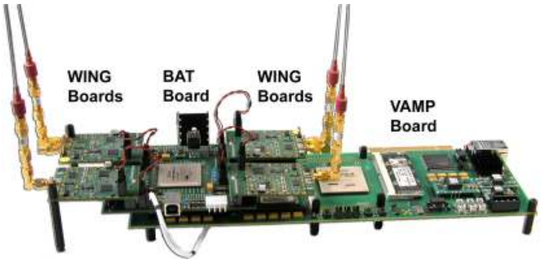

Figure 1: One terminal of the MIMO testbed

3. REAL-TIME MIMO TESTBED

The real-time multi-user MIMO testbed helps to understand various aspects of system-level design: It provides the base for VLSI implementation trade-offs, it offers the ability for assessing the MAC layer, and it also illustrates the importance of understanding cross-layer aspects such as latency for both MAC and PHY layers, e.g., MAC response time, or validity of channel state information.

An overview of the architecture of a MIMO terminal is given in Fig. 2. The entire system is partitioned into three major subsystems: The Ethernet subsystem allows for wired network connectivity including data transfers from the Internet. The PowerPC subsystem handles all MAC layer processing tasks, and the MIMO subsystem is responsible for all physical layer aspects of MIMO communication. The external SRAM memory and all subsystems are interconnected through a system bus. High-speed data transfers without

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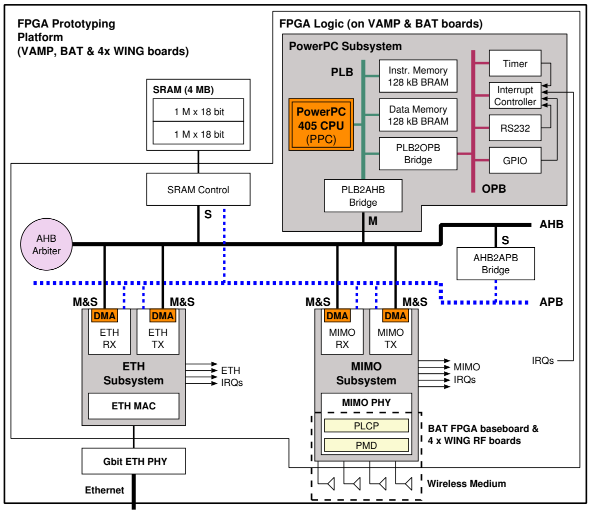

Figure 2: System architecture of a MIMO terminal

CPU interaction are carried out using direct memory access (DMA) engines.

MIMO Physical Layer

The MIMO physical layer (Fig. 3) is implemented on the two FPGAs of the VAMP board. The channel de-/coding block is based on bit-interleaved coded modulation (BICM) and contains a Viterbi decoder. The OFDM modulation block performs the mapping of binary data to constellation points and the I/FFT transformation. The MIMO processing block in the receive path carries out channel estimation and MMSE detection based on direct matrix inversion [2]. The synchronization block is responsible for frame start detection, frequency offset estimation and compensation [3]. Up-/downsampling and automatic gain control (AGC) are located on the BAT board.

The PHY layer was initially based on the IEEE 802.11a standard, and it has been extended with proprietary MIMO functionality. The MIMO PHY layer is designed to support up to four spatial streams. Modulation schemes range from BPSK to 64-QAM (Tbl. 1) and coding rates 1/2, 2/3, and 3/4. The physical layer data rates range from 24 Mbit/s with BPSK rate 1/2 to a maximum of 216 Mbit/s by using 64-QAM rate 3/4.

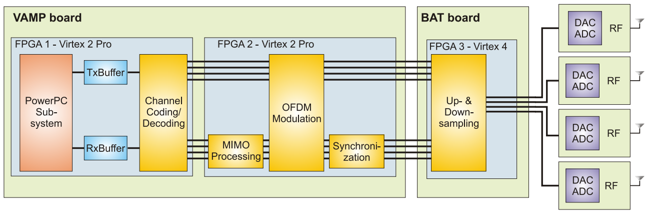

Figure 3: Partitioning of the MIMO physical layer

Media Access Control Layer

A polling-based media access control (MAC) layer is implemented in software on one PowerPC in FPGA 1 of the VAMP board. One terminal acts as access point (AP) for the entire network, and the other terminals act as stations (STA). The AP employs a point-coordination function for centralized and simplified servicing of all STAs. The AP is responsible for polling all STAs regularly according to its internal scheduling algorithm. This simple MAC coordination scheme allows for keeping the overall implementation complexity low [4].

Table 1: MIMO PHY modulation parameters

Channel bandwidth	20 MHz
Modulation	BPSK, QPSK, 16-QAM, 64-QAM
Number of subcarriers	64 in total (12 zero tones, 4 pilot tones, 48 data tones)
OFDM symbol duration	4 µs
Guard interval	0.8 µs
Subcarrier spacing	312.5 kHz

4. OFFLINE MIMO TESTBED

The offline testbed provides the ability for experiments over real-world MIMO channels. All signal processing takes place in Matlab. This approach enables easy and flexible assessment of new algorithms or protocols in conjunction with real-world aspects. A conceptual overview is shown in Fig. 4. The offline testbed employs only BAT and WING boards and is controlled by Matlab through the USB link. The baseband samples for each stream to be transmitted are written into a buffer on the FPGA of the BAT board. A dedicated command starts the transmission. On the receive side, a signal-power-based peak detector starts the recording of the incoming waveforms into a buffer. After complete reception, the samples are read out and processed by Matlab.

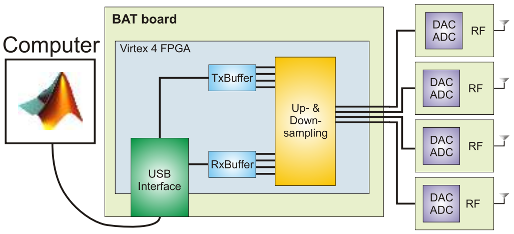

Figure 4: Block diagram of the offline testbed

5. ACKNOWLEDGMENTS

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