Multi-V_T UTBB FDSOI Device Architectures for Low-Power CMOS Circuit

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***Abstract*—This paper analyzes the potential of fully depleted silicon-on-insulator (FDSOI) technology as a multiple threshold voltage V_T platform for digital circuits compatible with bulk complementary metal–oxide–semiconductor (CMOS). Various technology options, such as gate materials, buried oxide thickness, back plane doping type, and back biasing, were investigated in order to achieve a technology platform that offers at least three distinct V_T options (high-V_T, standard-V_T, and low-V_T). The multi-V_T technology platform highlighted in this paper was developed with standard CMOS circuit design constraints in mind; its compatibility in terms of design and power management techniques, as well as its superior performance with regard to bulk CMOS, are described. Finally, it is shown that a multi-V_T technology platform based on two gate materials offers additional advantages as a competitive solution. The proposed approach enables excellent channel electrostatic control and low V_T variability of the FDSOI process. The viability of the proposed concept has been studied through technology computer-aided design simulations and demonstrated through experimental measurements on 30-nm gate length devices.**

***Index Terms*—Back plane (BP), multi-V_T, ultra-thin body and buried oxide (BOX) FDSOI (UTBB FDSOI), well implant.**

I. Introduction

CONTINUED scaling of planar bulk CMOS technologies enables density increase with diminishing improvements in performance and power dissipation. Device variability and threshold voltage V_T limited scaling hamper the reduction in power dissipation by limiting the minimum operating and standby supply voltages. To continue increasing the speed of low-power (LP) applications while keeping adequate static power consumption, various design and process solutions have been developed. Among them, multi-V_T CMOS design platforms are commonly used. High-V_T (HVT) (500 mV $\leq$ HVT $\leq$ 650 mV) transistors are used in noncritical paths to keep low leakage currents, whereas standard-V_T (SVT) (350 mV $\leq$ SVT $\leq$ 500 mV) and low-V_T (LVT) (200 mV $\leq$ LVT $\leq$ 350 mV) transistors are commonly used in critical paths to meet timing constraints [1], [2]. In addition, at a design level, various power management (PM) and circuit process compensation (PC) techniques have been developed and are also widely used to overcome the process limitations. The efficiency of most of these techniques (body biasing, reverse source biasing, etc.) depends on the efficiency of the body effect on the V_T adjustment of the devices [3]. Below the 45-nm node, the increase in short-channel effects (SCE) in bulk devices makes PM and PC techniques less efficient.

Undoped thin-film planar fully depleted silicon-on-insulator (FDSOI) devices are being investigated as an alternative to bulk devices in 32-nm node and below because of their excellent short-channel electrostatic control, low-leakage currents, and immunity to random dopant fluctuation [4]–[7]. Although FDSOI technology has a superior $I_{\mathrm{EFF}}/I_{\mathrm{OFF}}$ ratio, it is still necessary to incorporate multi-V_T, PM, and PC techniques to reduce the active/standby leakage and improve the variability control.

In contrast to bulk technology, V_T is primarily set by the gate material work function (WF) in FDSOI devices. Setting up multi-V_T devices in FDSOI technology is then very challenging, requiring a processing expertise to finely control the V_T value. Today, the cointegration of two gate materials has been demonstrated [8]–[11]. However, cointegrating more than two gate materials prohibitively complicates the process. Indeed, it requires perfectly controlling the gate patterning and cleaning to avoid degradations of the device electrical characteristics. To get additional V_T options, the solution would be to dope the channel, as in bulk technology, but at the expense of a higher V_T variability and mobility degradation, limiting the primarily benefit of FDSOI technology [12].

In [13] and [14], it has been proposed and demonstrated in 45-nm node that integrating a doped back plane (BP) below an ultra-thin buried oxide (BOX) (< 30 nm) allows setting up three distinct V_T options with a single metal gate. Regarding the process flow, this approach is very attractive due to its simplicity and compatibility with a standard FDSOI CMOS process. However, at a design level, this approach is not fully compatible with bulk CMOS circuit design and may require a redesign of certain existing intellectual properties (IPs).

In this paper, a fully compatible bulk CMOS multi-V_T technology platform derived from [13] and [14] is proposed

Manuscript received January 10, 2011; revised March 14, 2011 and May 5, 2011; accepted May 5, 2011. Date of publication June 16, 2011; date of current version July 22, 2011. This work was supported in part by IBM, by STMicroelectronics, by Laboratoire d'Electronique et de Technologie de l'Information Alliance program, and by the Catrene DEvice & CIrcuit performance boosted through SIlicon material Fabrication (DECISIF) and French Nanosmart Research and Development Projects. The review of this paper was arranged by Editor H. S. Momose.

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Digital Object Identifier 10.1109/TED.2011.2155658

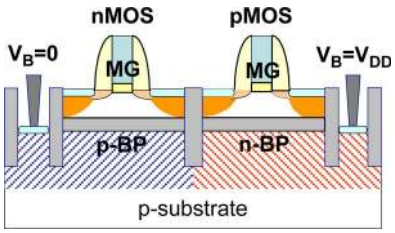

Fig. 1. Cross-sectional view of UTBB FDSOI nMOS and pMOS devices with BP.

TABLE I
V_T OPTIONS OF UTBB FDSOI nMOS AND pMOS DEVICES FOR VARIOUS BP DOPING TYPES AND V_{BS}

V_{BS}	0V	V_{DD}
n-BP	SVT (i)	LVT
p-BP	HVT	SVT (ii)
w/o BP	SVT (iii)	SVT (iii)
nMOSFET		

$\|V_{BS}\|$	0V	V_{DD}
n-BP	HVT	SVT (ii)
p-BP	SVT (i)	LVT
w/o BP	SVT (iii)	SVT (iii)
pMOSFET		

and evaluated in ultra-thin body and BOX (UTBB) FDSOI technology. This paper is organized as follows: In Section II, the efficiency of the single-gate multi-V_T approach is analyzed for 30-nm gate length devices. Furthermore, the impact of the different device architecture on the body effect efficiency is analyzed. In Section III, the circuit design limitations are discussed, and then, technological options are proposed to make this approach compatible with bulk CMOS circuit design. In Section IV, the concept is expanded to a solution based on two gate materials and demonstrated on silicon. Finally, conclusions and remarks are given in Section V.

II. SINGLE-GATE MULTI-V_T DEVICE CONCEPT

As illustrated in Fig. 1, UTBB FDSOI devices consist of an undoped silicon thin film ($T_{Si} \sim 1/4 \cdot L_G$) on a thin BOX ($10\ \text{nm} < T_{BOX} < 30\ \text{nm}$), covering a highly doped BP [15].

This device architecture was initially proposed to improve SCE and drain-induced barrier lowering (DIBL) by reducing the source/drain (S/D) capacitance coupling to the channel [16]–[18].

Later, the interest in this device architecture was extended to obtain multi-V_T devices [13]. In this approach, the V_T of the device is adjusted by the electrostatic control of the BOX/BP back interface. This back interface is shown as a thick oxide/poly-Si back gate, either n- or p-type. Depending on the BP type and the voltage applied (V_B), different V_T are then achieved. Table I summarizes the different nMOS and pMOS device V_T configurations. HVT devices are based on a BP doping type opposed to the S/D one and V_B equal to the source voltage V_S. LVT devices are based on a BP doping type similar to the S/D one and $|V_{BS}| = V_{DD}$. SVT option can be achieved by the following three different schemes: 1) similar BP with $V_{BS} = 0$; 2) opposed BP with $|V_{BS}| = V_{DD}$; and 3) finally, without BP implementation (w/o BP).

A. Simulation Conditions

The electrical characteristics of nMOS and pMOS devices have been extracted from technology computer-aided design (TCAD) simulations based on an improved low-field mobility model including surface roughness and remote Coulomb scattering effects calibrated on experimental data [19]. Simulated devices present a midgap (MG) metal gate ($\Phi_{MG} = 4.71$ eV), a high-κ dielectric gate stack of 1.2 nm equivalent oxide thickness (EOT), a Si-film of 6 nm with a doping level of 10^{15} cm^{-3} and BP doping profiles depicted in Fig. 2. BP doping profiles have been obtained by process simulations [20] based on the doping concentration and energy implantation parameters used in [21] and [22]. They have been optimized in order to keep the Si-film undoped leading a low V_T variability, as shown in [23]. Drift-diffusion with density-gradient quantum correction and usual Shockley–Read–Hall generation–recombination rate are used for carrier transport. Moreover, an advanced low-field mobility model including surface roughness and remote Coulomb scattering effects ensures a good mobility description, compared to experimental measurements [19]. Finally, SCE have been calibrated on recent experimental data by adjusting access doping levels and profiles down to 30-nm gate length [24].

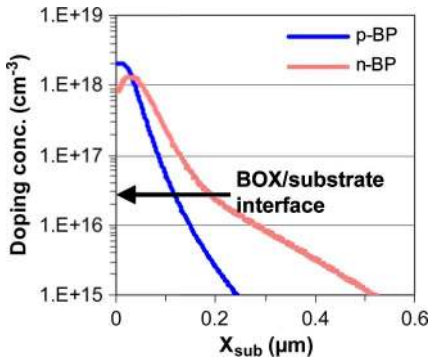

Fig. 2. Spike annealing at 1050 °C simulated BP doping profiles of UTBB FDSOI devices at $T_{BOX} = 10$ nm.

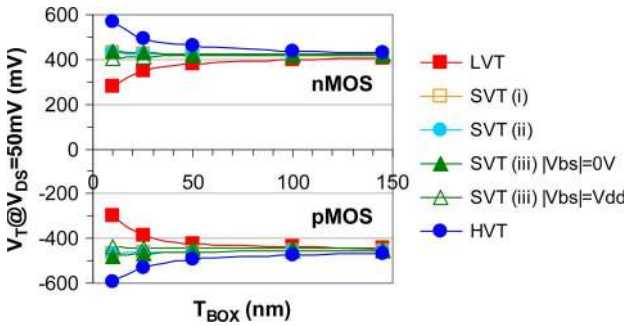

Fig. 3. Linear V_T versus T_{BOX} of FDSOI nMOS and pMOS devices for various BP configurations at $L_G = 30$ nm.

B. Threshold-Voltage Characteristics

Fig. 3 shows the linear V_T (extracted at constant current ($70.10^{-9}/L_G$ (μm)) at $V_{DS} = 50$ mV) variations versus the BOX thickness (T_{BOX}) for the device configurations defined in Table I. As expected, for T_{BOX} below 50 nm, the V_T response to V_{BS} and BP doping type becomes significant, giving rise to three distinct V_T options. It is worth to note that the V_T mismatch between the nMOS and pMOS devices is due to the

TABLE II
ELECTRICAL CHARACTERISTICS OF MULTI-V_T UTBB FDSOI nMOS AND pMOS DEVICES AT $T_{BOX} = 10$ nm, $L_G = 30$ nm, AND $V_{DD} = 0.9$ V

nMOSFET	lin V_T (mV)	DIBL (mV/V)	I_{ON} (µA/µm)	I_{OFF} (pA/µm)	sat SS (mV/dec)
LVT	278	46	480	2139	77
SVT (i)	429	37	332	16	76
SVT (ii)	430	37	333	17	77
SVT (iii) $\|V_{BS}\|$=0V	439	41	330	10	74
SVT (iii) $\|V_{BS}\|$=V_{DD}	408	83	404	68	73
HVT	567	37	208	0.1	73
pMOSFET	**lin $\|V_T\|$ (mV)**	**|DIBL| (mV/V)**	**I_{ON} (µA/µm)**	**I_{OFF} (pA/µm)**	**sat SS (mV/dec)**
LVT	301	47	353	1257	78
SVT (i)	468	40	229	6	77
SVT (ii)	468	43	233	6	77
SVT (iii) $\|V_{BS}\|$=0V	478	42	226	3	74
SVT (iii) $\|V_{BS}\|$=V_{DD}	435	89	297	38	73
HVT	591	42	146	0.06	72

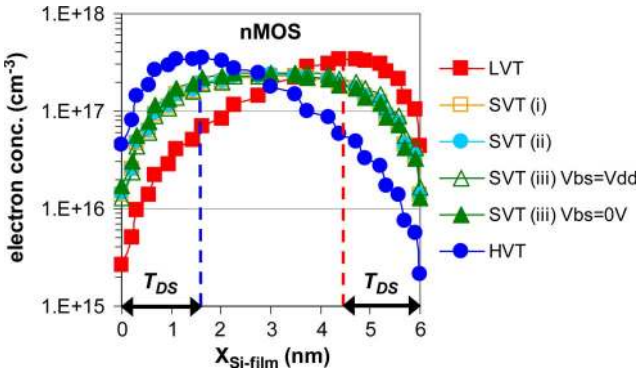

Fig. 4. Electron concentration versus Si-film depth ($X_{\text{Si-film}}$) of a UTBB FDSOI nMOS device for various BP configurations at $T_{BOX} = 10$ nm and $L_G = 1$ µm.

adjustments of access doping levels and profiles allowing to target the silicon data.

Table II summarizes the electrical characteristics obtained for each device options at 10 nm of T_{BOX}. The results obtained confirm the efficiency of the BP approach to set up multi-V_T devices. The LVT option is 290 mV lower than the HVT option for 2 nA/µm of I_{OFF} current, which complies with the LP 32-nm node specifications ($I_{OFF} < 5$ nA). Furthermore, the results show excellent SS and DIBL for each option.

C. Body Effect Characteristics

Recent device developments have shown that UTBB FDSOI technology is also a compelling alternative to bulk technology regarding PM and PC due to an excellent body factor ($\gamma = \Delta V_T/\Delta V_{BS}$) [14]. In UTBB FDSOI technology, γ is related to the Si-film charge Q_{Si} variation, which depends on the conductivity of the back Si-film/BOX interface. Fig. 4 shows the electron concentration in the Si-film for the different V_T options of a long-channel nMOS device at $V_G = V_T$. In contrast to the HVT option, the highest concentration appears close to the back interface for the LVT option, meaning that the barycenter of Q_{Si}, and therefore, the channel is located close to the back interface, when $V_G = V_T$. The space between the interface and the Q_{Si} barycenter, which is called dark space T_{DS}, is induced by the quantum-confinement effect. Besides, for the SVT options, the front and back Si-film interfaces are balanced, meaning that the Q_{Si} barycenter is in the middle of Si-film, leading to a volume-inversion channel.

For a long-channel device with a thick Si-film ($T_{Si} \geq 10 \times T_{DS}$), (1) and (2) give γ when a channel is created at the front γ_{FC} or the back γ_{BC} interface at $V_G = V_T$, respectively [25], i.e.,

$$\gamma_{FC} = \frac{C_{BOX}}{C_{OX}} \cdot \frac{C_{Si}}{C_{BOX} + C_{Si}} \tag{1}$$

$$\gamma_{BC} = \frac{C_{BOX}}{C_{OX}} \cdot \frac{C_{OX} + C_{Si}}{C_{Si}}. \tag{2}$$

Substituting the capacitance with their formulas ($C_{ox} = \varepsilon_0\varepsilon_{SiO2}\text{S/EOT}, C_{Si} = \varepsilon_0\varepsilon_{Si}\text{S/T}_{Si}, C_{BOX} = \varepsilon_0\varepsilon_{SiO2}\text{S/T}_{BOX}$), the following equations can be derived:

$$\gamma_{FC} = \frac{\text{EOT}}{T_{BOX} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{Si}} T_{Si}} \tag{3}$$

$$\gamma_{BC} = \frac{\text{EOT} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{Si}} T_{Si}}{T_{BOX}}. \tag{4}$$

Equations (3) and (4) translate the body factor dependence on the Si-film potential ϕ_{Si}, which depends on the gate-to-substrate capacitance network. For a front channel, [see (3)] ϕ_{Si} is between C_{ox} and C_{Si} in series with C_{BOX}, whereas ϕ_{Si} is between C_{ox} in series with C_{Si} and C_{BOX} for a back channel [see (4)]. ϕ_{Si} is related to the Q_{Si} barycenter, and then, the ϕ_{Si} location in Si-film linearly varies with the Q_{Si} barycenter. Equation (5) proposed a model precisely describing γ when the channel is located in the Si-film volume. The following equation is derived from (3) and (4) and the Q_{Si} barycenter location in the Si-film (X_{bar}):

$$\gamma = \frac{\text{EOT} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{Si}}(X_{bar})}{T_{BOX} + \frac{\varepsilon_{SiO_2}}{\varepsilon_{Si}}(T_{Si} - X_{bar})}. \tag{5}$$

When $X_{bar} = T_{Si}/2$, it approximately gives γ of the SVT options. When $X_{bar} = T_{DS}$, it gives the γ of the HVT option, and when $X_{bar} = T_{Si} - T_{DS}$, it gives the γ of the LVT option. For 1.2 nm of EOT, 1.6 nm of T_{DS}, 6 nm of T_{Si}, and 10 nm of T_{BOX}, analytically, γ are 141, 200, and 263 mV/V for the HVT, SVT, and LVT options, respectively. These results highlight that the back interface conductivity increase boosts the body effect due to the higher Q_{Si} charge controlled by the back gate.

Fig. 5(a) and (b) show the γ variation versus T_{BOX} of each nMOS and pMOS device configurations ($L_G = 1$ µm) extracted in forward (FBB) and reverse (RBB) back bias modes. FBB and RBB are defined with regard to the default V_{BS} value of each V_T option (see Table I), as illustrated in Fig. 6. The maximum $|\Delta V_{BS}|$ applied is $V_{DD}/2 = 450$ mV. As expected, the results display a significant increase in γ with the BOX thinning and a higher γ for LVT devices than the HVT ones. However, the LVT option does not achieve the theoretical maximum γ expected at 10 nm of T_{BOX} (156 to 180 mV/V versus 263 mV/V) and does not outperform the SVT options

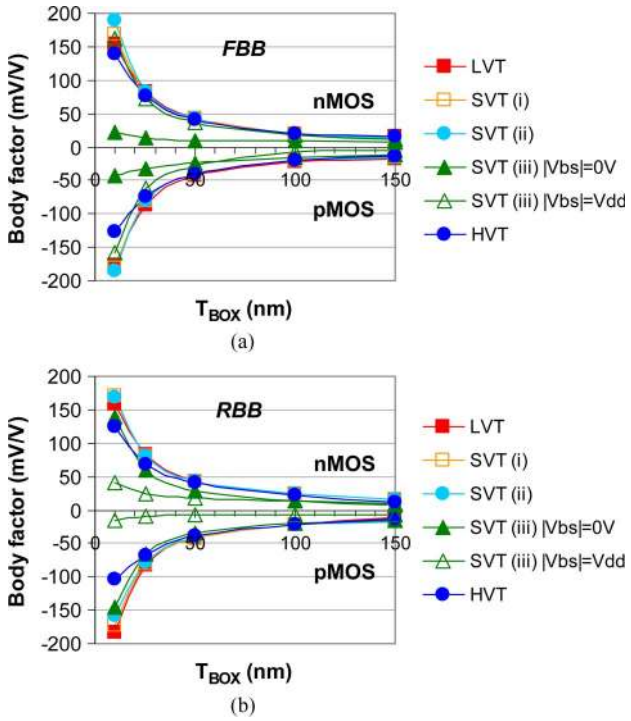

Fig. 5. Body factor ($\Delta V_T/\Delta V_{\rm BS}$) versus $T_{\rm BOX}$ from (a) FBB ($V_{\rm BS}+$ 450 mV for nMOS and $V_{\rm BS}-450$ mV for pMOS) and (b) RBB ($V_{\rm BS}-$ 450 mV for nMOS and $V_{\rm BS}+450$ mV for pMOS) effects of FDSOI nMOS and pMOS devices for various BP configurations at $L_G = 1$ μm.

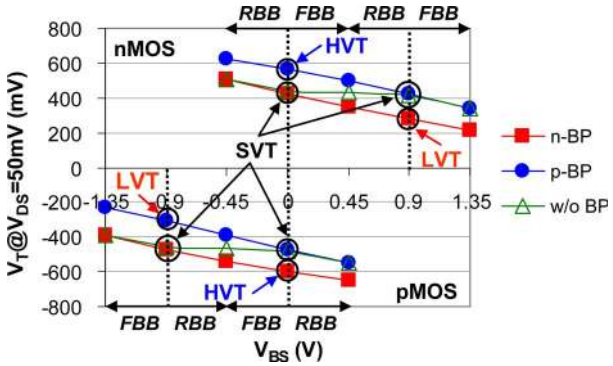

Fig. 6. Linear V_T versus $V_{\rm BS}$ of UTBB FDSOI nMOS and pMOS devices for various BP types at $T_{\rm BOX} = 10$ nm and $L_G = 1$ μm.

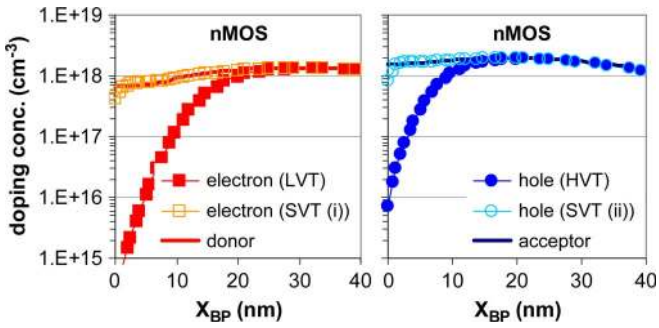

Fig. 7. Doping concentration versus BP depth $X_{\rm BP}$ of a UTBB FDSOI nMOS device for various BP configurations at $L_G = 1$ μm.

for nMOS devices. As illustrated in Fig. 7, it is caused by the BP depletion at the BOX/BP interface, increasing the equivalent BOX thickness, which limits the conduction state of the Si-film

TABLE III
BODY EFFECT CHARACTERISTICS ($\Delta V_T/\Delta V_{\rm BS}$ WITH $\Delta V_{\rm BS} = V_{\rm BS} \pm V_{\rm DD}/2$) OF LONG- AND SHORT-CHANNEL MULTI-V_T UTBB FDSOI nMOS AND pMOS DEVICES AT $T_{\rm BOX} = 10$ nm AND $V_{\rm DD} = 0.9$ V

γ (mV/V)	L_G=1µm	L_G=30nm	L_G=1µm	L_G=30nm
LVT	156	161	180	185
SVT (i)	170	172	177	178
SVT (ii)	179	179	171	170
HVT	132	128	115	111
	nMOSFET		pMOSFET	

back interface. This physical effect is amplified with $|V_{\rm BS}|$ in FBB, explaining why γ of LVT is lower than expected and lower than the SVT (i) and (ii). Indeed, SVT (i) is based on the same BP type, but the BP depletion is weaker. The HVT option is also affected by the BP depletion but much less than to a higher doping level, as shown in Fig. 2. SVT (ii) leads to the highest γ due to the opposite BP type used, setting the BOX/BP interface in an accumulation mode and resulting in an equivalent BOX thickness close to $T_{\rm BOX}$.

The same issue affects even more the SVT (iii) device configurations without BP due to a lower doping. For the nMOS device, with $0\ {\rm V} \le V_{\rm BS} \le V_{\rm DD}$ ($-V_{\rm DD} \le V_{\rm BS} \le 0$ V for pMOS devices), the BOX/BP interface is depleted, increasing the equivalent BOX thickness. For $V_{\rm BS} < 0$ V ($V_{\rm BS} > 0$ V for pMOS devices), the BOX/substrate interface reaches an inversion mode, whereas for $V_{\rm BS} > V_{\rm DD}$ ($V_{\rm BS} < -V_{\rm DD}$ for pMOS devices) the interface is in an accumulation mode [24]. In these former cases, the equivalent BOX thickness remains close to the intrinsic BOX thickness, which leads to γ values similar to the device with a BP.

The depletion phenomenon below the BOX can be introduced in equation (5), as shown in equation (6) where $T_{\rm dep}$ is the depletion thickness, i.e.,

$$\gamma = \frac{\mathrm{EOT} + \frac{\varepsilon_{\rm SiO_2}}{\varepsilon_{\rm Si}}(X_{\rm bar})}{T_{\rm BOX} + \frac{\varepsilon_{\rm SiO_2}}{\varepsilon_{\rm Si}}(T_{\rm Si} - X_{\rm bar} + T_{\rm dep})}. \tag{6}$$

In taking into account the BP depletion thickness for the HVT, SVT (i) (ii) and LVT nMOS devices, (6) gives γ of 122, 170, 180, and 154 mV/V, respectively. These results are in good agreement with those of the Table III. Regarding pMOS devices, due to complementary BP doping types, compared with nMOS devices, $T_{\rm dep}$ is higher for the HVT/SVT (ii) options, decreasing γ, and lower for the LVT/SVT (i) options, increasing γ. Nevertheless, it is worth to note that a hole channel leads to a higher $T_{\rm DS}$, which slightly increases the γ of the HVT devices and decreases the γ of the LVT devices.

For short-channel devices ($L_G = 30$ nm), extracted γ remains close to the long-channel ones, as shown in Table III. The SCE naturally reinforce the back interface conduction, increasing γ by few millivolts for the LVT and, to a lesser extent, SVT (i) options. Nevertheless, they also reduce, into the same order, the γ of devices favoring the front conduction such as HVT and, to a lesser extent, SVT (ii) options. This is due to the degradation of channel electrostatic control by the front gate. It is worth to note that the SVT device configurations with BP [(i), (ii)] give higher γ, except for pMOS devices

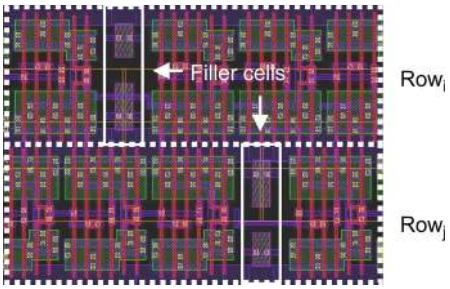

Fig. 8. Layout view of a complex digital circuit based on standard cell methodology.

due to a weaker BP depletion (p-BP doping higher than n-BP one), making them finally more attractive for PM and PC. Regarding the range of $|\Delta V_{\rm BS}|$, it is worth to note that it is not scalable, as in bulk technology [26]. This is due to the BOX dielectric isolation between S/D and substrate. In this way, the limit comes from the biasing of p-/n-well junctions between the nMOS and pMOS devices in CMOS circuits.

III. CMOS Circuit Design Constraints

Once the proposed device architectures have been electrically validated, their utilization in CMOS circuit has to be carefully studied.

In bulk CMOS technology, the physical design of complex digital circuits is based on the standard cell methodology. The cells are realized as fixed height, which enables them to be placed in rows, facilitating the process of automated digital layout. In order to bias the well, filler cells are periodically included in each row, as illustrated in Fig. 8. The single-gate multi-V_T UTBB FDSOI concept breaks down the circuit design regularity due to the use of different BP doping types per device type. Therefore, their cointegration leads to circuit design constraints that must be taken into account, in particular, for the SVT and LVT options.

A. SVT Option Considerations

For the SVT option, the two alternatives based on BP are the most promising devices for PM and PC. However, these devices cannot be implemented in a straightforward manner at the circuit level. Indeed, these configurations required an n-BP grounded for nMOS devices (or pMOS devices with regard to the second alternative) and a p-BP tied to $V_{\rm DD}$ for pMOS devices (for nMOS devices with regard to the second alternative) biasing the BP junction in forward, as illustrated in Fig. 9(a).

To overcome this issue, a triple-well technology is mandatory. However, it will impact the circuit density and, thus, is not suitable for digital circuit density. Another solution can be to process an additional BOX between BP and substrate with a deep shallow trench isolation (STI) but at the expense of the process complexity [27]. Fig. 9(b) depicts a high-density SVT device architecture proposed in [28]. It is based on a stack of BP and well layers. The BP is bordered by a deep–STI (for example, 300 nm from the top of Si-film), which leads to a vertical dielectric isolation of the BP. The well doping type

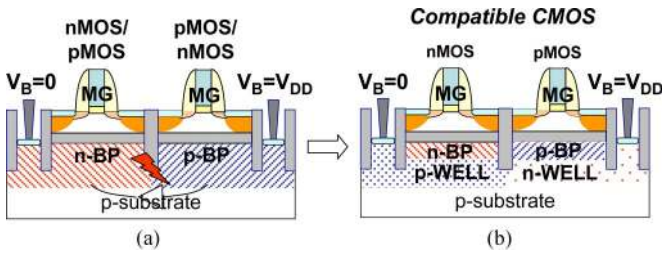

Fig. 9. Cross-sectional view of SVT UTBB FDSOI nMOS and pMOS devices with (a) BP and (b) complementary well types.

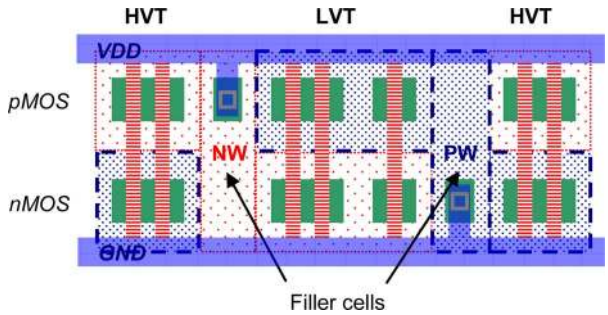

Fig. 10. Example of HVT and LVT standard cell cointegration with filler cells dedicated to make the bridge between these two types of standard cells.

used is complementary to the BP type, forming a p/n junction below the BOX (p-BP/n-well or n-BP/p-well). The BP biasing is therefore controlled by the well bias, and it becomes possible to apply $V_{\rm DD}$ to a p-BP and 0 V to an n-BP. Both the nMOS and pMOS devices can be implemented either with n-BP/p-well or p-BP/n-well stacks. However, to be compatible with the bulk CMOS design (i.e., nMOS $V_B = 0$, pMOS $V_B = V_{\rm DD}$), nMOS and pMOS transistors based on n-BP/p-well and p-BP/n-well, respectively, must be used. This makes the SVT (i)-based option the only usable solution.

B. LVT Option Considerations

The particularity of the LVT option is the use of opposite BP doping types for the nMOS and pMOS devices, compared with the HVT and SVT options. The design of a full LVT circuit can be easily managed, whereas the cointegration of the LVT standard cells with the SVT and HVT ones becomes more complex. Indeed, it leads to a disruptive design. In row, specific substrate contacts, which are called filler cells, become required to abut the different standard cell flavors, as illustrated in Fig. 10. Applying adaptive body biasing techniques (RBB and FBB) also required row-to-row isolation to tune the back gate of the HVT and LVT standard cells, independently. To limit area penalty, one solution would be to manage V_T-islands within the circuit, as for $V_{\rm DD}$-islands [29].

IV. Dual-Gate Multi-V_T Device Concept

The previous sections have demonstrated the feasibility of three distinct V_T options based on a single metal gate with MG WF with consideration of CMOS design constraints. This approach is compelling due to the use of a single-gate process but is limited by LVT device cointegration. To overcome this issue,

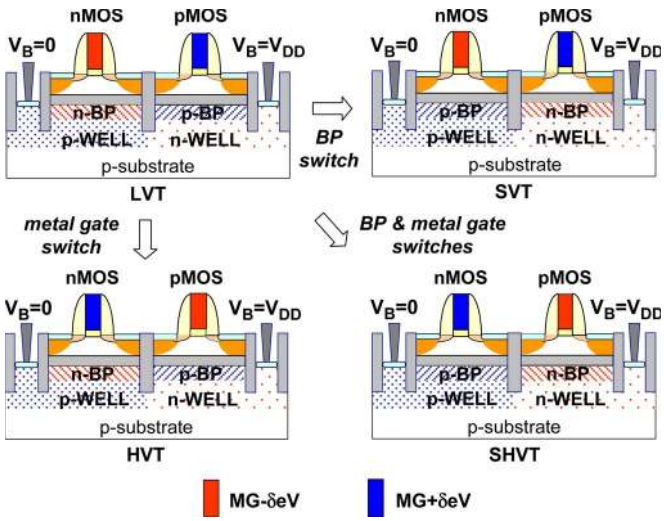

Fig. 11. Cross-sectional view of multi-V_T UTBB FDSOI nMOS and pMOS devices using two gate materials with work functions close to the MG (MG $\pm$ δeV).

one solution to enable LVT option could be channel counter doping but at the expense of the variability [12]. Another one could be triple-gate material integration. In addition to an MG metal gate to get the SVT option, two other types of metal gate will be used to obtain the LVT and HVT options. Nevertheless, cointegrating more than two different gate stacks prohibitively complicates the process. In contrast with bulk, FDSOI devices do not require band-edge WF due to the undoped Si-film [30]. It enables to tune the metal gate WF to adjust the V_T. In this section, the single metal gate multi-V_T concept is extended to two metal gate stacks. The proposed approach keeps the benefits of BP and ultra-thin BOX (V_T adjustment and modulation) while cointegrating two metal gate stacks, already existing in bulk technology.

A. Multi-V_T Strategy

Fig. 11 summarizes the strategy to achieve adequate HVT, SVT, and LVT devices. In this approach, the back bias effect used in the single-gate approach to shift the V_T is replaced by the use of two metal gate WF. As illustrated in Fig. 12, the WF of the metal gates are symmetrically placed from the MG metal gate WF to get a symmetrical V_T shift of the nMOS and pMOS devices. The gate WF is then tuned to fix the V_T of the HVT and LVT options, whereas the BP is used to enable the SVT option. Combining dual-gate integration and BP enables the following four distinct V_T options: 1) The LVT devices are based on a BP doping type similar to the S/D one with gate WF = MG $-$ δeV for the nMOS device and gate WF = MG + δeV for the pMOS device; 2) the HVT devices are obtained by inverting the gate materials while keeping the same BP type; 3) the SVT devices are obtained by inverting the BP type while keeping the same gate material as the LVT option; and 4) the super-HVT (SHVT) devices are obtained by inverting both the gate material and the BP type. For CMOS design compatibility, well-based concept presented in Section II is used. In contrast to the single-gate approach, p- and n-well are respectively grounded and tied

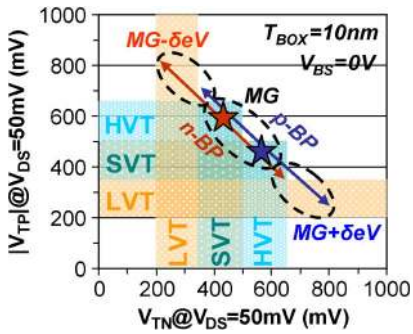

Fig. 12. Linear nMOS V_T versus linear pMOS V_T of UTBB FDSOI devices using two gate materials with work functions close to the MG (MG $-$ δeV and MG + δeV) and two BP doping types at $V_{\rm BS} = 0$ V, $T_{\rm BOX} = 10$ nm, and $L_G = 30$ nm.

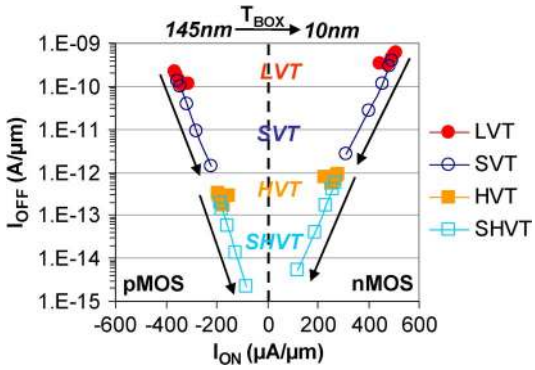

Fig. 13. $I_{\rm ON}$ versus $I_{\rm OFF}$ of UTBB FDSOI nMOS and pMOS devices using two gate materials with work functions close to the MG (MG $\pm$ 0.1 eV) for various $T_{\rm BOX}$ (10, 25, 50, 100, and 145 nm) at $L_G = 30$ nm.

to $V_{\rm DD}$ for all device options, making this multi-V_T dual-gate solution fully compatible with bulk CMOS design.

In Fig. 13, the gate WF has been tuned (MG $\pm$ 0.1 eV) to meet the $I_{\rm OFF}$ current specifications of the LVT and HVT devices for the 32-nm node. The figure shows the variation of the currents versus the BOX thickness, i.e., from 10 to 145 nm. The results highlight the only dependence of the SVT and SHVT options on the BOX. To well balance SHVT, HVT, SVT, and LVT options, the V_T shift induced by the gate WF and the BP must be roughly in the same order of magnitude. This rule of thumb is satisfied for 10–25 nm of $T_{\rm BOX}$ for a gate length of 30-nm.

B. Silicon Results

UTBB substrates of 300 mm with a $T_{\rm BOX}$ of 10 nm were used to fabricate UTBB FDSOI CMOS transistors and to validate the dual-gate multi-V_T solution. After Si-film thickness thinning down to 6 nm and STI fabrication, either indium or arsenic has been implanted to form a BP layer below the BOX. Two metal gates have been chemical-vapor-deposited on HfSiON dielectrics, i.e., 5 nm of TiN and 10 nm of TaAlN/TaN. The EOT is $\sim$1.15 nm, whatever the type of device and the gate stack [31]. Fig. 14 shows the experimental nMOS and pMOS linear V_T results obtained with HfSiON/TiN (MG $-$ δeV) and HfSiON/TaAlN/TaN (MG + δeV) gate stacks for the different device architectures defined in Fig. 11. Both experimental and

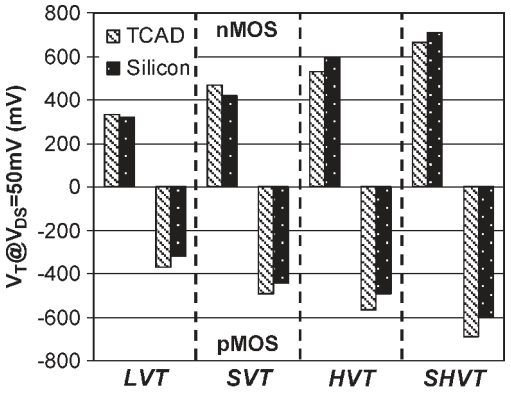

Fig. 14. Simulated and experimental linear V_T of multi-V_T UTBB FDSOI nMOS and pMOS devices using two gate materials with work functions close to the MG (MG $\pm$ 0.1 eV) at $T_{\mathrm{BOX}} = 10$ nm and $L_G = 30$ nm.

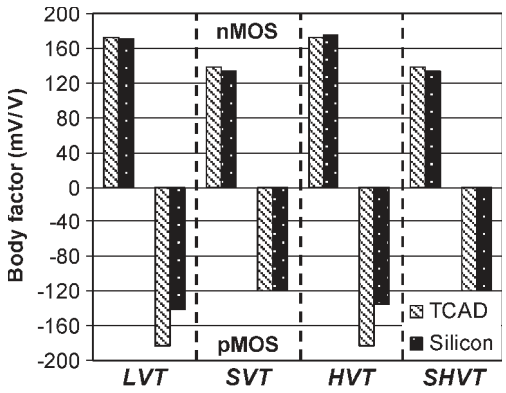

Fig. 15. Simulated and experimental body factor of multi-V_T UTBB FDSOI devices nMOS and pMOS using two gate materials with work functions close to the MG (MG $\pm$ 0.1 eV) at $T_{\mathrm{BOX}} = 10$ nm and $L_G = 30$ nm.

simulation results are compared. The data extracted from the measurements on silicon confirm the behavior predicted by the simulations.

Fig. 15 shows the body factor obtained for a V_{BS} variation of $\pm$450 mV ($V_{\mathrm{DD}}/2$). As expected and explained in Section II-C, the device architectures based on the BP configurations leading to back conduction (HVT and LVT) and lowest BP depletion result in the highest body factor. Indeed, in this case, the back gate controls a greater Q_{Si} charge.

The experimental results validate the viability of the multi-V_T approach and demonstrate that multi-V_T solutions compatible with bulk CMOS design are feasible on undoped-channel FDSOI technology.

V. Conclusion

In this paper, a deep analysis to set up multi-V_T devices in FDSOI technology has been presented. In this framework, various design and technology options, such as gate materials, BOX thickness, BP doping type, and back biasing have been investigated in order to achieve a technology platform, including three distinct V_T options. This multi-V_T technology platform has been developed while considering the CMOS circuit design constraints in order to be compatible with the existing bulk IPs and PM techniques. Finally, it has been shown that a multi-V_T technology platform based on dual-gate materials offers the best efficiency/complexity solution. Indeed, the proposed approach allows an excellent channel electrostatic control and, consequently, a better V_T variability control of the FDSOI technology. Moreover, efficient PM can be achieved due to an excellent body factor. Furthermore, a wide V_{BS} range can be applied due to the fully dielectric isolation of the devices from the substrate due to the BOX. TCAD simulations and experimental results validated the viability of the proposed multi-V_T approach and then demonstrated that multi-V_T solutions fully compatible with bulk designs are possible on undoped thin-film FDSOI technology. Regarding the process flow, this approach is very attractive due to its compatibility with a standard FDSOI process.

Acknowledgment

The authors would like to thank Aixtron for the metal gate depositions in fully depleted silicon-on-insulator experiments.

References

[1] T. Yamashita, N. Yoshida, M. Sakamoto, T. Matsumoto, M. Kusunoki, H. Takahashi, A. Wakahara, T. Ito, T. Shimizu, K. Kurita, K. Higeta, K. Mori, N. Tamba, N. Kato, K. Miyamoto, R. Yamagata, H. Tanaka, and T. Hiyama, "A 450 MHz 64 b RISC processor using multiple threshold voltage CMOS," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2000, pp. 414–415.

[2] S. Kunie, T. Hiraga, T. Tokue, S. Torii, and T. Ohsawa, "Low power architecture and design techniques for mobile handset LSI Medity M2," in *Proc. ASPDAC*, 2008, pp. 748–753.

[3] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[4] C. Fenouillet-Beranger, S. Denorme, B. Icard, F. Boeuf, J. Coignus, O. Faynot, L. Brevard, C. Buj, C. Soonekindt, J. Todeschini, J. C. Le-Denmat, N. Loubet, C. Gallon, P. Perreau, S. Manakli, B. Mmghetti, L. Pain, V. Arnal, A. Vandooren, D. Aime, L. Tosti, C. Savardi, F. Martin, T. Salvetat, S. Lhostis, C. Laviron, N. Auriac, T. Kormann, G. Chabanne, S. Gaillard, O. Belmont, E. Laffosse, D. Barge, A. Zauner, A. Tarnowka, K. Romanjec, H. Brut, A. Lagha, S. Bonnetier, F. Joly, N. Mayet, A. Cathignol, D. Galpin, D. Pop, R. Delsol, R. Pantel, F. Pionnier, G. Thomas, D. Bensahel, S. Deleombus, T. Skotnicki, and H. Mmgam, "Fully-depleted SOI technology using high-κ and single-metal gate for 32 nm node LSTP applications featuring 0.179 μm^2 6T-SRAM bitcell," in *IEDM Tech. Dig.*, 2007, pp. 267–270.

[5] A. Khakifirooz, K. Cheng, B. Jagannathan, P. Kulkarni, J. W. Sleight, D. Shahrjerdi, J. B. Chang, S. Lee, J. Li, H. Bu, R. Gauthier, B. Doris, and G. Shahidi, "Fully depleted extremely thin SOI for mainstream 20 nm low-power technology and beyond," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 152–153.

[6] O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Tosti, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelle, B.-Y. Nguyen, and S. Deleonibus, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding," in *IEDM Tech. Dig.*, 2008, pp. 245–248.

[7] K. Cheng, A. Khakifirooz, P. Kulkarni, S. Ponoth, J. Kuss, D. Shahrjerdi, L. F. Edge, A. Kimball, S. Kanakasabapathy, K. Xiu, S. Schmitz, A. Reznicek, T. Adam, H. He, N. Loubet, S. Holmes, S. Mehta, D. Yang, A. Upham, S.-C. Seo, J. L. Herman, R. Johnson, Y. Zhu, P. Jamison, B. S. Haran, Z. Zhu, L. H. Vanamurth, S. Fan, D. Horak, H. Bu, P. J. Oldiges, D. K. Sadana, P. Kozlowski, D. McHerron, J. O'Neill, and B. Doris, "Extremely thin SOI (ETSOI) CMOS with record low variability for low power system-on-chip applications," in *IEDM Tech. Dig.*, 2009, pp. 49–52.

[8] Z. B. Zhang, S. C. Song, K. Choi, J. H. Sim, P. Majhi, and B. H. Lee, "An integratable dual metal gate/high-k CMOS solution for FD-SOI and MuGFET technologies," in *Proc. IEEE Int. SOI Conf.*, 2005, pp. 157–158.

[9] D. Pham, H. Luan, K. Mathur, B. Sassman, B. Nguyen, G. Brown, J.-W. Yang, J. Oh, P. Zeitzoff, and L. Larson, "Single metal gate with dual work functions for FD-SOI and UTB double gate technologies," in *Proc. IEEE Int. SOI Conf.*, 2006, pp. 25–26.

[10] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. Mclntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45 nm logic technology with high-k+ metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 dry patterning, and 100% Pb-free packaging," in *IEDM Tech. Dig.*, 2007, pp. 247–250.

[11] C. M. Lai, C. T. Lin, L. W. Cheng, C. H. Hsu, J. T. Tseng, T. F. Chiang, C. H. Chou, Y. W. Chen, C. H. Yu, S. H. Hsu, C. G. Chen, Z. C. Lee, J. F. Lin, C. L. Yang, G. H. Ma, and S. C. Chien, "A novel 'hybrid' high-k/metal gate process for 28 nm high performance CMOSFETs," in *IEDM Tech. Dig.*, 2009, pp. 655–658.

[12] C. Buj-Dufournet, F. Andrieu, O. Faynot, O. Weber, F. Allain, L. Tosti, C. Fenouillet-Béranger, D. Lafond, and S. Deleonibus, "Counter-doping as a solution for multi threshold voltage on FDSOI MOSFETs with a single TiN/$Hf0_2$ gate stack," presented at the Int. Conf. Solid State Devices and Materials (SSDM), Miyagi, Japan, 2009, Paper A-1-3.

[13] J.-P. Noel, O. Thomas, C. Fenouillet-Beranger, M.-A. Jaud, P. Scheiblin, and A. Amara, "A simple and efficient concept for setting up multi-V_T devices in thin BOX fully-depleted SOI technology," in *Proc. ESSDERC*, 2009, pp. 137–140.

[14] C. Fenouillet, O. Thomas, P. Perreau, J.-P. Noel, A. Bajolet, S. Haendler, L. Tosti, S. Barnola, R. Beneyton, C. Perrot, C. de Buttet, F. Abbate, F. Baron, B. Pernet, Y. Campidelli, L. Pinzelli, P. Gouraud, M. Casse, C. Borowiak, O. Weber, F. Andrieu, S. Denorme, F. Boeuf, O. Faynot, T. Skotnicki, K. K. Bourdelle, B. Y. Nguyen, and F. Boedt, "Efficient multi-VT FDSOI technology with UTBOX for low power circuit design," in *VLSI Symp. Tech. Dig.*, 2010, pp. 65–66.

[15] T. Ishigaki, R. Tsuchiya, Y. Morita, H. Yoshimoto, N. Sugii, T. Iwamatsu, H. Oda, Y. Inoue, T. Ohtou, T. Hiramoto, and S. Kimura, "Silicon on thin BOX (SOTB) CMOS for ultralow standby power with forward-biasing performance booster," in *Proc. ESSDERC*, 2008, pp. 198–201.

[16] T. Ernst and S. Cristoloveanu, "Buried oxide fringing capacitance: A new physical model and its implication on SOI device scaling and architecture," in *Proc. IEEE Int. SOI Conf.*, 1999, pp. 38–39.

[17] T. Ernst, C. Tinella, C. Raynaud, and S. Cristoloveanu, "Fringing fields in sub-0.1 μm fully depleted SOI MOSFETs: Optimization of the device architecture," *Solid State Electron.*, vol. 46, no. 3, pp. 373–378, Mar. 2002.

[18] C. Gallon, C. Fenouillet-Beranger, A. Vandooren, F. Boeuf, S. Monfray, F. Payet, S. Orain, V. Fiori, F. Salvetti, N. Loubet, C. Charbuillet, A. Toffoli, F. Allain, K. Romanjek, I. Cayrefourcq, B. Ghyselen, C. Mazure, D. Delille, F. Judong, C. Perrot, M. Hopstaken, P. Scheblin, P. Rivallin, L. Brevard, O. Faynot, S. Cristoloveanu, and T. Skotnicki, "Ultra-thin fully depleted SOI devices with thin BOX, ground plane and strained liner booster," in *Proc. IEEE Int. SOI Conf.*, 2006, pp. 17–18.

[19] M.-A. Jaud, P. Scheiblin, S. Martinie, M. Casse, O. Rozeau, J. Dura, J. Mazurier, A. Toffoli, O. Thomas, F. Andrieu, and O. Weber, "TCAD simulation vs. experimental results in FDSOI technology: From advanced mobility modeling to 6T-SRAM cell characteristics prediction," in *Proc. SISPAD*, 2010, pp. 283–286.

[20] Atlas, MixedMode SILVACO Athena, 2010.

[21] C. Fenouillet-Beranger, S. Denorme, P. Perreau, C. Buj, O. Faynot, F. Andrieu, L. Tosti, S. Barnola, T. Salvetat, X. Garros, M. Casse, F. Allain, N. Loubet, L. Pham-NGuyen, E. Deloffre, M. Gros-Jean, R. Beneyton, C. Laviron, M. Marin, C. Leyris, S. Haendler, F. Leverd, P. Gouraud, P. Scheiblin, L. Clement, R. Pantel, S. Deleonibus, and T. Skotnicki, "FDSOI devices with thin BOX and ground plane integration for 32 nm node and below," in *Proc. ESSDERC*, 2008, pp. 206–209.

[22] C. Fenouillet-Beranger, P. Perreau, S. Denorme, L. Tosti, F. Andrieu, O. Weber, S. Barnola, C. Arvet, Y. Campidelli, S. Haendler, R. Beneyton, C. Perrot, C. de Buttet, P. Gros, L. Pham-Nguyen, F. Leverd, P. Gouraud, F. Abbate, F. Baron, A. Torres, C. Laviron, L. Pinzelli, J. Vetier, C. Borowiak, A. Margain, D. Delprat, F. Boedt, K. Bourdelle, B.-Y. Nguyen, O. Faynot, and T. Skotnicki, "Impact of a 10 nm ultra-thin BOX (UTBOX) and ground plane on FDSOI devices for 32 nm node and below," in *Proc. ESSDERC*, 2009, pp. 89–91.

[23] Q. Liu, A. Yagishita, N. Loubet, A. Khakifirooz, P. Kulkarni, T. Yamamoto, K. Cheng, M. Fujiwara, J. Cai, D. Dorman, S. Mehta, P. Khare, K. Yako, Y. Zhu, S. Mignot, S. Kanakasabapathy, S. Monfray, F. Boeuf, C. Koburger, H. Sunamura, S. Ponoth, A. Reznicek, B. Haran, A. Upham, R. Johnson, L. F. Edge, J. Kuss, T. Levin, N. Berliner, E. Leobandung, T. Skotnicki, M. Hane, H. Bu, K. Ishimaru, W. Kleemeier, M. Takayanagi, B. Doris, and R. Sampson, "Ultra-thin-body and BOX (UTBB) fully depleted (FD) device integration for 22 nm node and beyond," in *VLSI Symp. Tech. Dig.*, 2010, pp. 61–62.

[24] F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J.-P. Noel, C. Fenouillet-Beranger, J.-P. Mazellier, P. Perreau, T. Poiroux, Y. Morand, T. Morel, S. Allegret, V. Loup, S. Barnola, F. Martin, J.-F. Damlencourt, I. Servin, M. Casse, X. Garros, O. Rozeau, M.-A. Jaud, G. Cibrario, J. Cluzel, A. Toffoli, F. Allain, R. Kies, D. Lafond, V. Delaye, C. Tabone, L. Tosti, L. Brevard, P. Gaud, V. Paruchuri, K. K. Bourdelle, W. Schwarzenbach, O. Bonnin, B.-Y. Nguyen, B. Doris, F. Buf, T. Skotnicki, and O. Faynot, "Low leakage and low variability ultra-thin body and buried oxide (UTBB) SOI technology for 20 nm low power CMOS and beyond," in *VLSI Symp. Tech. Dig.*, 2010, pp. 57–58.

[25] J.-P. Colinge, *Silicon-On-Insulator Technology: Materials to VLSI*, 3rd ed. New York: Springer-Verlag, 1997.

[26] A. Keshavarzi, S. Ma, S. Narendra, B. Bloechel, K. Mistry, T. Ghani, S. Borkar, and V. De, "Effectiveness of reverse body bias for leakage control in scaled dual Vt CMOS ICs," in *Proc. ISLPED*, 2001, pp. 207–212.

[27] M. Khater, J. Cai, R. H. Dennard, J. Yau, C. Wang, L. Shi, M. Guillorn, J. Ott, Q. Ouyang, and W. Haensch, "FDSOI CMOS with dielectrically-isolated back gates and 30 nm L_G high-κ/metal gate," in *VLSI Symp. Tech. Dig.*, 2010, pp. 43–44.

[28] J.-P. Noel, O. Thomas, M.-A. Jaud, C. Fenouillet-Beranger, P. Rivallin, P. Scheiblin, T. Poiroux, F. Boeuf, F. Andrieu, O. Weber, O. Faynot, and A. Amara, "UT2B-FDSOI device architecture dedicated to low power design techniques," in *Proc. ESSDERC*, 2010, pp. 210–213.

[29] D. E. Lackey, P. S. Zuchowski, T. R. Bednar, D. W. Stout, S. W. Gould, and J. M. Cohn, "Managing power and performance for system-on-chip designs using voltage islands," in *Proc. ICCAD*, 2002, pp. 195–202.

[30] F. Andrieu, C. Fenouillet-Béranger, O. Weber, S. Baudot, C. Buj, J. P. Noel, O. Thomas, O. Rozeau, P. Perreau, L. Tosti, L. Brévard, and O. Faynot, "Ultrathin body and BOX SOI and sSOI for low power application at the 22 nm technology node and below," presented at the Int. Conf. Solid State Devices and Materials (SSDM), Miyagi, Japan, 2009, Paper A-1-1.

[31] O. Weber, F. Andrieu, J. Mazurier, M. Casse, X. Garros, C. Leroux, F. Martin, P. Perreau, C. Fenouillet-Beranger, S. Barnola, R. Gassilloud, C. Arvet, O. Thomas, J.-P. Noel, O. Rozeau, M.-A. Jaud, T. Poiroux, D. Lafond, A. Toffoli, F. Allain, C. Tabone, L. Tosti, L. Brevard, P. Lehnen, U. Weber, P. K. Baumann, O. Boissiere, W. Schwarzenbach, K. Bourdelle, B.-Y. Nguyen, F. Boeuf, T. Skotnicki, and O. Faynot, "Work-function engineering in gate first technology for multi-V_T dual-gate FDSOI CMOS on UTBOX," in *IEDM Tech. Dig.*, 2010, pp. 3.4.1–3.4.4.

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During his Ph.D. studies, he worked at the Commissariat à l'Énergie Atomique/Laboratoire d'Electronique et de Technologie de l'Information (CEA–LETI), Micro and Nanotechnology Innovation Centre, Grenoble, France, on the fabrication and characterization of advanced complementary metal–oxide–semiconductor (CMOS) transistors featuring strained Si and Ge channels and high-*k*/metal gate stacks. Between 2006 and 2007, he was a Postdoctoral Fellow at the University of Tokyo, Tokyo, Japan, where he was engaged in research on the physics and characterization of strained-Si MOS devices. In November 2007, he joined CEA–LETI as a Research Staff Member. His current research interest is on the planar fully depleted silicon-on-insulator CMOS integration for sub-32-nm technology nodes.

Thierry Poiroux received the M.S. degree from Ecole Centrale Paris, Paris, France, in 1995 and the Ph.D. degree from the University of Nantes, Nantes, France, in 2000.

His Ph.D. work was carried out at the Commissariat à l'Énergie Atomique/Laboratoire d'Electronique et de Technologie de l'Information (CEA–LETI), Grenoble, France, and Matra MHS on plasma process-induced damage. In April 2000, he joined CEA–LETI as a Research Staff Member. Until 2002, he was involved in partially and fully depleted silicon-on-insulator (SOI) process integration and compact modeling. From 2002 to 2007, he worked on advanced device architectures and was in charge of multiple-gate device modeling and planar double gate process integration. In 2007, he started an activity on graphene, which is a promising material for the beyond complementary metal–oxide–semiconductor era. Since 2011, he has been the Head of the Innovative Device Laboratory of CEA–LETI. He has authored or coauthored five book chapters and about 100 papers and communications in the fields of plasma process-induced damage; SOI; and multiple-gate device physics, fabrication, characterization, and modeling. He is the holder of 11 patents on novel devices and process integration.

Claire Fenouillet-Beranger was born in Grenoble, France, in 1974. She received the Postgraduate Diploma in microelectronics and the Ph.D. degree from Institut National Polytechnique de Grenoble, Grenoble, France, in 1998 and 2001, respectively.

In 1998, she joined the Commissariat à l'Énergie Atomique/Laboratoire d'Electronique et de Technologie de l'Information (CEA–LETI), Grenoble, where she carried out her Ph.D. work on the integration and characterization of silicon-on-insulator devices. Since 2001, she has been a CEA–LETI Assignee in advanced Research and Development, STMicroelectronics Center, Crolles, France, on fully depleted SOI technology platform development and characterization.

Pierrette Rivallin was born in France, in 1955.

In 1994, she joined the technology computer-aided design (CAD) simulation group after a long period of developing software for medicine and magnetic domains. She is in charge of the development of numerical simulation tools in the specific fields of ionic implantation, impurities diffusion, and thermal oxidation, as well as the integration of these tools into advanced technology CAD systems for microelectronic engineering.

Pascal Scheiblin received the Ph.D. degree in physics from Université de Paris XI, Orsay, France, in 1990.

He worked several years on implementation of physical models in technology computer-aided design (TCAD) tools, in particular, advanced dopant diffusion models. He joined the Commissariat à l'Énergie Atomique/Laboratoire d'Electronique et de Technologie de l'Information, Grenoble, France, in 1998, in charge of the development of methodologies for TCAD calibration. His current research interest is TCAD simulation for ultimate fully depleted metal–oxide–semiconductor field-effect transistors and silicon photovoltaic devices.

François Andrieu received the M.S. and Ph.D. degrees in physics and nanoelectronics from the Institut National Polytechnique de Grenoble, Grenoble, France, in 2002 and 2005, respectively.

In 2005, he joined the Commissariat à l'Énergie Atomique/Laboratoire d'Electronique et de Technologie de l'Information, Grenoble, as a Research Engineer. He is a Senior Scientist for the French Observatory of Micro and Nanotechnology. His work is currently dedicated to the planar fully depleted silicon-on-insulator complementary metal–oxide–semiconductor technology for the 20-nm node and below. He has managed or been involved in several European projects (such as the MEDEA+ Silonis and Decisif ones) and industrial projects (joint programs with Soitec and STMicroelectronics/IBM). He is the author or coauthor of 111 journal articles or conference abstracts and six invited papers and is the holder of four patents.

Dr. Andrieu received the Best Young Researcher Paper Award from the European Solid State Device Research Conference in 2005.

Maud Vinet received the B.S. degree in physics from the Ecole Nationale Supérieure de Physique de Grenoble, Grenoble, France, the M.Sc. degree in experimental methods for physics from the Université Joseph Fourier, Grenoble, in 1997, and the Ph.D. degree from the Institut National Polytechnique de Grenoble, Grenoble, in 2001.

While she was working on her Ph.D. degree, she developed low-temperature scanning tunnelling microscopy and spectroscopy in the Commissariat à l'Énergie Atomique, Grenoble. She joined the Commissariat à l'Énergie Atomique/Laboratoire d'Electronique et de Technologie de l'Information (CEA–LETI), Grenoble, in 2001 as a Device Engineer in the Electronics Nanodevices Laboratory. For five years, she was involved in advanced-devices integration from double-gate to single-electron transistors. She was then in charge of 3-D monolithic integration for complementary metal–oxide–semiconductor applications. Her work consisted in finding innovative technological solutions to fit with advanced devices electrical specifications. In 2009, she joined IBM at Albany as a CEA–LETI Assignee to work on extremely thin silicon-on-insulator (SOI) integration. In 2010, she was a member of the technical committee of the International Conference on Very Large Scale Integration system-on-a-chip. She is the author or coauthor of about 90 papers (conferences and journals) and the holder of 30 patents related to nanotechnology.

Dr. Vinet received the Young Researcher Award at the Solid States Devices and Materials Conference in Tokyo in 2004. From 2007 to 2009, she was a member of the technical committee of the SOI conference.

Olivier Rozeau, photograph and biography not available at the time of publication

Frédéric Boeuf was born in 1972. He received the M.Eng. and M.S. degrees from the Institut National Polytechnique de Grenoble, Grenoble, France, in 1996, and the Ph.D. degree from the University Joseph Fourier of Grenoble, Grenoble, in 2000.

In 2000, he joined STMicroelectronics, Crolles, France, where he worked on the predevelopment phase of 65- and 45-nm complementary metal–oxide–semiconductor (CMOS) technologies. He actively participated to the development of the Model for Assessment of cmoS Technologies And Roadmaps (MASTAR) model, used for the definition of the 2005 to 2009 editions of the "International Technology Roadmap for Semiconductors" to which he collaborated. He is currently managing the Advanced Devices Technology group working toward the 14-nm CMOS thin-films technology and disruptive technologies. He is an Industrial Advisor of several Ph.D. theses in the field of device integration and modeling. His fields of expertise are semiconductor physics and CMOS device physics. He has authored or coauthored over 135 publications, including books chapters, invited talks, and presented papers at several conferences in the fields mentioned. He submitted several patents.

Dr. Boeuf served in several European commission-funded projects as work package or subproject leader. He also served as the Chair of the "CMOS Devices" technical subcommittee and the European Arrangement Chair of the International Electron Device Meeting Conference in 2007 and 2008–2009, respectively. He has been a member of the "Device Physics" subcommittee of the "Solid State Devices and Materials" Conference since 2006 and participated to the Technical Program Committee of the European Solid State Device Research Conference in from 2004 to 2005.

Olivier Faynot received the M.S. and Ph.D. degrees from the Institut National Polytechnique de Grenoble, Grenoble, France, in 1991 and 1995, respectively.

His doctoral research was related to the characterization and modeling of deep submicron fully depleted silicon-on-insulator devices fabricated on ultra-thin silicon-implanted oxide wafers. He joined the Commissariat à l'Énergie Atomique/Laboratoire d'Electronique et de Technologie de l'Information (CEA–LETI), Grenoble, in 1995, working on simulation and modeling of deep submicron fully and partially depleted silicon-on-insulator (SOI) devices. His main activity was the development of a dedicated partially depleted SOI SPICE model, which is called LETISOI. From 2000 to 2002, he was involved in the development of a sub-0.1-μm partially depleted SOI technology. From 2003 to 2007, he was leading the development of advanced single- and multiple-gate fully depleted SOI technologies with high-κ and metal gate. From 2008 to 2010, he managed the innovative devices laboratory at CEA–LETI. Since 2011, he is responsible of the Microelectronic Component Section at CEA–LETI. He is the author or coauthor of more than 140 scientific publications on SOI in journals and international conferences.

Dr. Faynot has been successively in the committees of main international conferences such as the International Electron Device Meeting, the symposium on Very Large Scale Integration Technology, the IEEE International SOI conference, and the Solid State Device and Materials Conference since 2001.

Amara Amara (M'95–SM'04) received the Higher Degree Research (Confirmation of Leading Research Capabilities) from Evry University, Evry, France, and the M.S. degree in microelectronics and computer science and the Ph.D. degree in computer science from Paris VI University, Paris, France, in 1989 and 1984, respectively.

He is currently the Deputy Managing Director of Institut Supérieur d'Electronique de Paris, Paris, in charge of Research and International Cooperation. His research interests are mainly related to low-power circuit design and circuit and technology interactions for advanced electron devices (silicon-on-insulator (SOI), double-gate fully depleted SOI, ultra-thin body SOI, 3-D integration, etc.).

Dr. Amara is the Vice President of the French IEEE Section and was a former IEEE Circuits and Systems Society Board-of-Governors Member.