Multibit Σ–Δ PWM Digital Controller IC for DC–DC Converters Operating at Switching Frequencies Beyond 10 MHz

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***Abstract*—An integrated digital controller for dc–dc switch-mode power supplies (SMPS) used in portable applications is introduced. The controller has very low power consumption, fast dynamic response, and can operate at programmable constant switching frequencies exceeding 10 MHz. To achieve these characteristics, three novel functional blocks, a digital pulse-width modulator based on second-order sigma–delta concept (Σ–Δ DPWM), dual-clocking mode compensator, and nonlinear analog-to-digital converter are combined. In steady state, to minimize power consumption, the controller is clocked at a frequency lower than SMPS switching frequency. During transients the clock rate is increased to the switching frequency improving transient response. The controller integrated circuit (IC) is fabricated in a standard 0.18-μm process and tested with a 750-mW buck converter prototype. Experimental results show the controller current consumption of 55 μA/MHz and verify closed-loop operation at programmable switching frequencies up to 12.3 MHz. Simulation results indicating that this architecture can potentially support operation at switching frequencies beyond 100 MHz are also presented.**

***Index Terms*—Digital control, high-frequency low-power dc–dc converter, second-order sigma–delta DPWM.**

I. Introduction

DIGITAL control offers attractive features that can result in significant enhancements of low-power switch-mode power supplies (SMPS) characteristics. It has been shown that digital realization allows the development of new control techniques that increase overall efficiency of the power stage through multimode operation [1]–[3], enable active monitoring of SMPS parameters and subsequent auto-tuning [4]–[7], and improve transient response by avoiding gain and parameter variation problems characteristic for analog implementations [8], [9]. Also, with the support of automated design tools and hardware description languages (HDL), digital systems can be designed in a short time and easily modified. These tools also allow simple transfer of the designs from one implementation technology to another, i.e., design portability. This is highly desirable in modern IC design, where the implementation technologies are changing constantly.

In spite the fact that all of these characteristics are very suitable for low-power applications, in miniature battery-powered devices such as mobile phones, PDA-s, and MP3 players, pulsewidth-modulated (PWM) analog-controlled SMPS are almost exclusively used. This is mostly due to the absence of low-power digital architectures that can support operation at constant switching frequencies significantly higher than 1 MHz. The power consumption of the existing digital controllers is often comparable to that of the supplied low-power electronic loads resulting in a poor overall efficiency of the SMPS. At higher switching frequencies the analog controllers take much less power, and consequently are more suitable solution, even though they do not posses most of the abovementioned features.

This arrangement, involving analog controlled SMPS to supply mostly digital portable devices, creates problems in the realization of advanced power management techniques for battery saving [10]. Due to limited analog hardware flexibility, techniques such as dynamic voltage scaling (DVS) and adaptive body biasing (ABB) cannot be easily implemented without a significant increase in hardware complexity.

One of the main limitations to maximum switching frequency at which digital controllers can be effectively used in low-power applications is the power consumption of digital pulsewidth modulator (DPWM). It is usually proportional to the product of the switching frequency and the DPWM resolution, which needs to be sufficiently high to eliminate undesirable limit-cycle oscillations [11], [12]. In addition, other functional blocks of digital controllers, analog-to-digital converters and compensators, usually take a significant amount of power, resulting in poor efficiency of low-power SMPS.

On the other hand, alternative digital architectures that do not require PWM signals, such as hysteretic and pulse-train modulation, usually operate at nonconstant switching frequencies creating wide-bandwidth noise, and as such, are not preferable in sensitive electronic devices. Because of that, constant-frequency DPWM controllers are still very interesting for low-power applications.

Recent research publications [13]–[16] demonstrate high-resolution low-power DPWM controllers that operate at switching frequencies between 400 kHz and 2 MHz. Compared to their readily available analog counterparts [17] the presented controllers still operate at five to ten times lower switching frequencies. Consequently, they require significantly larger power

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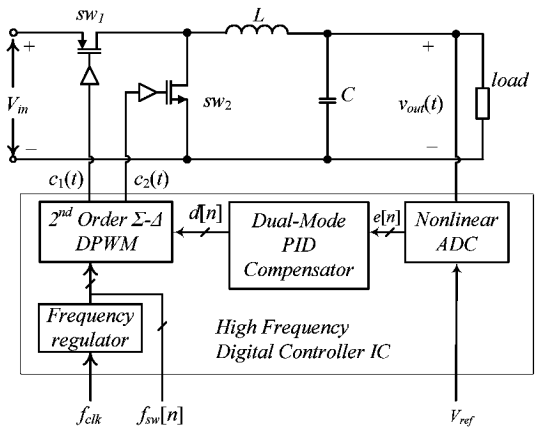


Fig. 1. Buck converter regulated by high-frequency multibit DPWM controller IC.

stages that nullify most of the digital control advantages. Even more, these digital systems will probably not be able to regulate upcoming SMPS that are expected to operate at switching frequencies beyond 10 MHz [18], [19]. The higher frequency DPWM architecture presented in [20] cannot be used in portable devices either. It is designed for higher power SMPS, where the power consumption of the controller is not so crucial. In addition at maximum switching frequency of 15 MHz the resolution of the DPWM is only 6 b. In most of the cases, this resolution is not sufficient for the elimination of limit-cycle oscillations.

In this paper, our main goal is to present a new architecture of very low-power digital PWM controller IC for dc–dc SMPS that can operate at programmable constant switching frequencies higher than 10 MHz and has very fast load-transient response. This architecture allows utilization of digital control advantages in existing and upcoming low-power SMPS and can be implemented with a simple hardware requiring very small silicon area.

Fig. 1 shows a block diagram of the new digital controller IC regulating operation of a synchronous buck power stage. To achieve low power consumption and operation at programmable constant switching frequencies beyond 10 MHz, the following new architectures of basic functional blocks are developed:

1. a multibit second-order sigma–delta digital pulsewidth modulator (second-order Σ–Δ DPWM);
2. a dual-clocking mode compensator;
3. a nonlinear analog-to-digital converter (ADC).

In addition, we developed a frequency-regulation block that allows synchronization of this self-clocking system with an external clock.

Based on the values of voltage $V_{\rm ref}$ and the converter output $v_{\rm out}$ (t), the nonlinear ADC having nonuniform quantization steps creates digital error signal $e[n]$. This value is then processed by the dual—mode PID compensator that produces digital duty ratio control variable $d[n]$. Depending on the conditions in the SMPS circuit, the PID compensator operates in one of two possible modes. In steady state, to reduce power consumption, the compensator is clocked at a frequency lower than the switching frequency. During disturbances, the clock is increased to improve controller transient response.

The second-order Σ–Δ DPWM creates constant frequency PWM control signals c_1 (t) and c_2 (t) for the power stage. It utilizes a second-order Σ–Δ modulator to achieve high effective resolution and operation without noise related problems, typically existing in first-order Σ–Δ DPWM implementations [21]. The controller switching frequency can be either digitally programmed using an external signal $f_{\rm sw}[n]$ or it can be synchronized with an external clock, through the frequency regulator.

The following section briefly reviews operation of conventional Σ–Δ digital pulsewidth modulators and addresses problems of slow convergence and low frequency tones appearing in first-order Σ–Δ structures. This section also shows the new second-order Σ–Δ DPWM architecture that minimizes effects of mentioned problems. In addition it also describes operation of the new frequency regulator. Section III gives details on the operation and implementation of dual clocking mode compensator. In Section IV, the nonlinear ADC is described. Section V presents simulations and experimental results obtained with a fabricated chip that utilizes the new controller architecture. In Section VI, the main results of this paper are summarized.

II. Multibit Digital PWM Based on a Second-Order Σ–Δ Modulator

Most of the existing DPWM architectures [22] are not well-suited for operation at switching frequencies beyond 10 MHz. They either rely on power consuming counters operating at frequencies several-orders of magnitude higher than the converter switching frequency or use ring-oscillator structures. In the later case, the resolution of DPWM, i.e., its time quantization steps, is constrained by finite propagation time of ring oscillator delay cells. For example, a 10-MHz ring-oscillator based DPWM having 10-b resolution requires cells whose propagation time is less than 100 ps. Today, such small time delays can be achieved only with the most advanced and expensive IC implementation technologies (0.18-μm CMOS and smaller). Hence, the linearity and regulation of switching frequency can be compromised. These problems will become even more prominent if the converters operating at switching frequencies as high as 100 MHz [19] find wider use. Hybrid architectures [14]–[16] combining a counter and a delay line suffer from the same problem since the resolution of the DPWM is also limited with propagation times of delay cells.

To minimize requirements on the resolution of DPWM, dithering [11] and sigma–delta architectures that increase effective resolution of the DPWM through averaging process are developed [23]–[28].

A. Principle of Operation

As illustrated in Fig. 2(a), Σ–Δ DPWM consists of a low-resolution low-power DPWM (core DPWM) capable of operating at high switching frequencies and a Σ–Δ modulator, which improves effective resolution of the core DPWM. In the design shown in the figure, the effective resolution of a 4-b DPWM core is improved to 10 b. The Σ–Δ operation is based on the well-known noise-shaping concept widely used in analog-to-digital and digital-to-analog converters [21], [30].

Over several switching cycles, the Σ–Δ modulator varies $d_{\rm LR}[n]$, the low-resolution input of the core DPWM, between

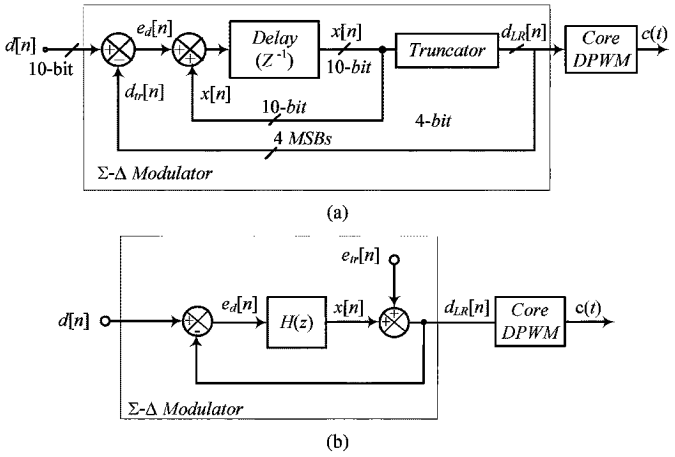


Fig. 2. First-order Σ–Δ: (a) simplified block diagram and (b) equivalent model.

few of 16 possible values (0, 0.0625, 0.125, ..., and 0.9325) to achieve a high-resolution average duty ratio value, equal to the 10-b input $d[n]$. When connected to a switching converter power stage, as shown in Fig. 1, no additional hardware is needed for averaging. It is naturally performed with the filtering components of the power stage.

The Σ-Δ modulator itself consists of two adders, a truncator, and delay blocks forming two feedback loops, and it can be modeled as shown in Fig. 2(b) [28], [29]. The inner loop behaves as an integrator

$$H(z) = \frac{X(z)}{E_d(z)} = \frac{z^{-1}}{1 - z^{-1}} \tag{1}$$

that forces the average value of $e_d[n]$, the difference between $d[n]$ and $d_{\rm tr}[{\rm n}]$, to zero. Fig. 2(b) also shows truncation noise, $e_{\rm tr}[{\rm n}]$, which models the process of sending only four most significant bits (MSBs) of the integrator output, $x[n]$, to the core DPWM. In this case, z-transform of $d_{\rm LR}[n]$ becomes

$$D_{\rm LR}(z) = \frac{H(z)}{1 + H(z)} D(z) + \frac{1}{1 + H(z)} E_{\rm tr}(z). \tag{2}$$

This equation shows how the transfer function $H(z)$ influences the truncated signal. When $H(z)$ is large in magnitude, i.e., $||H(z)|| \gg 1$, the high-resolution input is almost unchanged, the quantization error is suppressed, and, consequently, $d_{\rm LR}[n]$ becomes approximately equal to the high resolution input $d[n]$. The part of the equation describing error attenuation

$$N_{\rm TF}(z) = \frac{1}{1 + H(z)} \tag{3}$$

is called the noise-shaping transfer function, whose order usually defines the order of the Σ-Δ modulator. For the case given by (1), $H(z)$ forms a first-order modulator that has infinite gain at zero frequency, i.e., at $z = 1$, resulting in the complete elimination of dc quantization error, i.e.,

$$D_{\rm LR}(z)|_{H(z=1)\to\infty} = D(z). \tag{4}$$

B. Problems of Low-Frequency Tones and Slow Convergence

Several publications [23], [24], [26]–[28] show DPWM architectures based on various modifications of first-order sigma–delta concept. These systems increase switching frequency, but still require a core DPWM with relatively high resolution (6 to 8 b) and often suffer from low-frequency noise at the converter output [26]. Additionally, in most of the realizations, the bandwidth of voltage control loop is significantly reduced.

The slow averaging and noise related problems can be analyzed by observing Table I showing signal values for Σ-Δ DPWM of Fig. 2(a) over 25 switching cycles for a randomly selected input $d[n]$. It can be seen that the average value of the core DPWM relatively slowly approaches the high-resolution input, meaning that $d[n]$ needs to remain constant over a large number of switching cycles to allow averaging. This condition is usually satisfied with a voltage loop whose bandwidth is limited to minimize $d[n]$ variations [26]. As a result, the dynamic response of Σ-Δ DPWM controllers is often compromised.

The table also demonstrates low-frequency periodic behavior of the core DPWM output (shadowed sequence), known as tones, which introduce low-frequency noise. The tones exist when the high-resolution input $d[n]$ does not belong to a limited set of possible $d_{\rm LR}[n]$ values. In that case, first-order Σ-Δ modulator periodically changes its low-resolution output between two adjacent levels resulting in oscillations whose frequency depends on d [n]. For example, when the 10-b value $d[n]$ is a binary equivalent of 528 (integer arithmetic assumed), corresponding to the $528/1024$ duty ratio value, the duty ratio of the core DPWM changes as follows $8/16, 8/16, 8/16, 9/16, 8/16, 8/16, 8/16, 9/16, 8/16 \ldots$ The average value of this sequence attains the desired value over four switching cycles, i.e., $528/1024 = 1/4(3 \cdot 8/16 + 9/16)$. At the same time, the sequence introduces tones at $1/4$ the switching frequency.

In an SMPS with a Σ-Δ DPWM (as the one shown in Fig. 1), an effective suppression of tones is only possible when the frequency of tones is significantly higher than the corner frequency of the power stage. For certain values of $d[n]$, this condition is not satisfied and a low frequency noise appears at the output. Even more, the tones can be amplified when their frequency coincides with the corner frequency of power stage having high quality factor Q [29]. To demonstrate this effect in Fig. 3 we show experimental results obtained with a 9 to 5 V, 400-kHz buck converter operating with the first-order Σ-Δ DPWM of Fig. 2(a). The LC components of the converter are selected to obtain the corner frequency of approximately 6 kHz. For $d[n] = 513$, which results in a tone at $1/64$ of the switching frequency, large oscillations of the output voltage can be observed. The oscillations are tones multiplied by the gain of converter control-to-output transfer function $G_{\rm vd}(s)$ [29].

Using the analysis presented in [21], it is easy to calculate frequency of tones for any input $d[n]$ and show that for a Σ-Δ DPWM having N-bit input and $N_{\rm core}$-bit core DPWM the lowest tone frequency is

$$f_{\rm tone\_min} = \frac{1}{2^{(N - N_{\rm core})}} \cdot f_{\rm sw}. \tag{5}$$

TABLE I
STATES OF THE SIGNALS OF A FIRST-ORDER SIGMA–DELTA DPWM AND AVERAGE DUTY RATIO VALUE CALCULATED OVER N SWITCHING CYCLES

n	$d[n]$	Desired Duty ratio	$e[n]$	$x[n+1]$	$x[n]$	$d_{LR}[n]$	Average Duty Ratio
1	200	0.1953	0.1953	0.1953	0.0000	0.0000	0.0000
2	200	0.1953	0.0078	0.2031	0.1953	0.1875	0.0937
3	200	0.1953	0.0078	0.2109	0.2031	0.1875	0.1250
4	200	0.1953	0.0078	0.2187	0.2109	0.1875	0.1406
5	200	0.1953	0.0078	0.2265	0.2187	0.1875	0.1500
6	200	0.1953	0.0078	0.2343	0.2265	0.1875	0.1562
7	200	0.1953	0.0078	0.2421	0.2343	0.1875	0.1607
8	200	0.1953	0.0078	0.2500	0.2421	0.1875	0.1640
9	200	0.1953	-0.05469	0.1953	0.2500	0.2500	0.1736
10	200	0.1953	0.0078	0.2031	0.1953	0.1875	0.1750
11	200	0.1953	0.0078	0.2109	0.2031	0.1875	0.1761
12	200	0.1953	0.0078	0.2187	0.2109	0.1875	0.1770
13	200	0.1953	0.0078	0.2265	0.2187	0.1875	0.1778
14	200	0.1953	0.0078	0.2343	0.2265	0.1875	0.1785
15	200	0.1953	0.0078	0.2421	0.2343	0.1875	0.1791
16	200	0.1953	0.0078	0.2500	0.2421	0.1875	0.1796
17	200	0.1953	-0.05468	0.1953	0.2500	0.2500	0.1838
18	200	0.1953	0.0078	0.2031	0.1953	0.1875	0.1840
19	200	0.1953	0.0078	0.2109	0.2031	0.1875	0.1842
20	200	0.1953	0.0078	0.2187	0.2109	0.1875	0.1843
21	200	0.1953	0.0078	0.2265	0.2187	0.1875	0.1845
22	200	0.1953	0.0078	0.2343	0.2265	0.1875	0.1846
23	200	0.1953	0.0078	0.2421	0.2343	0.1875	0.1847
24	200	0.1953	0.0078	0.2500	0.2421	0.1875	0.1849

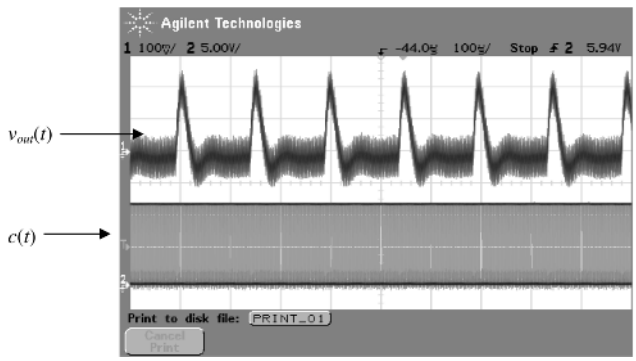


Fig. 3. Output voltage of experimental converter affected by low-frequency tones of first-order Σ-Δ PWM. Ch1 (ac-100 mV/div): output voltage; Ch2 (dc-5 V/div): PWM signal $c(t)$.

This equation also explains why in most of the existing Σ-Δ architectures [23]–[26] only a modest improvement of the core DPWM resolution is achieved. To eliminate the noise, the difference between the effective and core resolution ($N-N_{\text{core}}$ of (5)) is minimized keeping the tones at frequencies higher than power stage corner frequency. It should be noted that the negative effect of low-frequency tones usually cannot be eliminated with a faster voltage loop. As described above, such an attempt would cause faster $d[n]$ changes, degradation of effective DPWM resolution, and undesirable limit cycling of the compensator [11].

C. Second-Order Sigma–Delta DPWM

The problems of slow convergence toward high-resolution input and low-frequency tones existing in first-order Σ-Δ modulators have been extensively analyzed in research related to oversampling ADCs and digital-to-analog converters (DACs) [21], [30]. It has been shown that second-order Σ-Δ architectures strongly suppress low-frequency tones and have faster convergences. In the switching converter presented in [32], these advantages are recognized and a single-bit analog second-order Σ-Δ modulator is effectively used to improve output regulation of a pulse-train digital controller by spreading the spectrum of its output voltage ripple. This single-bit system still operates at a variable switching frequency that increases the current stress of power stage components and, consequently, requires larger and slower semiconductor switchers.

In this paper, we show a new second-order multibit Σ-Δ DPWM architecture that allows operation at programmable constant switching frequencies. The second-order multibit Σ-Δ DPWM also minimizes the abovementioned tone-related problems of first-order architectures allowing the use of a low-resolution low-power core DPWM to achieve switching frequencies beyond 10 MHz.

The design of second-order multibit Σ-Δ DPWM, shown in Fig. 6, is inspired by power DAC [24], [25] architectures. However, the main difference is in the system complexity. Since the DPWM does not require a very fast power-consuming ADC in feedback path (in this case only a truncated signal is sent back) its implementation is significantly simpler, and can be fully realized with digital components.

The system of Fig. 4 is a 10-b second-order sigma–delta with a 4-b core DPWM. Compared to the previously shown first-order implementation the main difference is in transfer function H (z) [Fig. 2(b)]. In this case, two delay blocks, an adder, and multiplier form the discrete-time transfer function

$$H(z) = \frac{X(z)}{E_d(z)} = \frac{z^{-1}}{(1-z^{-1})^2} \tag{6}$$

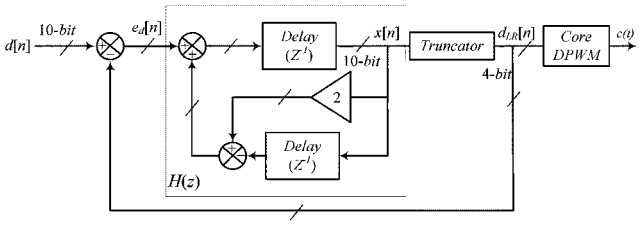


Fig. 4. Block diagram of a 10-b, second-order, Σ-Δ DPWM having 4-b core.

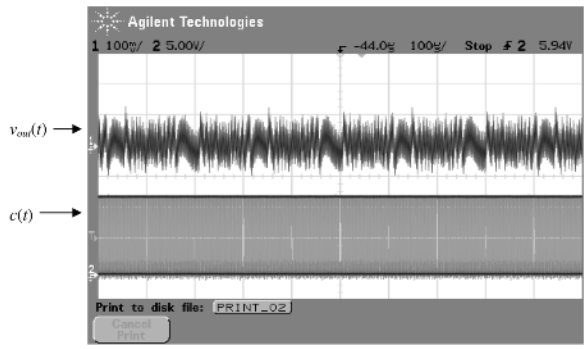


Fig. 5. Output of experimental switching converter regulated with second-order Σ-Δ DPWM. Ch1 (ac-100 mV/div): Output voltage $v_{\rm out}(t)$; Ch2 (dc-5 V/div): PWM signal $c(t)$.

which results in the desired second-order noise transfer function $N_{\rm TF}(z)$ described with (3).

The effect of the second-order sigma–delta on the tones suppression can be explained through the well-known noise shaping analysis [21], [30]. It shows that a second-order system moves the truncation noise, and consequently, tones to higher frequencies where the attenuation of the output low-pass filter is stronger.

To demonstrate positive effect of the second-order Σ-Δ DPWM in the experimental system described in Section I-B, the first-order Σ-Δ DPWM is replaced with the system of Fig. 4. The waveforms of Fig. 5 demonstrate that the low-frequency tones shown in Fig. 3 are almost completely eliminated even though the resolution of the core DPWM is still low (4 b).

The noise-shaping analysis can also be used to show that the effective resolution of a second-order sigma–delta DPWM, which is clocked at the switching frequency $f_{\rm sw}$, is [30]

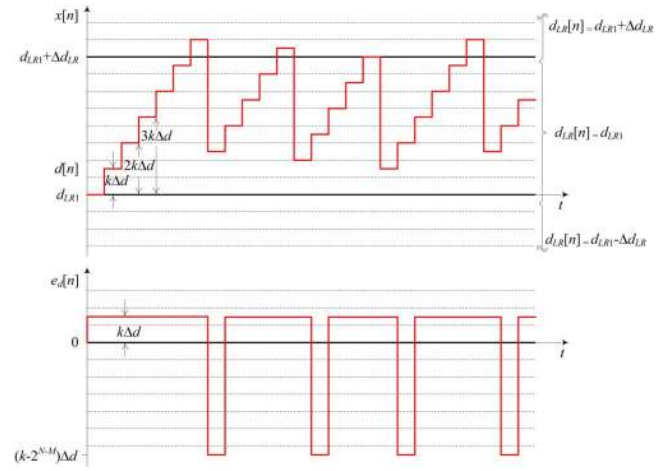
$$N_{\rm DPWM} \approx N_{\rm core} + 2.5\log_2\left(\frac{f_{\rm sw}}{f_{\rm update}}\right) \tag{7}$$

where $T_{\rm update} = 1/f_{\rm update}$ is the time rate at which the high-resolution input $d[n]$ is updated. Accordingly, for the system of Fig. 4, $d[n]$ should be updated at $f_{\rm update} = f_{\rm sw}/8$ to achieve effective resolution of 10 b using 4-b core DPWM.

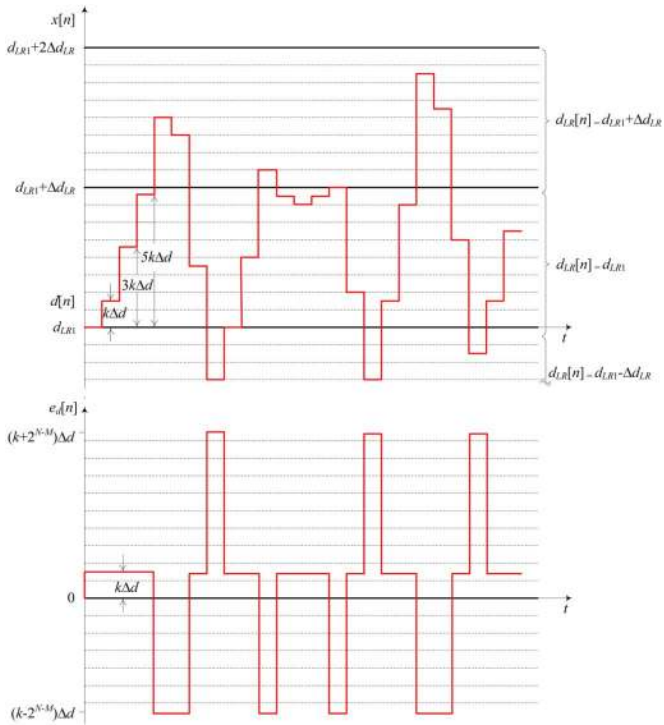
Alternatively, the influence of the second-order Σ-Δ can be observed through a comparison of its response to a step change $d[n]$ with the same response of a first-order Σ-Δ DPWM. This process is described with the following equations and corresponding diagrams of Fig. 6(a) and (b).

Let us assume that the following step input:

$$\begin{aligned} d[n] &= d_{\rm LR1},\ \text{for } n < 0 \\ d[n] &= d_{\rm LR1} + k\cdot\Delta d,\ \text{for} n \geq 0 \end{aligned} \tag{8}$$



(a)



(b)

Fig. 6. Signal waveforms of a (a) first-order Σ-Δ DPWM and (b) second-order sigma–delta DPWM.

is applied to the inputs of a first-order and a second-order Σ-Δ DPWM. The initial value $d_{\rm LR1}$ belongs to the limited set of possible low-resolution core DPWM inputs, and then, a step equal to k least significant bits of $d[n]$ occurs. It is also assumed that the increment is smaller than the quantization step of the core DPWM,

$$\Delta d_{\rm core} = 2^{(N-N_{\rm core})}\Delta d \tag{9}$$

where, as mentioned earlier, N is the number of bits of $d[n]$. This type of step function is selected to simplify the analysis. The same results can be easily obtained for any other step and initial condition.

A signal-flow analysis of the system illustrated in Fig. 2(a) shows that the inner loop output $x[n]$ and $e_d[n]$ change as follows:

$$x[n+1] = e_d[n] + x[n] \quad \text{, where} \tag{10}$$

$$e_d[n] = d[n] - d_{\mathrm{LR}}[n]. \tag{11}$$

Since for $n \leq 0, e_d[n] = 0$, and for $n > 0, e_t[n] = k\Delta d$

$$\begin{aligned} x[0] &= d_{\mathrm{LR1}} \\ x[1] &= d_{\mathrm{LR1}} + k\Delta d = d[n] \\ x[2] &= d_{\mathrm{LR1}} + 2k \cdot \Delta d \\ x[3] &= d_{\mathrm{LR1}} + 3k \cdot \Delta d \\ &\cdot \\ &\cdot \\ &\cdot \\ x[n] &= d_{\mathrm{LR1}} + n \cdot k \cdot \Delta d. \end{aligned} \tag{12}$$

It can be seen that for the first-order system $x[n]$ changes linearly, at the rate proportional to value k. This process continues until $x[n]$ reaches or exceeds the first successive quantization step of the core DPWM, $d_{\mathrm{LR1}} + \Delta d_{\mathrm{core}}$. At the time DPWM output changes, $e_d[n]$ becomes negative and $x[n]$ starts ramping down with the slope $k - 2^{N-Ncore}$. As shown in Fig. 6(a), the process is periodical and *DPWM output always changes between two adjacent values*.

A similar analysis can be performed for the second-order Σ-Δ DPWM. It shows that

$$x[n+1] = e_d[n] + 2 \cdot x[n-1] - x[n-2] \tag{13}$$

and that sequence $x[n]$ changes as follows:

$$\begin{aligned} x[0] &= d_{\mathrm{LR1}} \\ x[1] &= d_{\mathrm{LR1}} + k\Delta d = d[n] \\ x[2] &= d_{\mathrm{LR1}} + 3k \cdot \Delta d \\ x[3] &= d_{\mathrm{LR1}} + 5k \cdot \Delta d \\ x[4] &= d_{\mathrm{LR1}} + 8k \cdot \Delta d \\ &\cdot \\ &\cdot \\ &\cdot \\ x[n+1] &= d_{\mathrm{LR1}} + \left(2 + \frac{n(n+1)}{2}\right) k \\ &\quad \cdot \Delta d, \quad \text{for } n > 0. \end{aligned} \tag{14}$$

The rate of change described with the previous equation is much faster than that of the first-order Σ-Δ and, as shown in Fig. 6(b), in some instances the steps are larger than Δd_{core}. As a result, *the changes of the core DPWM are more frequent and larger in amplitude.* Consequently, higher frequency tones are produced and faster averaging process is achieved.

Even though the variations of the duty ratio are stronger, their effect on the switching converter output voltage is smaller, as shown in the previous experiments. This is because the largest portion of the tones energy is contained at frequencies significantly higher than the power stage corner frequency where a strong attenuation is possible.

It should be noted that in a second-order Σ-Δ modulator a tradeoff between the reduction of the core DPWM resolution and the amount of low-frequency tones introduced in the system exists as well, although significantly less severe then in the first-order case. The tradeoff is a complex function of the Σ-Δ modulator parameters and its operating point and its analysis is usually challenging [30]. To ensure that the effect of quantization noise is negligible, a help of widely available simulation tools is usually advisable [21].

In this case, to verify satisfactory operation of the system, a sweep analysis of output noise value for all possible inputs $d[n]$ can be performed. Consequently, the minimum allowable core DPWM resolution for a limited value of the output voltage noise can be found in a relatively simple manner.

D. Practical Implementation

To minimize size and power consumption, the second-order Σ-Δ DPWM of Fig. 4 is modified and realized as shown in Figs. 7(a) and (b) Instead of using 10-b signal $x[n]$, the Σ–Δ modulator processes the truncation error only. This structure is known as error-feedback [21], [30] and performs the same function as the above described second-order system utilizing much simpler digital hardware. In this case, only two adders are used, and $e_d[n]$ and $d_{\mathrm{LR}}[n]$ are just six least significant bits (LSBs) and four MSBs of $x[n]$, respectively. In addition, each delay block is realized with only six D flip-flops and the sizes of the adders are reduced accordingly. The $\times 2$ multiplication block is implemented as a simple 7-b logic shifter. The function of the limiter is to restrict $d_{\mathrm{LR}}[n]$ to positive values and prevent overflows.

The modulator is clocked at the switching frequency, by a signal created with the core DPWM. The 4-b core DPWM is based on the ring-oscillator architecture [13], [14], [22] consisting of sixteen digitally programmable delay cells, a 16:1 multiplexer, and an S–R latch. The programmable delay cells provide regulation of switching frequency through signal $f_{\mathrm{sw}}[n]$, which is either created externally or by a frequency matching block, which is described in the following subsection.

At this point it might be interesting to compare the two presented Σ-Δ architectures (first and second order) with a DPWM using programmable digital dither [11], [31]. Similarly to the first-order Σ-Δ, the dithering DPWM varies the duty ratio of a core-resolution DPWM by an LSB to improve the effective resolution. The dithering sequence, stored in a lookup table, is programmed such that for any given input it results in the minimum possible low-frequency ripple [31]. As a result, the overall ripple of the dithering DPWM is smaller than that of the first-order Σ-Δ DPWM, which does not always produce the optimum sequence. However, for several critical duty-ratio values, including the one described in the example of Section II-B, both methods produce the same low-frequency tones [31]. Hence, they have the same limitations regarding the selection of the resolution of the core DPWM. Since the second-order Σ-Δ DPWM

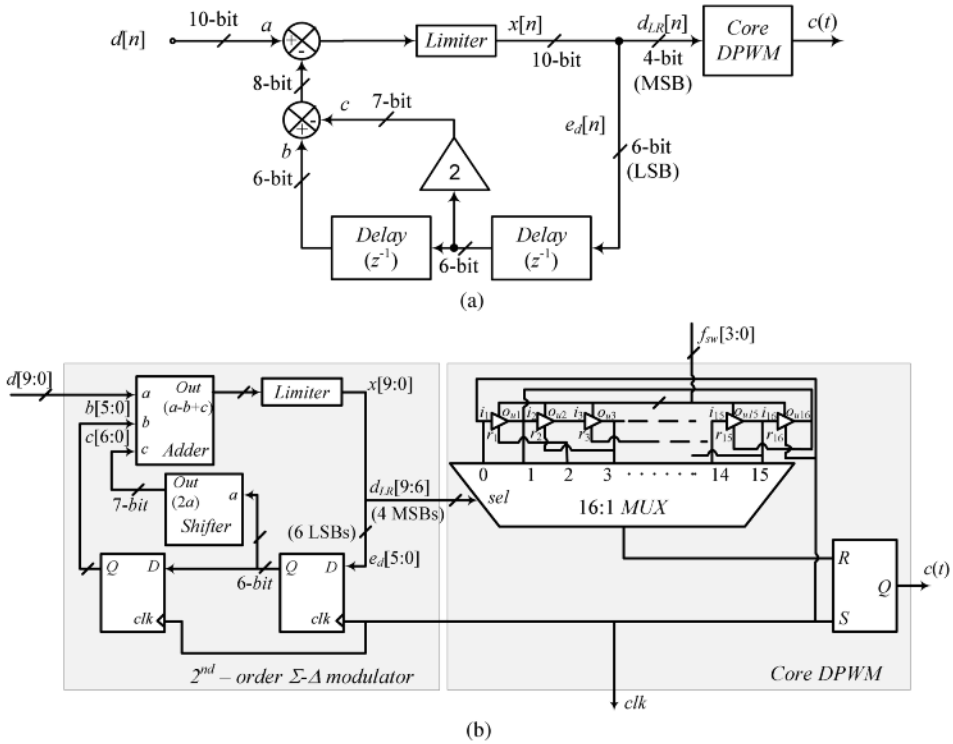


Fig. 7. Error-feedback second-order Σ-Δ DPWM: (a) functional block diagram and (b) practical implementation.

pushes all tones to higher frequencies a more power efficient implementation of the core DPWM is possible. The second-order Σ-Δ modulator also eliminates the need for a relatively large look-up table of $2^{2(N_{\mathrm{DPWM}}-N_{\mathrm{core}})-1}$ b [11], [31], used to store the optimal dithering sequences. This on-chip area saving comes at the expense of larger power consumption of the modulator part itself, caused by relatively large adders operating at the switching frequency. However, as shown in Section V, this consumption is practically negligible compared to the power taken by the core DPWM.

1) Digitally Programmable Delay Cell and Frequency Synchronization Block: Fig. 8(a) shows a delay cell that has a digitally programmable propagation time. It is based on a modification of current starved delay architecture [33], whose delay depends on the rate of discharge of C_{eq}, the equivalent capacitance seen at the node a. The discharging is performed by a set of ten transistors, Q_2 to Q_{11}. Five of them, Q_2 to Q_6, are acting as logic switchers and the others are mirroring/multiplying the bias current I_{bias}. The transistors Q_7 to Q_{11} are sized in a binary-weighted fashion (W/L, 2 W/L, 4 W/L, and 8 W/L) resulting in equivalent ratios of their mirrored currents and consequently in different discharge rates. The 4-b control input f_{sw} [3:0] switches transistors Q_2 to Q_6 to change the discharge current, i.e., delay, by varying the number of mirroring transistors operating in parallel. To minimize the size and power consumption of the DPWM, the same current biasing circuit is shared among all 16 cells.

The block diagram of Fig. 8(b) illustrates a new block that provides synchronization of the SMPS switching frequency with an external clock, which is often desirable to minimize interference in electronic devices. The system utilizes the idea of a replicating delay line, previously used in analog delay locked loops [34]. In this case, we show implementation that can be fully realized with digital hardware and is modified to operate with ring-oscillator based DPWMs.

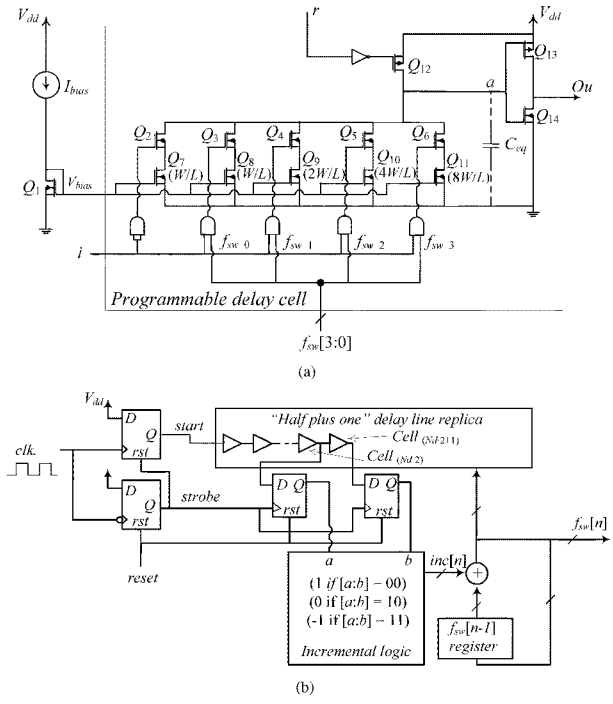


Fig. 8. Frequency regulation system: (a) digitally programmable current-starved delay cell and (b) frequency synchronization block.

The synchronization is achieved by comparing a half of the period of external clock signal, clk, with the propagation time through a *half plus one* replica of core DPWM's delay line,

having $N_d/2+1$ delay cells, where N_d is the number of delay elements of the core DPWM. Initially, at a rising edge of the clock *start* signal is created and passed through the replica, whose last two cells, i.e., $N_d/2$ and $N_d/2+1$, are connected to two edge triggered flip-flops. Then, at the immediately following negative edge of the clock, *strobe* signal is created and a "snapshot" of those two delay cells is taken by D flip-flops. The snapshot is then processed with the incremental logic block. Two logic zeroes show a slower propagation (i.e., longer switching period) and increase the value of frequency control register $f_{\rm sw}$ [3:0]. Similarly, two ones indicate a lower switching frequency and cause decrease of $f_{\rm sw}$ [3:0]. It is assumed that half periods of DPWM and external clock are approximately equal when the binary combination 10 occurs. In this case, an external clock with exact 50% duty ratio is required. For the case when a nonideal clock signal is applied the present circuit needs a minor modification. Then, the delay line can be replaced with a larger replica containing N_d+1 cells, and the start and the strobe signal need to be created with two successive rising or falling edges of the clock signal.

It should be noted that all-digital implementation of programmable frequency DPWM and synchronization blocks is also possible. It is more suitable when custom mixed-signal design of delay cells is not possible (FPGA implementation for instance) or when the controller current consumption measured in microamps is not crucial. In that case, the digitally programmable current starved delay cells can be replaced with a structure consisting of a multiplexer and digital logic gates acting as delay cells [8].

III. Dual-Mode Compensator

To minimize power consumption of the compensator and make it suitable for operation with the previously described Σ-Δ DPWM, we developed a dual-mode PID compensator architecture that can also be used with other DPWM topologies.

Previous analysis showed that in order to achieve high effective resolution of a Σ-Δ DPWM its input needs to be updated at the rate significantly lower than the switching frequency of the converter. This implies that a successful realization of the proposed structure requires a slow compensator that would change control value $d[n]$ slowly, and in that way eliminate possible noise problems. However, this solution compromises the dynamic performance of the switching converter and result in poor transient response.

The dual-mode architecture, shown in Fig. 9(a), consists of a mode-control logic block and dual-mode compensator, which is based on look-up tables (LUTs). This design utilizes the fact that high DPWM resolution is necessary in steady state only, while during transients it can be reduced to improve controller response. Depending on the value of output voltage error $e[n]$ (Fig. 1) *mode control logic* resolves whether the SMPS is in steady state or going through a transient and changes the mode of operation accordingly.

The mode change is performed through *mode* control signal. In steady state, the controller operates in *under-sampled mode*, where the frequency of PID compensator clock signal, $\rm clk_1$, is reduced and a new value of duty ratio control variable $d[n]$ is calculated and updated slowly using slow_mode set of look-up

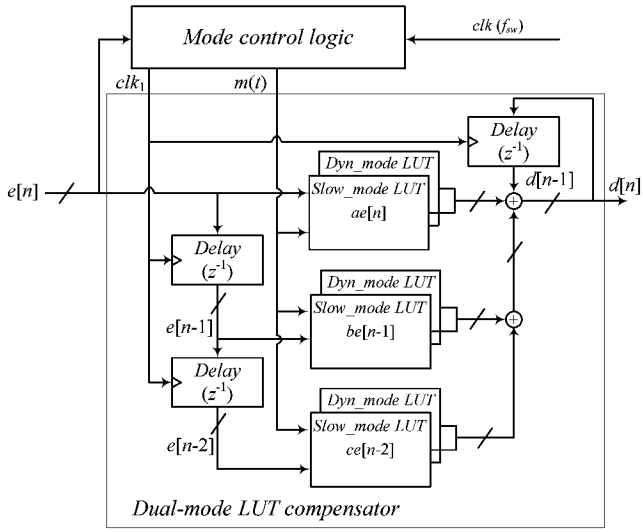


Fig. 9. Block diagram of dual-mode PID compensator.

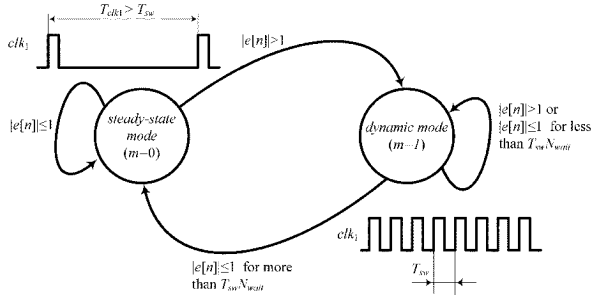


Fig. 10. State-transition diagram of mode control logic.

tables. This allows sufficiently long Σ-Δ averaging process, i.e., results in high effective DPWM resolution, and significantly reduced power consumption of the controller. During transients the clock is changed, $d[n]$ is updated once per switching cycle, and faster LUT based compensator (Dyn_mode PID of Fig. 9) is used to achieve fast transient response.

The LUT-based PID compensators employ discrete-time control laws that can be described with the following general equation:

$$d[n] = d[n-1] + ae[n] + be[n-1] + ce[n-2]. \qquad (15)$$

In both modes, the same adders and registers are used to calculate $d[n]$ and keep previous values of error and output variable, $e[n-1], e[n-2]$ and $d[n-1]$, respectively. The compensator coefficients a, b, and c, i.e., tables entries, are determined in accordance with the procedure described in [35].

A. Mode Control Logic

To eliminate potential stability problems related to dynamic switching between different control modes [36] *mode control logic* is developed. The operation of the *mode control logic* is described with the state diagram shown in Fig. 10. Initially, it is assumed that the controller is in steady state, characterized with low value of mode signal and low clocking frequency of the PID compensator. It remains in this state as long as output

voltage variations are small, i.e., $e[n] \leq 1$. Upon a strong disturbance the error increases and the controller switches to dynamic mode. The dynamic mode is maintained until a sufficiently long sequence $e[n] \leq 1$ values occur indicating that the converter is in equilibrium again.

It should be noted that a simple hysteretic logic [27] that immediately switches in static mode when the error becomes zero (or lower than certain number) often causes stability problems and, as such, is not an optimal solution for the dual-mode operation. During transients, even though converter is not in steady state instantaneous values of the output capacitor voltage can result in a short sequence of zero errors. In that case, if conventional hysteretic logic is used a fault steady-state is recognized and the controller prematurely switches in the slow control mode. Since the slow controller is not able to handle the transient, the error becomes large again and a cyclic switching between the modes occurs.

IV. Nonlinear Analog-to-Digital Converter

Windowed-based ADCs [13], [14], [37], [38] measuring the output voltage only around the reference voltage, i.e., zero error bin, are proven to be efficient solutions for low-power digital controllers both in terms of power consumption and required on-chip area for implementation. Architectures based on delay lines [15], [38] and ring oscillators [13], [37] are most common examples. In these ADCs the conversion is performed with voltage-controlled oscillators (VCOs) or through changes of propagation times of delay cells supplied by the measured voltage. The main drawback of these architectures is that the quantization step and conversion speed depend on the operating point defined with reference voltage $V_{\rm ref}$, resulting in variable gain and slower conversion times at low input voltages.

In low-power portable applications, besides having very low power consumption and short conversion time, the ADC is also required to operate with continuously decreasing input voltages. The supply voltages of modern digital circuits are reducing constantly following rapid advances in IC implementation technology. In order to eliminate the need for the redesign of digital controllers each time characteristics of the supplied devices change, it is desirable to have an ADC, whose operation is unaffected with the change of $V_{\rm ref}$.

To eliminate the problem of variable quantization steps self-strobe solution combining delay line, VCO, and digital calibration logic is shown in [38]. In this system, the digital logic effectively controls the size of quantization step but the problems of the variable conversion time and operation at lower supply voltage have not been addressed.

In the solution presented in [13], a pMOS differential pair eliminates the influence of operating point on the ADC operation. The pair produces two currents, whose difference is proportional to output voltage error, that are used to control frequencies of two ring oscillators clocking counters. A digital equivalent of the analog error is then created by comparing the counters values every switching cycle. It was shown that this ADC operates effectively in a switching converter operating at frequencies up to 1.5 MHz. The ADC consumes about 75 μA/MHz, most of it is taken by the counters and ring oscillators, which are significantly less power efficient than delay lines.

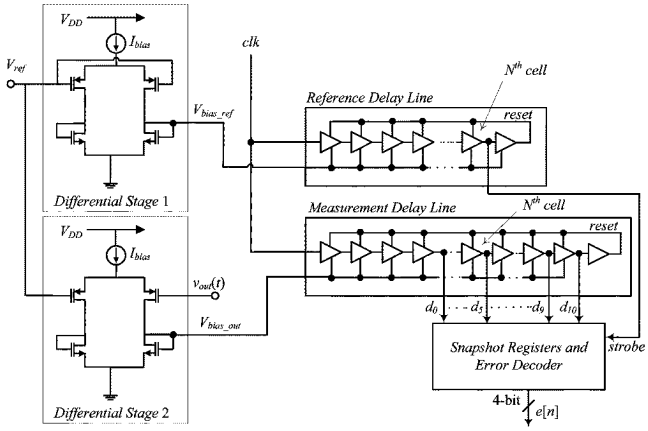


Fig. 11. Nonlinear ADC based on differential stage and delay line.

At switching frequencies exceeding 10 MHz, this consumption would have a significant effect on the overall efficiency of a low-power SMPS.

The ADC we introduce here combines advantages of previous designs to achieve significantly lower power consumption and characteristics unaffected by the changes of operating point. A block diagram of the ADC is shown in Fig. 11. Two input differential stages are used to provide bias voltages for reference and output voltage measurement delay lines containing different numbers of identical current-starved delay cells. The input voltage measurement line contains five more cells than the reference line. Similar to the solution presented in [38], the output voltage error is measured by comparing propagation times of clk signal through the delay lines. Both delay lines are triggered simultaneously, with the rising edge of clk signal initiating movement of two pulses through them. When the pulse propagating through the reference delay line reaches the Nth delay cell, a *strobe* signal is created and a snapshot of the measured delay line is taken. Then, based on the number of cells the clk signal has propagated through, the *error decoder* determines $e[n]$, the digital equivalent of the output voltage error, and sends it to PID compensator of Fig. 9.

Two identical differential stages, as connected in Fig. 11, allow operation with low input voltages and characteristics of ADC independent of $V_{\rm ref}$. It can be seen that $V_{\rm bias\_ref}$, the output of P-MOS differential stage DS_1 is unchanged for $V_{\rm ref}$ ranging from zero volts to maximum input value limited with $V_{\rm DD}$, threshold voltages of pMOS transistors, and current biasing circuit.

The voltage of the differential stage DS_2 regulating propagation through measurement delay line can be described as follows [39]:

$$\begin{aligned} V_{\rm bias\_out} &= V_{\rm bias\_ref} + K(V_{\rm ref} - v_{\rm out}(t)) \\ &= V_{\rm bias\_ref} - Ke_v(t) \end{aligned} \tag{16}$$

where $e_v\,(t)$ is the output voltage error and K is a constant that depends on $I_{\rm bias}$ and the sizing of the transistors in differential stages as well as on the construction of delay cells. This equation shows that the difference in propagation times through two delay lines only depends on the voltage difference and is not influenced by the changes of $V_{\rm ref}$.

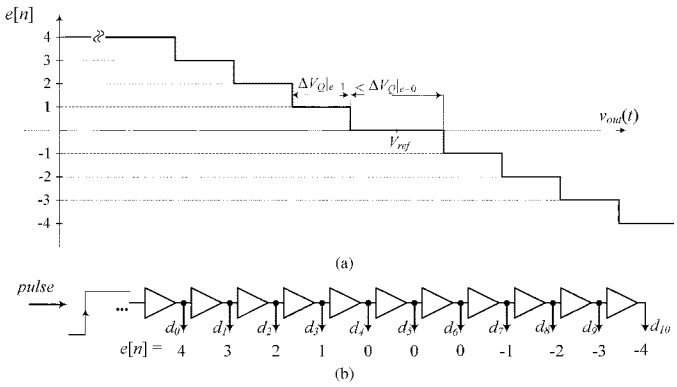


Fig. 12. Nonlinear quantization ADC steps: (a) input-to-output static characteristic and (b) practical implementation.

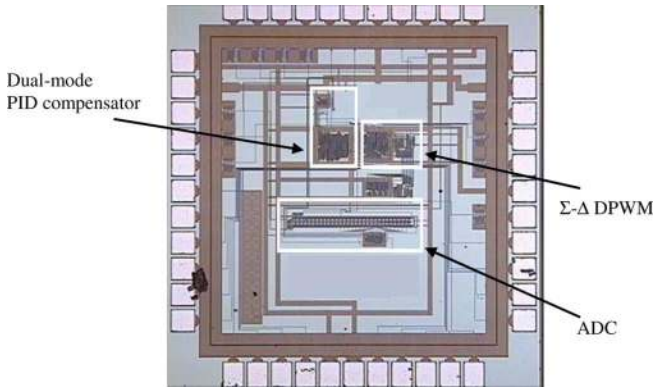


Fig. 13. Die photo of the fabricated ultra-high frequency digital controller IC.

TABLE II
CHIP PERFORMANCE SUMMARY

DPWM switching frequency	Programmable, 400 kHz to 18 MHz
DPWM effective resolution	10-bit
Σ-Δ DPWM chip area	0.028 mm^2
Core DPWM current consumption	43 μA/MHz
Σ-Δ Modulator current consumption	2 μA/MHz
PID compensator chip area	0.03 mm^2
PID compensator current consumption	2 μA/MHz
ADC conversion time	Programmable up to 50 ns
ADC quantization step	Adjustable, > 15 mV
ADC power consumption	8 μA/MHz
ADC chip area	0.108 mm^2

In this structure, both conversion speed and quantization steps depend on $I_{\rm bias}$ and the construction of delay cells. This means that more functions to this ADC such as dynamic variation of quantization steps, and variable conversion time can be added by replacing currently used conventional current-starved delay cells with digitally programmable ones shown in Fig. 8(a). In addition, to further reduce power consumption it would be possible to shut down the current bias circuit after the ADC conversion is completed and activate it again with the new rising edge of the clock signal.

A. Nonlinear Quantization

Another novelty of this design is that it utilizes nonlinear quantization steps to introduce variable gain and improve controller transient response without causing limit cycle oscillations. In digitally controlled SMPS, it is usually desirable to limit the minimum size of the ADC's input voltage quantization step resulting in zero error value, i.e., limit the width of zero error bin. If quantization step ΔV_Q is too small, higher DPWM resolution is required to eliminate possible limit cycle oscillations [11], [12]. On the other hand, outside the zero-error bin, larger steps result in lower sensitivity to output voltage variations and reduced loop gain caused by nonlinear quantization effects [12].

To improve controller performance, the input output characteristic of this ADC is shaped as shown in Fig. 12(a). The zero-error bin is larger than the other quantization steps corresponding to a significant difference between $V_{\rm ref}$ and the converter output voltage. As a result, the gain of ADC, defined as

$$K_{\rm ADC} = \frac{\Delta e[n]}{\Delta V_Q} \tag{16a}$$

is made to be larger for nonzero values and a nonlinear gain characteristic is created.

Fig. 12(b) describes how the nonlinear ADC characteristic is implemented. It shows output values of the error decoder for different snapshots of the measurement delay line taken at the end of conversion process. The nonlinearity is created by assigning zero error to three different snapshots of the measurement line. As shown in Fig. 12(b), it is assumed that $e[n]$ is zero if the pulse propagating through measurement line goes through the same number of cells as the one moving through the reference line, or if the difference in the number of cells signals have propagated through is not larger than one.

V. SIMULATIONS AND EXPERIMENTAL RESULTS

This new digital controller architecture is implemented on an application specific integrated circuit (ASIC) and fabricated in 0.18-μm CMOS process. The fabricated chip is then tested with a 3.3 V, 750-mW buck converter operating at switching frequency of 12 MHz. In addition, the results of HSPICE simulation of the same design with adjusted parameters for operation at switching frequency beyond 100 MHz are shown.

A. Chip Characteristics

Fig. 13 shows die photo of the fabricated chip prototype and Table II summarizes its main characteristics. It can be seen that the IC occupies very small silicon area and that the controller has low power consumption comparable to state-of-the-art analog solutions.

As mentioned in the previous section the power consumption of the ADC can be further reduced by operating bias circuit only during a portion of the switching interval. Simulations predict that, depending on conversion time, this modification can result in the reduction of ADC's power consumption to between $1/3$ and $1/5$ of its original value. Furthermore, the design of delay cells and biasing circuit of the DPWM can be optimized to achieve power consumption of 4 μA/MHz, as reported in [13], [40]. In that case, the total consumption in the range of 10 to 15 μA/MHz can be expected.

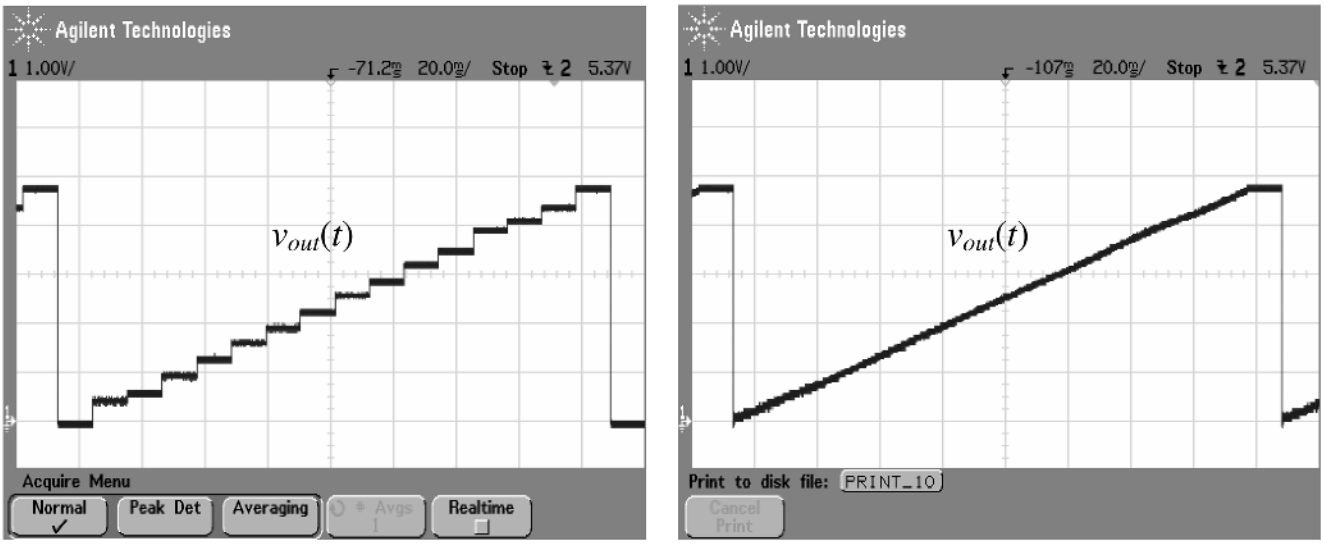


Fig. 14. Output of experimental switching converter for gradual change of duty ratio control input $d[n]$ from 0 to 1023. Left: without Σ-Δ modulator. Right: when the Σ-Δ modulator is active.

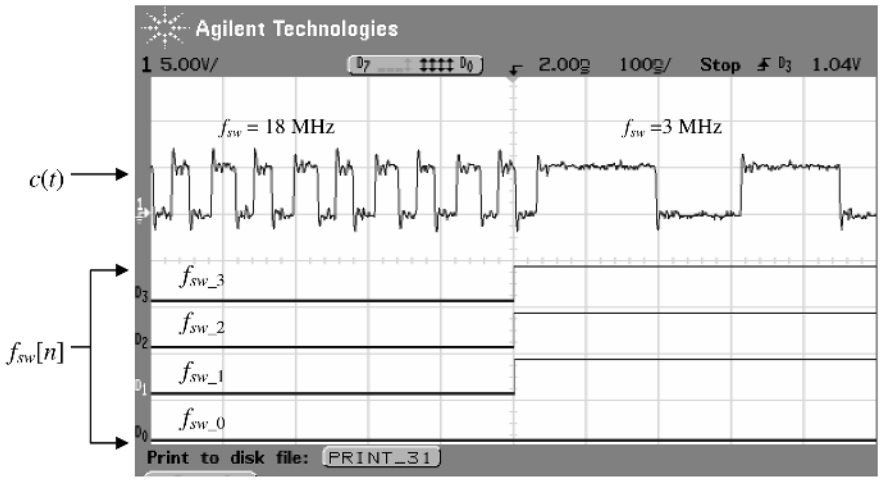


Fig. 15. Change of DPWM switching frequency through $f_{\rm sw}[n]$ variations, Ch.1: PWM control signal $c(t)$; D0 to D3: 4-b switching frequency control signal $f_{\rm sw}[n]$.

B. Verification of Open-Loop Operation

Here, the results of functional verification of Σ-Δ DPWM operation are given. Fig. 14 demonstrates the effect of Σ-Δ modulator on the effective DPWM resolution. It shows the output of an experimental switching converter for a sweep change of duty ratio caused by slow incremental change of 10-b control input d [n], from 0 to 1023. The results are shown for two modes of operation, when the Σ-Δ modulator is disabled and when it is active. It can be seen that, as described in Section II, the effective resolution of the core DPWM is significantly improved. In addition it can be seen that the modulator improves linearity of the DPWM. Different propagation times of core DPWM delay cells caused by process variation, parasitic capacitance of the chip layout, and different loading of delay cells used for clock generation cause nonuniform quantization steps of the core DPWM. Due to the operation of Σ-Δ, the variations of the delays are also averaged and their effect is minimized.

It should be noted that the uniformity of the quantization steps of the core DPWM can be improved by loading all of them equally, with additional buffer cells. However, this solution would result in an increase of the equivalent capacitance of current starved delay cells [Fig. 8(a)] and consequently in higher power consumption of the core DPWM.

Fig. 15 demonstrates operation of DPWM for the change of frequency regulation signal $f_{\rm sw}[n]$ [Fig. 8(b)] between two values. It can be seen that the frequency can be changed in a single switching cycle and that the DPWM can operate at 18 MHz. This shows that if programmable delay cells having higher resolution are used this IC could potentially operate as a combined digital pulse-frequency/pulsewidth modulator as well and, consequently, be used in quasi-resonant converter topologies.

C. Closed-Loop Operation

To verify closed-loop operation a 6 to 3.3 V, 750-mW, buck power stage was constructed and regulated by the controller IC as shown in Fig. 1. The switching frequency of the controller is intentionally reduced to 12.6 MHz to accommodate limitations

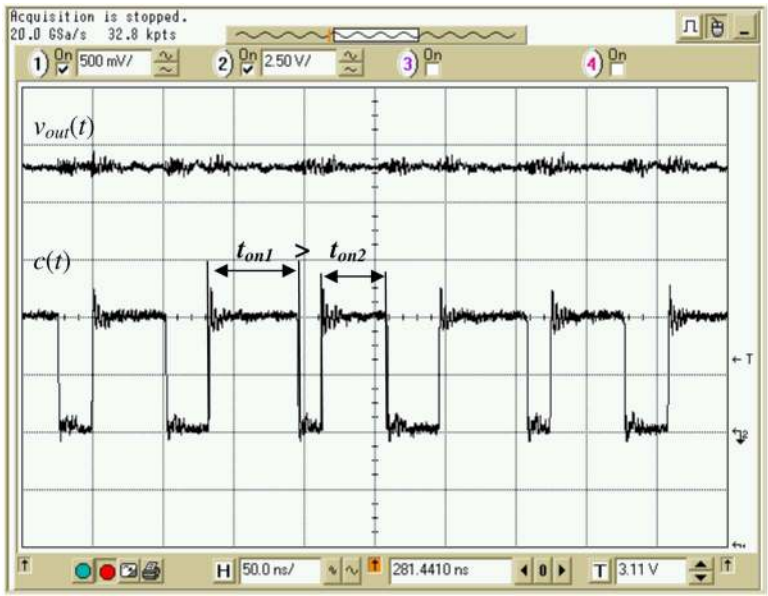


Fig. 16. Steady-state operation of digital controller at 12.6-MHz switching frequency, Ch.1: Regulated output voltage at 3.3 V (500 mV/div); Ch.2: PWM control signal $c(t)$ (2.5 V/div). Time scale is 50 ns/div.

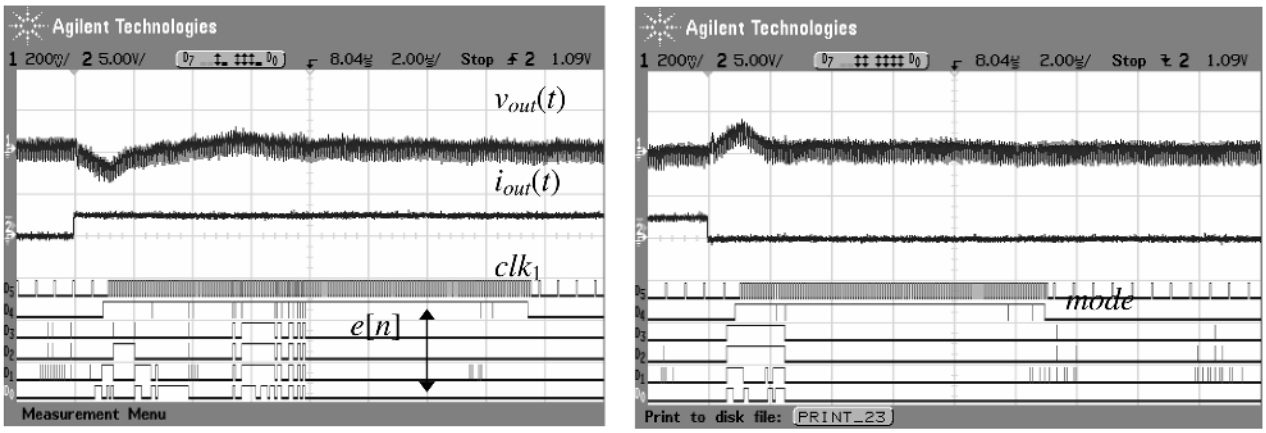


Fig. 17. Results of load transient experiment. Ch.1: Regulated output voltage at 3.3 V (ac-200 mV/div); Ch.2: Load current; D5: compensator clock signal clk1 (Fig. 9); D4: mode control signal; D0 to D3: 4-b binary error value $e[n]$.

of currently available power stage components (commercially available inductors, gate drivers, and power MOSFET-s).

Fig. 16 demonstrates steady state operation of the closed-loop system. The diagrams show that the controller provides a well-regulated output voltage without limit cycle oscillations or noise related problems even though the resolution of the core DPWM is only 4 b. The waveforms also demonstrate how the modulator changes duty ratio value, i.e., $t_{\rm on}$ time, through several successive switching cycles to achieve high effective DPWM resolution.

Fig. 17 shows results of a load transient response experiment for the output current change between 10 and 220 mA and demonstrates operation of the dual-mode PID controller described in Section III. Upon a load transient is recognized the controller switches to dynamic mode (frequency of $\rm clk_1$ shown in Fig. 9 is high). The controller remains in dynamic mode until the output voltage is stabilized, i.e., $e[n]$ is small over a large number of switching cycles. Then, it returns to *steady-state control mode*, where the frequency of $\rm clk_1$ decreases. The results verify that dual-mode operation results in a fast load transient response.

D. Simulation Results

The fabricated IC is optimized to operate at switching frequencies between 1.5 and 20 MHz. In order to show that the same structure can be used with upcoming power supplies operating at even higher switching frequencies, we slightly modified the actual IC design and simulated its operation at 150 MHz, using HSPICE. The switching frequency of Σ-Δ DPWM and the conversion speed of the ADC are increased through different sizing of current starved delay cells and adjustments of bias current of the circuits shown in Figs. 8(a) and 11, respectively.

The results of analog HSPICE simulation are shown in Figs. 18 and 19. Fig. 18 shows PWM waveforms of Σ-Δ

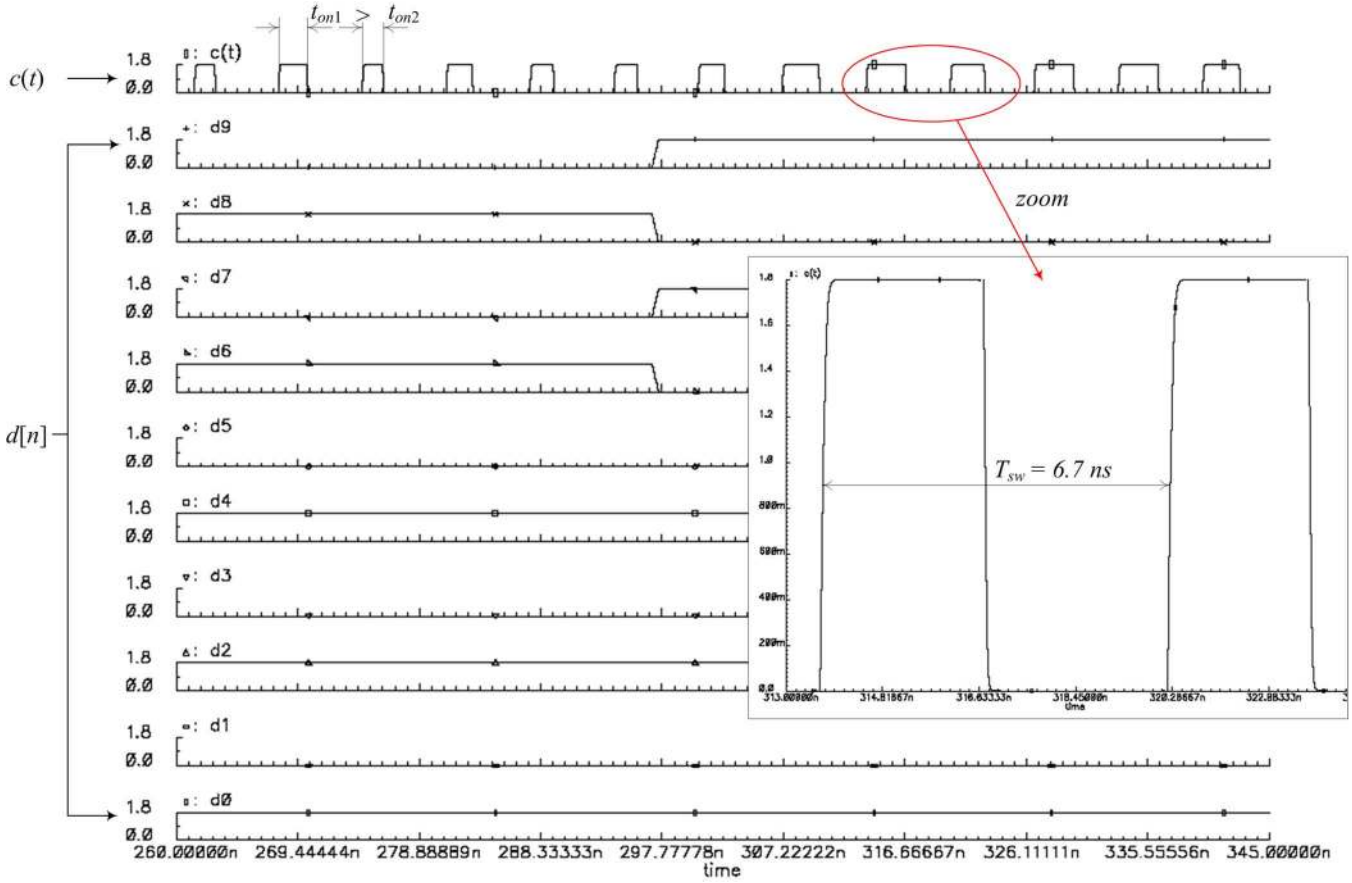


Fig. 18. Simulation results for Σ-Δ DPWM operating at 150 MHz.

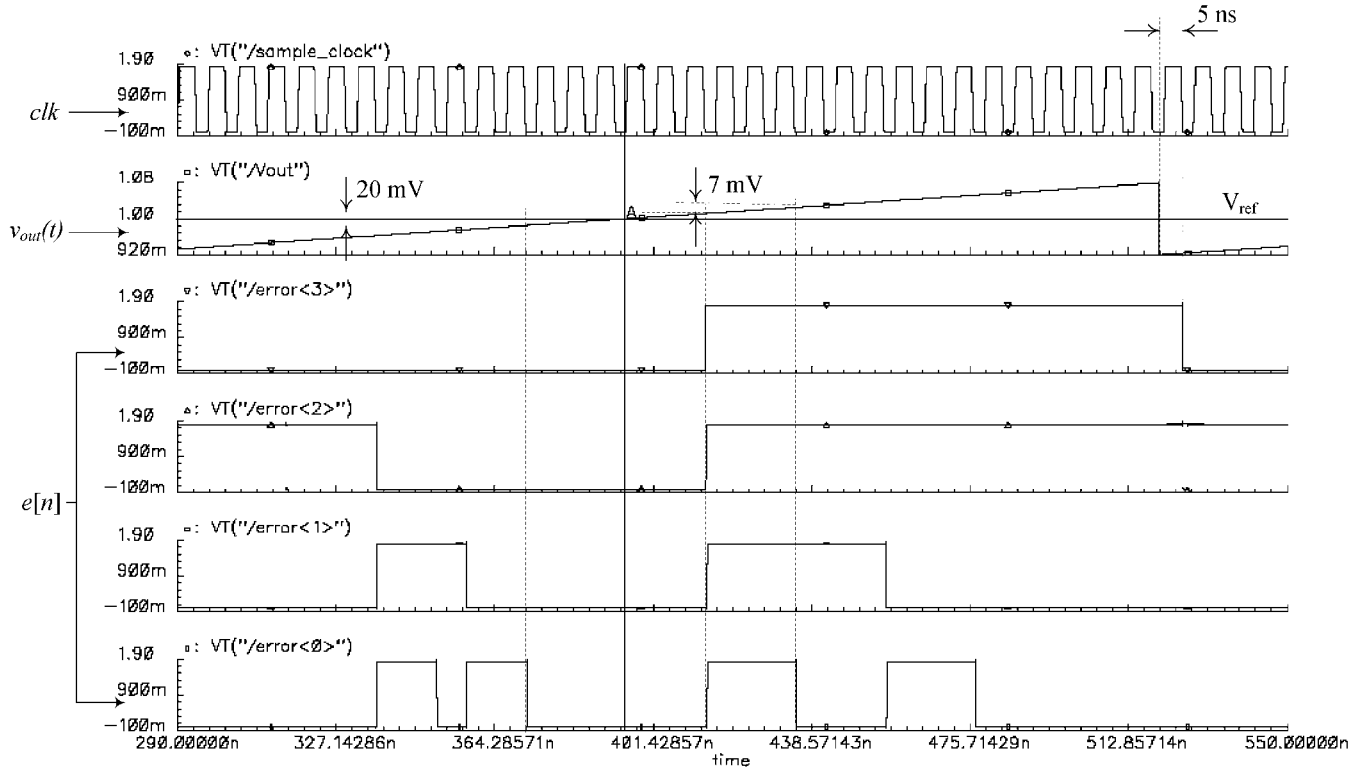


Fig. 19. Simulation results for ADC operating 150-MHz sampling rate.

DPWM for a change of 10-b duty ratio control value $d[n]$ between 341 and 661, binary. The simulation shows PWM signal $c(t)$ at 150 MHz and demonstrate operation of Σ-Δ modulator changing $t_{\rm on}$ time over successive switching cycles. At this

frequency, the effective 10-b DPWM resolution corresponds to the equivalent time step of less than 7 ps. Due to limited speed, this time-step cannot be achieved with ring-oscillator or counter based DPWM architectures using most common technologies for IC implementation. For example, typical propagation time of a 0.18-μm CMOS digital logic cell is between 20 and 50 ps limiting maximum frequency/resolution of the other architectures. The estimated current consumption is 700 μA, significantly smaller than what Table II predicts. This is because delay cells with smaller equivalent capacitance [Fig. 8(a)] are used to increase the switching frequency. The reduced capacitance requires less energy to be charged and causes shorter lasting shoot-through current through the output CMOS stage of delay cells, both of which significantly reduce overall power consumption.

The simulation results of Fig. 19 demonstrate operation of the nonlinear ADC when the clock signal frequency, provided by the DPWM, is 150 MHz. The waveforms show how the ramping change of switching converter output voltage, $v_{\rm out}(t)$, around 1 V reference influences ADC's output, i.e., error $e[n]$. It can be seen that $e[n]$ also ramps from the binary value -4 to $+4$, for 80-mV effective change of the converter input voltage. Nonuniform quantization steps described in the previous section can also be observed. The zero error bin of this ADC is around 20 mV, approximately three times larger than the step corresponding to $e[n] = -1$. Simulations also verify fast analog-to-digital conversion. It can be seen that he ADC needs only 5 ns to react to an abrupt voltage change and convert analog signal into its digital equivalent. The current consumption is about 950 μA, because of the same reasons mentioned in the previous case, it is smaller than the value given in Table II.

These results verify that proposed architecture can provide an effective digital control solution for the fastest switching power converters today, as well as for upcoming systems expected to operate at frequencies beyond 100 MHz.

VI. Conclusion

A digital PWM controller IC for low-power dc–dc switching converters capable of operating at switching frequencies exceeding 10 MHz is presented. To achieve the high frequency of operation, low power consumption and improved load transient response, the controller utilizes three novel architectures of basic functional blocks, second-order multibit Σ-Δ DPWM, dual-mode PID compensator, and nonlinear ADC. It is shown how the second-order Σ-Δ modulator eliminates tone related problems occurring in first-order Σ-Δ DPWM architectures and consequently allows a significant increase of switching frequency and effective DPWM resolution. The dual-mode PID compensator operating at a sampling rate lower than switching frequency in steady state, and at the switching rate during transients, is developed to minimize overall power consumption without sacrificing transient response. The ADC combining dual differential input stage, delay lines, and nonlinear error logic is introduced as well. It allows operation with input voltages as low as zero volts and has quantization steps and conversion time independent of the operating point. The nonlinear error logic additionally improves dynamic response by creating nonuniform quantization steps that increase gain of the ADC for nonzero output voltage errors.

The new controller architecture is implemented on a 0.18 μm CMOS integrated circuit and operation of the Σ-Δ DPWM at programmable constant switching frequencies up to 16 MHz is demonstrated. The fabricated IC exhibits low current consumption of 55 μA/MHz. Operation in closed loop with an experimental 12.4 MHz, 6 to 3.3 V, 750-mW buck converter is demonstrated and good transient response performance is verified as well. Furthermore, the same design is modified to operate at higher switching frequencies and tested through simulations. It is shown that this digital architecture offers potential solution for controlling upcoming low-power switching converters that are likely to operate at switching frequencies beyond 100 MHz.

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