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MULTICHANNEL ANALOG TO DIGITAL CONVERTER AND READOUT SYSTEM FOR THE TIME PROJECTION CHAMBER

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Abstract

The Time Projection Chamber (TPC) project involves the characterization of signals arriving at approximately 20,000 separate detector wires and pad electrodes. The characterization requires measurement of the signal amplitudes in 100 ns time slices over a total time of 20 μs (the total chamber drift time). Charge Coupled Devices (CCD's) are used to store an image of the 20 μs span of signals and the image is "played back" at a low rate (50 μs time slices, i.e., a time expansion of 500:1). Digitization of the 20,000 parallel signals at the output of the CCD's must therefore be accomplished in 50 μs and readout of digital data into the computer system must also be accomplished in this time. Many zeros occur in the data, a fact which reduces the data handling demands on the readout system, but does not reduce the stringent requirements on the digitizer. Therefore, the requirements on the digitizer are highlighted by the need for low cost, low power consumption and by the need to perform 9-bit digitizing in less than 50 μs. Furthermore, a double buffering scheme must be used to permit interleaving digitizing and digital readout cycles.

We describe our implementation of this concept and some possible applications for other experiments which require many Analog to Digital Converter (ADC) channels.

Introduction

The central element of the PEP-4 detector at the PEP storage ring at Stanford, California, is the TPC. It is a large volume drift chamber, a cylinder of 2 m diameter and 2 m long, which provides intrinsically three dimensional spatial data. The chamber is shown schematically in Fig. 1. It is in a 1.5 tesla solinoidal magnetic field, and is filled with a mixture of 80% argon and 20% methane at a pressure of 10 atmospheres. A voltage of approximately 150 kV is applied to the center plane to produce an electric field which drifts the electrons produced by particle tracks in the chamber to the position sensitive proportional-wire detectors at the two end caps. Each end cap is equipped with six sectors of position sensing detectors--wires at positive voltage, which serve as proportional counters to amplify the charge reaching the wires by a factor of about 1000. The wire signals give information on the radial distance (r) of a track from the centerline. There are 192 of these "dE/dx-wires" per sector. In addition there are 12 wires distributed over the sector, which give the azimuthal angle (ϕ) of the tracks.

This angle information derived from a row of small (7 cm x 7 mm) pads placed under these wires, on which the avalanche on the wire induces signals. These signals can be used to determine the centroid of the avalanche. The coordinate along the beam axis (Z) is derived from the time of arrival of the charge from the tracks following a start signal derived from the PEP beam signals.

The signal amplitudes on the dE/dx wire determine the energy-loss pattern along the track. The magnetic field serves primarily to determine the momentum of the particle, by measurement of the curvature of the tracks, but it also reduces the transverse spreading of electrons during the drift process. The summation of all these data allows identification of the many particles produced in very high-energy interactions and determines their energies and momenta. (For a detailed description the reader is referred to Ref. 1.)

Simply stated, TPC required a system capable of providing 20 μs of data sampled on the basis of 100 ns time intervals, the input signals coming from 16384 sources. This translates to a total of three million 9-bit words of possible information. The signals from the wires feed low-noise-charge-sensitive preamplifiers, then go to shaping amplifiers, where the pulses are amplified and shaped to optimize signal-to-noise ratios. The resulting signals are then sampled and stored in CCD's which are normally being clocked at 10 MHz.[2] Operating in this mode, the CCD's contain a "flash picture" of the past 20 μs of signals split into 100 ns time segments. When an event is detected by suitable trigger electronics, the CCD clock rate is slowed down, and the amplitude information now residing in the CCD's is shifted to their output at a 20 kHz rate. Digitization of signals and transfer of the digitized signals to the computer processing system must therefore be accomplished in less than 50 μs (i.e., one CCD slow clock cycle). This paper describes the A-D-convertor design used in this application. It also discusses the method employed to readout only the interesting information which is estimated to be about 10,000 words per event out of the three million possible words. Fortunately, this drastically reduces the requirements on the readout and processing system.

System Considerations

The original TPC proposal described the use of 128 fast ADC's (1 μs digitizing time) assigned these dynamically via priority encoders to channels containing valid (i.e., non-zero) information. This concept required a discriminator and a D-A-converter for each channel. To avoid saturating a particular set of multiplexed channels, it would be necessary to scramble channel to address relationships, so that signals in physically adjacent channels would go to different multiplexer-ADC combinations. This would have required an additional "unscrambling" step in the readout system and therefore an additional set of data buffers. This complexity resulted in the study of alternative schemes.

Since the outputs from the CCD's are constant voltage levels for 50 μs, an obvious way to digitize their values is to use Wilkinson rundown ADC's. This is very similar to the Large Scale Digitizer (LSD) concept, which has been used successfully at LBL [3] and elsewhere. Since the ramp generator and the associated logic can be shared between many channels,

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each ADC channel consists essentially only of one comparator and one register. The simplicity of this approach--the parts count is similar to the comparator +DAC part of the multiplexer scheme--makes it feasible to supply one ADC per signal channel and to digitize all signals from the CCD's. Detection of valid information (i.e., amplitude > threshold) then consists of comparing two digital numbers, one from the ADC register and the other from a preset threshold register. Valid information is then placed in an output buffer, which can be readout, while the next digitization takes place.

The resolution requirements (9 bit) for the ADC are dictated by the necessity for particle identification and track-center finding.

Configuration

We decided to put 16 ADC channels on one board, and put 16 ADC boards and one control board into a single rack-mounted bin. The control board contains the ramp generator, the clock drivers, and also the line drivers and receivers which receive the ADC data from the ADC boards and provide the connection to the computer. Also, threshold information for the individual ADC channel is distributed from the computer to the ADC boards via the control board. The methods used to distribute the ramp and the clock pulses have been discussed in earlier papers.[1,2]

Since this version of the LSD concept relies heavily on registers, cost effectiveness dictates the use of low-cost registers. Since the lowest cost per bit is offered by Random Access Memory (RAM) chips, the first version of the design (shown in Fig. 2) was based on their use.

The voltage level from the CCD is compared to a 41 μs long linear ramp, spanning the full signal amplitude range. A change of state in the comparator output is synchronized to the clock, and shaped to one clock pulse width. In this clock pulse, a bit is written in the data line of the particular channel of the "hit-list" RAM (16 word x 16 bit) and simultaneously the state of the clock counter is written into a "pulse-height" RAM (16 word x 12 bit, only 9 bits are used here). After this operation a 4-bit event counter is incremented, whose output generates the address for these RAM's.

After all channels have fired, the hit list RAM contains a sequential list of hit patterns (note: more than one channel can register the same amplitude) and the pulse-height RAM contains the associated pulse-height numbers. The information in the RAM's is not ordered in channel number sequence, but rather in an amplitude sequence. For readout the data must be reordered according to channel number. This done in the 9 μs period after the end of the ramp.

The reordering is done by looking with a maskable priority encoder at the outputs of the bit list RAM to derive the channel number of the fired channels. This channel number is then used to address a RAM which contains the threshold information. If the pulse height is larger than the threshold, it is written into the output RAM, and the line corresponding to the channel number fired is masked. Then either the next channel is checked, or if there are no more unmasked bits at the particular pulse height the event counter is decremented, the mask is reset, and the procedure continued until all events have been processed. The output RAM then contains only valid information, which can be readout during the next 41 μs digitization cycle. In this scheme the same number of integrated circuits is used for resolutions between 9 and 12 bits, the difference being only the number of outputs used in the pulse height, threshold, and output RAM's. Also, this circuit can handle multiple hits in one signal channel, which can happen, e.g., in tice digitizers, as long as they are separated by one or more clock pulses.

The disadvantage of the method is the complexity associated with the reordering, since the data are initially ordered according to amplitude. For readout purposes however an ordering according to channel number is needed. This could be done either by using another priority encoder to derive the location of valid data in the output RAM or by another reordering step. Both possibilities increase the number of the integrated circuits needed. Another problem is, that in order to meet the clock speed requirements (12 MHz), Schottky RAM's would have to be used, with the associated higher power dissipation.

Therefore in our final design, we have chosen to use 8-bit low power Schottky register, IC's, which have become available recently, and to use one additional flip flop per ADC channel to achieve the 9-bit resolution needed. The circuit is given in Figs. 3 and 4. Again as an input comparator changes state, this change is synchronized to the clock, and the current state of the clock pulse counter is written into a register consisting of an 8-bit tri-state-output register and an additional flip flop. At the end of the ramp, all channels, which have not changed are forced to change, so that "overflows" appear at amplitude channel 511.

Here no reordering is necessary, the control logic steps through the contents of the ADC register in a sequence of descending channel number, compares them with the appropriate threshold, and writes them in to the output RAM, if they were > threshold. If there was a valid event, it increments a valid event counter. This compression process occurs on all ADC boards in parallel, so that the ordered and compressed data is available after 16 read/compare/write cycles. Data in the output RAM's can then be read out in an already ordered fashion by the control board. The control board sequences through all ADC boards in its bin, skipping the ones which have no valid data (i.e., when the valid event counter is zero). A fast bin-skip feature is also provided to permit skipping a bin in one readout cycle, if it contains no valid data.

The threshold RAM's on the ADC board must be loaded from the computer. This can be done by digitizing the input levels with no signals present, and then by writing a number greater than this measured "zero level" into the threshold RAM's. The information from a particular channel can be suppressed by setting bit 9 in the corresponding threshold RAM, this prevents the transfer from the ADC register to the output RAM.

The advantage of the register version is the simplicity of the data reduction logic, since all operations can be done by directly addressing a particular channel, where, in the RAM version, priority encoders must be used. However, the resolution of the "register" ADC is essentially limited to 9 bits, because more bits would require more IC packages than the "RAM" ADC with a resolution of 12 bits.

In addition, the register implementation cannot tolerate multiple hits in one channel, such as might be required in time digitizers.

We use a digitizer clock frequency of 12.5 MHz, which gives a maximum digitizing time of 41 μs for 9 bits. Since the CCD slow clock rate is 10 kHz (i.e., 50 μs/step) 9 μs remain to reduce and reorder the data. During the first 40 μs of the next CCD slow clock cycle, valid data from the previous clock cycle are presented to the readout bus. Since only valid data is present, the requirements on the readout system are minimized.

Conclusion

We have designed a low-cost, multichannel ADC and readout system, which meets all the requirements imposed by the TPC detector. All signals in every channel are digitized, thereby avoiding the difficulties associated with the multiplexing of many analog signal into one common ADC. Since the amplitude information is digitized by the same device, regardless of its amplitude, there is only one calibration necessary for each channel. The digital information is available after a reasonably short time (41 μs), and all further data processing can be done with digital numbers. This allows elimination of invalid information, i.e., zeros, very early in the signal processing, and therefore reduces the demands on the readout system. It should be possible then, to do "real time" data processing with microprocessors on the stream of reduced data.

If faster integrated circuits (ike ECL) are used the number of bits can be increased, or the digitizing time can be shortened.

This class of ADC and readout system is well matched to the modern generation of detectors, where many signal channel have to be inspected in a short time, but only a few produce valid information.

References

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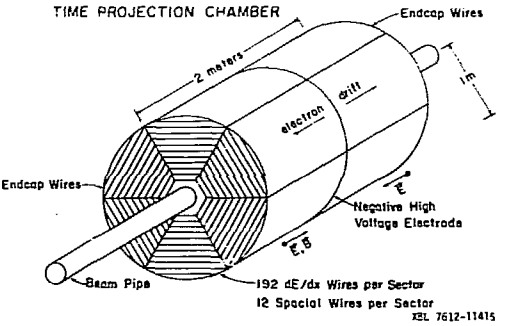

Fig. 1. Schematic picture of the Time Projection Chamber. Charged particles produced ionization in the high pressure gas of the TPC. The ionization electrons drift toward the end-caps under the influence of the axial magnetic and electric fields. Sense wires then multiply this charge and the detector electronics are used to measure the charge and its time of arrival.

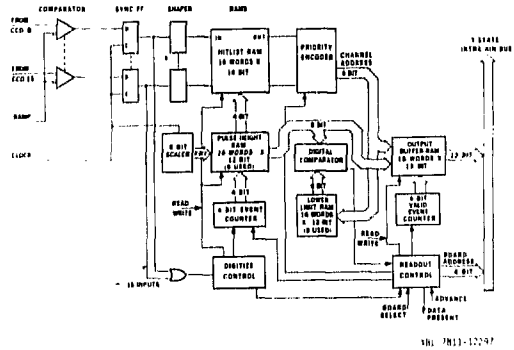

Fig. 2. Partial schematic of the first version of the digitizer. The levels from the CCS's are compared to a common ramp. The crossing time of the ramp and the level is synchronized to the common clock, and the digitize control stores, at the appropriate pulse height, the hit list RAM. After the end of the ramp the readout control compares the information from the different channels to the corresponding lower level, and writes it into the output buffer RAM. The further readout is similar to Fig. 4.

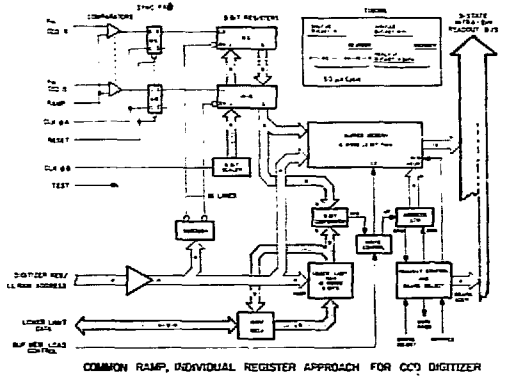

Fig. 3. Partial schematic of the register version of the digitizer. The crossing of the common ramp with with levels from the CCD's are synchronized to the clock, and the pulse height number is written into the registers. After the end of the ramp the readout control sequences through all 1C registers, and writes their content into the output buffer memory. This buffer is then read out under the control board of Fig. 4.

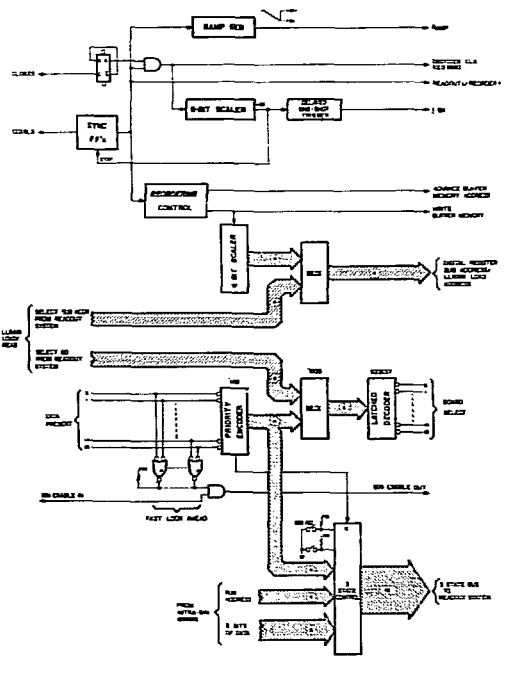

Fig. 4. Partial schematic of the control board of the second version of the digitizer. This board generates the common ramp, common clock and the pulses which control the reordering and read out. The 'data present' lines from the digitizer board are used to select only the boards which have non-zero data for readout.