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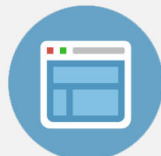
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Multidomain ferroelectricity as a limiting factor for voltage amplification in ferroelectric field-effect transistors

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We revise the possibility of having an amplified surface potential in ferroelectric field-effect transistors pointed out by [S. Salahuddin and S. Datta, *Nano Lett.* **8**, 405 (2008)]. We show that the negative-capacitance regime that allows for such amplification is actually bounded by the appearance of multidomain ferroelectricity. This imposes a severe limit to the maximum step-up of the surface potential obtainable in the device. We indicate new device design rules taking into account this scenario. © 2010 American Institute of Physics. [doi:10.1063/1.3494533]

The operation of field-effect transistors (FETs) generates a heat whose dissipation imposes severe restrictions to the miniaturization of integrated circuits. The lowering of the FET operating voltage is therefore highly desirable, which has to be accompanied with a reduction in the threshold voltage to maintain performances. This, however, implies the increase in the stand-by power since the inverse of the so-called subthreshold slope appears limited to 60 mV/dec at room temperature. At present, this is considered as an important roadblock for the transistor scaling down.¹ Recently Salahuddin and Datta² have suggested that the 60 mV/dec limit can be overcome in ferroelectric FETs as the sketched in Fig. 1. These FETs has a long history as candidates for nondestructive readout memory elements.³ The idea of Salahuddin and Datta is to exploit a negative capacitance regime of the ferroelectric in which the surface potential of the semiconductor V_s is up-converted and therefore the so-called body factor of the transistor $m \equiv (\partial V_s / \partial V_g)^{-1}$, where V_g is the gate potential, becomes smaller than one.

The physics behind this negative capacitance regime is associated to depolarizing field effects, i.e., the electric field that accompanies the polarization of the (finite-size) ferroelectric. As a result of this field, there is a shift in ferroelectric transition point and the ferroelectric can operate in its (otherwise unstable) paraelectric state. What is more, in such a state, the voltage drop ΔV through the ferroelectric decreases by increasing the gate voltage. This yields the desired amplification, since the changes in the surface potential V_s are then larger than the ones in the gate voltage ($V_g = \Delta V + V_s$). This possibility is explained in Fig. 2. Here we plot the load line $Q = C_s V_s = C_s (V_g - \Delta V)$, where Q and C_s are the charge and the semiconductor capacitance, respectively, and the $Q(\Delta V)$ characteristic of the ferroelectric. The slope of this later is always positive if the ferroelectric is well inside its paraelectric phase [Fig. 2(a)] and therefore the intersection between this function and the load line shifts toward higher voltages if the gate voltage is increased. The ferroelectric then behaves as the conventional oxide in the FET. However, when the ferroelectric $Q(\Delta V)$ characteristic acquires its S-shaped form, its slope is negative for $\Delta V = 0$

[Figs. 2(b) and 2(c)]. This happens below the nominal transition temperature of the ferroelectric (see below). If such a slope is more negative than $-C_s$ [Fig. 2(b)], then the intersection with the load line shifts toward lower voltages as the gate voltage increases. This means that the surface potential is enhanced as we have explained before, which can associated with a negative-capacitance behavior of the ferroelectric. If the ferroelectric $Q(\Delta V)$ characteristic gets sufficiently flat for low voltages then there appears three points of intersection with the load line [Fig. 2(c)], from which only the marked with dots correspond to stable states for the ferroelectric (now in its ferroelectric state). The voltage amplification holds until these points shift again toward higher values if the gate voltage is increased as shown in Fig. 2(c). This eventually translates into hysteresis loops for gate voltages varying cyclically from positive to negative.

According to these reasonings, the maximum amplification of the gate potential is expected to be limited by the eventual transition into the ferroelectric state. Salahuddin and Datta have tacitly assumed that this transition implies the single-domain state in which the spontaneous polarization is uniform through the ferroelectric. The actual situation, however, can be far more subtle. As a result of the depolarizing field the ferroelectric instability is generally equivalent to the appearance of multidomain ferroelectricity in which the polarization varies in space, with transition temperature shifts rather different from the assumed by Salahuddin and Datta.⁴ The aim of this paper is to show that the negative capacitance regime then gets saturated, which puts severe limits to the maximum amplification of the gate voltage that can be obtained in ferroelectric FETs.

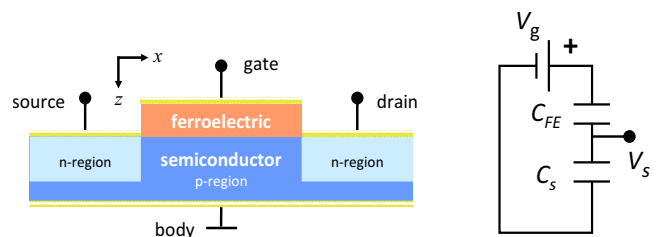


FIG. 1. (Color online) Schematic cross section of a ferroelectric FET (left) and equivalent circuit for the metal/ferroelectric/semiconductor stack (right).

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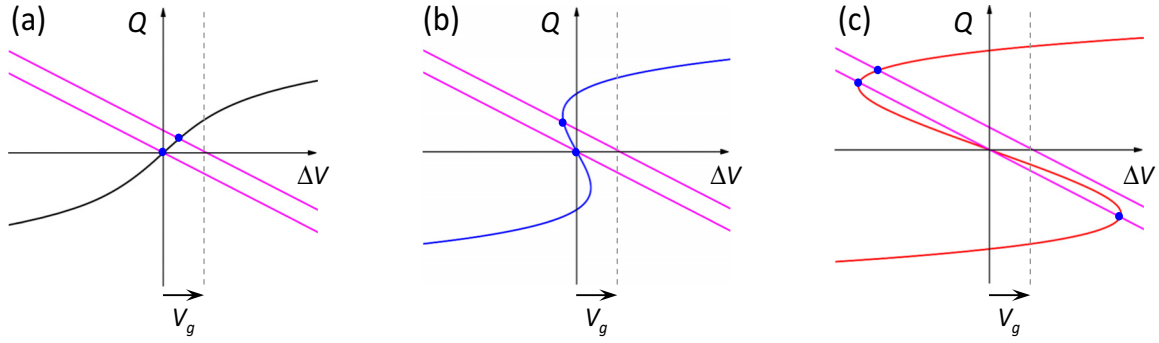


FIG. 2. (Color online) Sequence of possible states in the ferroelectric FET and geometrical determination of the bias point: [(a) and (b)] paraelectric states, and (c) hysteretic ferroelectric state. In (b) the negative capacitance regime with the step-up conversion of the surface potential is achieved.

To obtain the response of the FET to the applied voltage we follow the Landau-type approach described in Ref. 4. On one hand, the behavior of the ferroelectric is described by the equations

$$aP + bP^3 - c\nabla^2 P = -\partial_z V, \quad (1a)$$

$$[\varepsilon_{\parallel}(\partial_x^2 + \partial_y^2) + \varepsilon_0 \partial_z^2]V - \partial_z P = 0. \quad (1b)$$

Here P is the distribution of polarization along the ferroelectric z -axis and V the electrostatic potential in the ferroelectric. Equation (1a), which can be derived from a Ginzburg–Landau–Devonshire free energy, represents the constitutive equation for the ferroelectric whose electrostatics, as follows from Maxwell’s equations, is eventually determined by Eq. (1b). The instability that gives rise to ferroelectricity is described by the vanishing of the coefficient $a = a'(T - T_c^0)$ as usual, where T_c^0 is the nominal transition temperature (in the absence of depolarizing field) while the rest of coefficients are assumed to be positive constants. We thus assume a second-order (continuous) phase transition, which *a priori* is the most favorable scenario for the amplification of the FET gate voltage. On the other hand, the semiconductor is assumed to be undoped (or lightly doped) operating within its subthreshold regime as in Ref. 2. Thus, its mobile carrier density can be neglected and we simply have the equation $\nabla^2 V_s = 0$ for the electrostatic potential in the semiconductor. At the ferroelectric–semiconductor interface these quantities have to satisfy the electrostatic matching conditions $V = V_s$ and $\varepsilon_0 \partial_z V - P = \varepsilon_s \partial_z V_s$, where ε_s is the dielectric constant of the semiconductor.⁵ In addition, we have the boundary conditions $V = V_g$ at the gate and $V_s = 0$ in the semiconductor beyond its depletion layer (see Fig. 1). V_g is assumed to be below the FET threshold voltage in the following.

As long as the ferroelectric stays in its paraelectric phase the body factor of the FET is given by

$$m = 1 + \frac{\varepsilon_s}{1 + \varepsilon_0 a} \frac{l}{w} a. \quad (2)$$

Here l and w represent the thickness of the ferroelectric and the width of the semiconductor depletion layer, respectively. Noting that $\varepsilon_0 |a| \ll 1$ in the vicinity of the ferroelectric instability one obtains $m \sim 1 + \varepsilon_s a l / w = 1 + C_s / C_{FE}$, where $C_s = \varepsilon_s / w$ and $C_{FE} = 1 / (a l)$, which is the result reported by Salahuddin and Datta.² The desired up-conversion of the surface potential is obtained if the body factor is $m < 1$. This is possible if the bare polarization stiffness a gets negative and hence the ferroelectric can act as a negative capacitance

($C_{FE} < 0$). If depolarizing fields were totally screened, that would mean the instability of the paraelectric phase with respect to the spontaneous polarization of the system. This polarization, however, is accompanied with some depolarizing field in the FET, which produces an increase in the polarization stiffness. In consequence, the ferroelectric can remain in its paraelectric phase even if the bare stiffness is $a < 0$. In fact, the ferroelectric can be proven to be stable with respect to uniform distributions of polarization up to the point $a_* = -1 / (\varepsilon_0 + \varepsilon_s l / w)$ where the expression (2) for the body factor would give zero. This point, however, generally does not correspond to the transition point in the ferroelectric FET as we show in the following.

The actual phase transition point is determined by the point at which the Eqs. (1a) and (1b) have their first non-trivial solution ($P \neq 0$) for $V_g = 0$. This can be found by following the general procedure outlined in Ref. 4. For the FET geometry and the typical values for the depletion width of lightly doped semiconductors ($w \sim 0.1 - 1 \mu\text{m}$), such a solution corresponds to a polarization wave $P_0(x, z) = p_0 \cos(k_x x) \cos(k_z z)$, with $k_z = \pi / 2l$ and $k_x = (\varepsilon_{\parallel} c)^{-1/4} (\pi / 2l)^{1/2}$, and appears at

$$a_c \approx -\sqrt{\frac{c}{\varepsilon_{\parallel}}} \frac{\pi}{l}. \quad (3)$$

The parameters entering in this expression can be estimated as $\varepsilon_{\parallel} / \varepsilon_0 \sim 1 - 100$ and $c \sim d_{at}^2 / \varepsilon_0$, where d_{at} is the characteristic atomic distance ($c \sim 10^{-9} - 10^{-11} \text{ J m}^3 / \text{C}^2$, see e.g., Ref. 6). In the FET setups $w, l \gg d_{at}$, and consequently $a_c \gg a_*$. So, in fact, much before the paraelectric phase can get unstable with respect to the uniform polarization, the ferroelectric transits into its (multidomain) ferroelectric phase at a_c . At this point, the body factor in Eq. (2) takes the value

$$m_{\min} \approx 1 - \frac{\varepsilon_s}{\varepsilon_{\parallel}} \frac{\pi \sqrt{\varepsilon_{\parallel} c}}{w}, \quad (4)$$

which we anticipate to be the minimum obtainable in the ferroelectric FET. It is worth noting that m_{\min} depends on material parameters of both the semiconductor and the ferroelectric but not on the thickness of this later. The above numbers give $m_{\min} \sim 0.99$ only, though this could be further reduced to ~ 0.7 considering the state-of-the-art semiconductor capacitance $C_s = 0.1 \text{ F/m}^2$ (which however requires strong doping and therefore is beyond our model).

As we have mentioned, the expression (2) for the body factor is valid as long as the ferroelectric stays in its paraelectric phase. That is, for $a \geq a_c$. To obtain the corre-

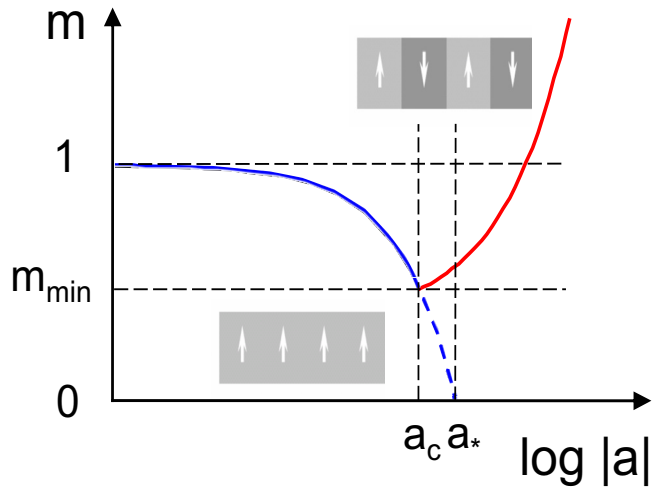


FIG. 3. (Color online) Schematic behavior of the ferroelectric FET body factor m as a function of the control parameter $a = a'(T - T_c^0)$: (blue color online) ignoring nonuniform distributions of polarization (red color online) taking into account multidomain ferroelectricity. Since ferroelectricity is expected in a multidomain state, m remains finite with its minimum at the corresponding transition point a_c . Otherwise it could be downed to zero at the paraelectric \leftrightarrow uniform ferroelectric transition point a_* .

sponding expression for $a \leq a_c$ it is important to take into account that there is a nonzero background polarization in the ferroelectric. Close to the transition point such a polarization is well described by the polarization wave P_0 found before and, to our purposes, higher harmonics can be neglected. Within this approximation the amplitude of the polarization wave is $p_0 \cong \pm (4/3) \sqrt{|a - a_c|/b}$. Furthermore we express the total polarization as $P_{tot} = P_0(x, z) + \delta P$, where δP is due to the applied gate voltage, and linearize the equations with respect to this quantity ($P_{tot}^3 \cong P_0^3 + 3P_0^2 \delta P$). We then obtain the body factor

$$m \cong 1 + \varepsilon_s \frac{l}{w} \left(a_c + \frac{1}{3} |a - a_c| \right). \quad (5)$$

As we see, the body factor in fact increases once the ferroelectric enters in its (multidomain) ferroelectric phase. This hardening results from the cubic P^3 term that eventually stabilizes the system. Nevertheless, the ferroelectric stays in the negative capacitance regime for some range of temperatures below the transition point. The precise computation of this range requires to go beyond the single harmonic approximation to describe properly the evolution of the ferroelectric ground state, which is beyond the scope of the present work.

It is worth mentioning that the negative capacitance regime in the (multidomain) ferroelectric phase also manifests in the unusual hysteresis loops with negative slopes described in Ref. 7 to rationalize experimental data on ferroelectric thin films.⁸ The behavior of the body factor is illustrated in Fig. 3 as a function of the control parameter a . The maximum amplification of the gate voltage corresponds to Eq. (4) at the transition point a_c . We note that, in order to obtain a significant gain, the semiconductor capacitance should be engineered to be $C_s = (\sqrt{\varepsilon_{||}}/c) / \pi$ per surface area. This design rule is independent of the ferroelectric thickness. Such a thickness simply sets the amplification window that, for practical purposes, has to be tuned about room temperature. In a multidomain scenario the gradient coefficient c plays a more important role, giving the above design rule in sharp contrast the reported in Ref. 2.

In conclusion, we have shown that appearance of multidomain ferroelectricity may substantially limit the maximum voltage amplification expected in ferroelectric FETs.

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¹International Technology Roadmap for Semiconductors, 2009 Edition. www.itrs.net.

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³See, e.g., M. Dawber, K. M. Rabe, and J. F. Scott, *Rev. Mod. Phys.* **77**, 1083 (2005), and references therein.

⁴See, e.g., A. M. Bratkovsky and A. P. Levanyuk, *J. Comput. Theor. Nanosci.* **6**, 465 (2009), and references therein.

⁵Experimentally, suitable ferroelectric-semiconductor interfaces are difficult to process and buffer layers are frequently needed to avoid, e.g., interdiffusion problems. In addition, different species such as SiO_x may appear at the interface. This can be seen as an additional capacitance C_{int} in series with the semiconductor capacitance C_s . Its influence on the body factor can be easily taken into account by replacing $C_s = \varepsilon_s/w$ in Eqs. (2), (4), and (5) by their resulting effective capacitance $C_s C_{int} / (C_s + C_{int})$.

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