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MULTILEVEL CONVERTERS - A NEW BREED OF POWER CONVERTERS

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Abstract-Multilevel voltage source converters are emerging as a new breed of power converter options for high-power applications. The multilevel voltage source converters typically synthesize the staircase voltage wave from several levels of dc capacitor voltages. One of the major limitations of the multilevel converters is the voltage unbalance between different levels. The techniques to balance the voltage between different levels normally involve voltage clamping or capacitor charge control. There are several ways of implementing voltage balance in multilevel converters. Without considering the traditional magnetic coupled converters, this paper presents three recently developed multilevel voltage source converters: (1) diode-clamp, (2) flying-capacitors, and (3) cascadedinverters with separate dc sources. The operating principle. features, constraints, and potential applications of these converters will be discussed.

I. INTRODUCTION

Recently the "multilevel converter" has drawn tremendous interest in the power industry $[1\sim12]$. The general structure of the multilevel converter is to synthesize a sinusoidal voltage from several levels of voltages, typically obtained from capacitor voltage sources. The so-called "multilevel" starts from three levels. A three-level converter, also known as a "neutral-clamped" converter, consists of two capacitor voltages in series and uses the center tap as the neutral [13]. Each phase leg of the three-level converter has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The waveform obtained from a three-level converter is a quasi-square wave output.

The diode-clamp method can be applied to higher level converters [6]. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase wave which approaches the sinusoidal wave with minimum harmonic distortion [14]. Ultimately, a zero harmonic distortion of the output wave can be obtained by an infinite number of levels. More levels also mean higher

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voltages can be spanned by series devices without device voltage sharing problems. Unfortunately, the number of the achievable voltage levels is quite limited not only due to voltage unbalance problems but also due to voltage clamping requirement, circuit layout, and packaging constraints. To date, hardware implementation has only been reported up to six levels for a back-to-back intertie application [9], in which the voltage unbalance problem has been successfully overcome.

The magnetic transformer coupled multi-pulse voltage source converter has been a well-known method and has been implemented in 18- and 48-pulse converters for battery storage and static condenser (STATCON) energy applications, respectively [15,16]. Traditional magnetic coupled multipulse converters typically synthesize the staircase voltage wave by varying transformer turns ratio with complicated zig-zag connections. Problems of the magnetic transformer coupling method are bulky, heavy, and lossy. The capacitor voltage synthesis method is thus preferred to the magnetic coupling method. There are three reported capacitor voltage synthesis based multilevel converters: (1) diode-clamp, (2) flying-capacitors, and (3) cascaded-inverters with separated dc sources.

This paper will describe operating principles of these capacitor voltage synthesis multilevel converters. Based on the features and constraints, the application areas of these multilevel converters will be addressed.

II. DIODE-CLAMP MULTILEVEL CONVERTER

A. Basic Principle

An *m*-level diode-clamp converter typically consists of m-1 capacitors on the dc bus and produces m levels of the phase voltage. Fig. 1 shows a single-phase full bridge fivelevel diode-clamp converter in which the dc bus consists of four capacitors, C_1 , C_2 , C_3 , and C_4 . For a dc bus voltage V_{dc} the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dr}/4$, through clamping diodes.

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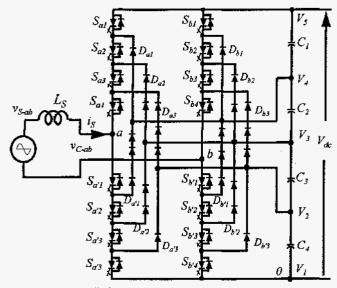


Fig. 1. A diode-clamp 5-level converter circuit diagram

To explain how the staircase voltage is synthesized, the negative dc rail, θ , is considered as the output phase voltage reference point. Using the 5-level converter shown in Fig. 1 as an example, there are five switch combinations to synthesize five level voltages across a and θ .

- (1) For voltage level $V_{a0} = V_{dc}$, turn on all upper switches S_{al} through S_{al} .
- (2) For voltage level $V_{a\theta}=3V_{dc}/4$, turn on three upper switches S_{a2} through S_{a4} and one lower switch $S_{a''}$.
- (3) For voltage level $V_{a0} = V_{dc}/2$, turn on two upper switches S_{a3} and S_{a4} and two lower switches $S_{a'1}$ and $S_{a'2}$.
- (4) For voltage level $V_{a0} = V_{dc}/4$, turn on one upper switches S_{a1} and three lower switches S_{a1} through S_{a3} .
- (5) For voltage level $V_{a0}=0$, turn on all lower half switches $S_{a'i}$ through $S_{a'i}$.

Table I lists the voltage levels and their corresponding switch states. State condition 1 means the switch is on, and 0 means the switch is off. Notice that each switch is only switched once per cycle. There exist four complimentary switch pairs in each phase. The complimentary switch pair is defined such that turning on one of the pair switches will exclude the other from being turned on. Using phase-leg *a* as the example, the four complementary pairs are $(S_{a1}, S_{a'1})$, $(S_{a2}, S_{a'2}), (S_{a3}, S_{a'3})$, and $(S_{a4}, S_{a'4})$.

TABLE I Diode-clamp 5-level converter voltage levels and their corresponding switch states

Switch States								
Output	Switch State							
V _{a0}	Sal	S_{a2}	S _{a3}	S _{a4}	$S_{a'I}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	0	l	1	1	1	0	0	0
$V_3 = V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2 = V_{dc}/4$	0	0	0	1	1	1	1	0
$V_I = 0$	0	0	0	0	1	1	1	1

Fig. 2 shows phase and line voltage waveforms of the example 5-level converter. The line voltage consists of a positive phase-leg a voltage and a negative phase-leg b voltage. Each phase voltage tracks one-half of the sinusoidal wave. The resulting line voltage is a 9-level staircase wave. This implies that an *m*-level converter has an *m*-level output phase voltage and a (2m-1)-level output line voltage.

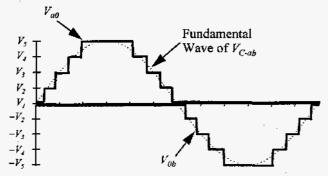


Fig. 2. Phase and line voltage waveforms of a 5-level diode-clamp voltage source converter.

B. Features

High Voltage Rating Required for Blocking Diodes

Although each active switching device is only required to block a voltage level of $V_{dc}/(m-1)$, the clamping diodes need to have different voltage ratings for reverse voltage blocking. Using $D_{a'i}$ of Fig. 1 as an example, when all lower devices, $S_{a'i} \sim S_{a'i}$ are turned on, $D_{a'i}$ needs to block three capacitor voltages, or $3V_{dc}/4$. Similarly, D_{a2} and $D_{a'2}$ need to block $2V_{dc}/4$, and D_{a3} needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be $(m-1)\times(m-2)$. This number represents a quadratic increase in m. When m is sufficiently high, the number of diodes required will make the system impractical to implement.

Unequal Device Rating

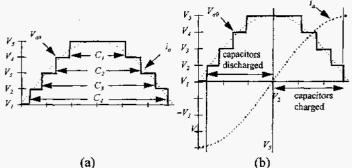
From Table 1, it can be seen that switch S_{a1} conducts only during $V_{a0} = V_{dc}$, while switch S_{a4} conducts over the entire cycle except $V_{a0} = 0$. Such an unequal conduction duty requires different current ratings for switching devices. When the inverter design is to use the average duty for all devices, the outer switches may be oversized, and the inner switches may be undersized. If the design is to suit the worst case, then there will be $(m-1)\times(m-2)/2$ devices oversized.

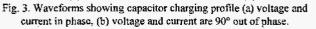
Capacitor Voltage Unbalance

In most applications, a power converter needs to transfer real power from ac to dc (rectifier) or dc to ac (inverter operation). When operating at unity power factor, the charging time for rectifier operation (or discharging time for inverter operation) for each capacitor is different, as shown in Fig. 3(a). Such a capacitor charging profile repeats every half cycle, and the result is unbalanced capacitor voltages between different levels.

The voltage unbalance problem in a multilevel converter can be solved by several approaches, such as replacing capacitors by a controlled constant dc voltage source such as pulse-width modulation (PWM) voltage regulators or batteries. The use of a controlled dc voltage will result in system complexity and cost penalties. With the high power nature of utility power systems, the converter switching frequency must be kept to a minimum to avoid switching losses and electromagnetic interference (EMI) problems.

When operating at zero power factor, however, the capacitor voltages can be balanced by equal charge and discharge in one-half cycle, as shown in Fig. 3(b). This indicates that the converter can transfer pure reactive power without the voltage unbalance problem.





In summary, advantages and disadvantages of a diodeclamp multilevel voltage source converter are as follows. Advantages:

- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Efficiency is high because all devices are switched at the fundamental frequency.
- Reactive power flow can be controlled.
- The control method is simple for a back-to-back intertie system.

Disadvantages:

- Excessive clamping diodes are required when the number of levels is high.
- It is difficult to do real power flow control for the individual converter.

III. MULTILEVEL CONVERTER USING FLYING-CAPACITORS

A. Basic Principle

Fig. 4 illustrates the fundamental building block of a single-phase full-bridge flying-capacitor based 5-level converter [5]. Each phase-leg has an identical structure. Assuming that each capacitor has the same voltage rating, the

series connection of capacitors in Fig. 4 is to indicate the voltage level between the clamping points. Three inner-loop balancing capacitors for phase leg a, C_{ai} , C_{a2} , and C_{a3} are independent from those for phase leg b. All phase legs share the same dc link capacitors, $C_{i}\sim C_{4}$.

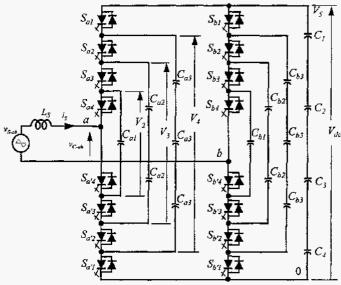


Fig. 4. Circuit diagram of a flying capacitor based 5-level single-phase voltage source converter.

The voltage level defined in the flying-capacitor converter is similar to that of the diode-clamp type converter. The phase voltage of an *m*-level converter has *m* levels including the reference level, and the line voltage has (2m-1)levels. Assuming that each capacitor has the same voltage rating as the switching device, the dc bus needs (m-1)capacitors for an *m*-level converter.

The voltage synthesis in a flying-capacitor converter has more flexibility than a diode-clamp converter. Using Fig. 4 as the example, the voltage of the 5-level phase-leg *a* output with respect to the negative dc rail, V_{a0} , can be synthesized by the following switch combinations:

- (1) For voltage level $V_{a0} = V_{dc}$, turn on all upper switches S_{a1} through S_{a4} .
- (2) For voltage level $V_{a0}=3V_{dc}/4$, there are three combinations:

(a) S_{a1} , S_{a2} , S_{a3} , $S_{a'4}$ ($V_{a0} = V_{dc} - V_{dc}/4$), (b) S_{a2} , S_{a3} , S_{a4} , $S_{a'1}$ ($V_{a0} = 3V_{dc}/4$), and (a) $S_{a2} = S_{a3} = S_{a4} - S_{a'1} (V_{a0} = 2V_{dc}/4)$, $V_{a'1} = V_{a'1} + V_{a'1}$

- (c) S_{a1} , S_{a3} , S_{a4} , $S_{a'2}$ ($V_{a0} = V_{dc} 3V_{dc}/4 + V_{dc}/2$).
- (3) For voltage level $V_{a0} = V_{dc}/2$, there are six combinations: (a) $S_{a1}, S_{a2}, S_{a'3}, S_{a''} (V_{a0} = V_{dc} - V_{dc}/2)$, (b) $S_{a3}, S_{a4}, S_{a'1}, S_{a'2} (V_{a0} = V_{dc}/2)$, (c) $S_{a1}, S_{a3}, S_{a'2}, S_{a'4} (V_{a0} = V_{dc} - 3V_{dc}/4 + V_{dc}/2 - V_{dc}/4)$, (d) $S_{a1}, S_{a4}, S_{a'2}, S_{a'3} (V_{a0} = V_{dc} - 3V_{dc}/4 + V_{dc}/4)$, (e) $S_{a2}, S_{a4}, S_{a'1}, S_{a'3} (V_{a0} = 3V_{dc}/4 - V_{dc}/4 + V_{dc}/4)$, and (f) $S_{a2}, S_{a3}, S_{a'1}, S_{a'4} (V_{a0} = 3V_{dc}/4 - V_{dc}/4)$.

- (4) For voltage level $V_{a0}=V_{dc}/4$, there are three combinations:
 - (a) S_{al} , $S_{a'2}$, $S_{a'3}$, $S_{a'4}$ ($V_{a0} = V_{dc} 3V_{dc}/4$), (b) S_{a4} , $S_{a'1}$, $S_{a'2}$, $S_{a'3}$ ($V_{a0} = V_{dc}/4$), and (c) S_{a3} , $S_{a'1}$, $S_{a'2}$, $S_{a'4}$ ($V_{a0} = V_{dc}/2 - V_{dc}/4$).
- (5) For voltage level $V_{ab}=0$, turn on all lower switches $S_{a'l}$ through $S_{a'a'}$.

Table II lists a possible combination of the voltage levels and their corresponding switch states. Using such a switch combination, each device needs to be switched only once per cycle. According to the device turn-on time requirement listed in Table II, the flying-capacitor multilevel converter also has unequal device duty problems.

 TABLE II

 A possible switch combination for the flying capacitor based 5-level converter.

Convertor.								
Output	Switch State							
$V_{\alpha 0}$	Sal	S_{a2}	Sas	S_{a4}	$ S_{a'f} $	$S_{a'3}$	Sa'2	$S_{a'I}$
$V_5 = V_{dc}$	1	1	1	1	0	0	0	0
$V_4 = 3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3 = V_{dc}/2$	1	1	0	0	l	1	0	0
$V_2 = V_{dc}/4$	1	0	0	0	1	1	1	0
$V_I = 0$	0	0	0	0	1	1	ī	1

B. Features

Besides the difficulty of balancing voltage in real power conversion, the major problem in this inverter is the requirement of a large number of storage capacitors. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an *m*-level converter will require a total of $(m-1)\times(m-2)/2$ auxiliary capacitors per phase leg in addition to (m-1) main dc bus capacitors. With the assumption that all capacitors have the same voltage rating, an *m*-level diode-clamp inverter only requires (m-1)capacitors.

In order to balance the capacitor charge and discharge, one may employ two or more switch combinations for middle voltage levels (i.e., $3V_{dc}/4$, $V_{dc}/2$, and $V_{dc}/4$) in one or several fundamental cycles. Thus, by proper selection of switch combinations, the flying-capacitor multilevel converter may be used in real power conversions. However, when it involves real power conversions, the selection of a switch combination becomes very complicated, and the switching frequency needs to be higher than the fundamental frequency.

In summary, advantages and disadvantages of a flyingcapacitor multilevel voltage source converter are as follows.

Advantages:

- Large amount of storage capacitors provides extra ride through capabilities during power outage.
- Provides switch combination redundancy for balancing different voltage levels.

- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Both real and reactive power flow can be controlled, making a possible voltage source converter candidate for high voltage dc transmission.

Disadvantages:

- An excessive number of storage capacitors is required when the number of converter levels is high. Highlevel systems are more difficult to package and more expensive with the required bulky capacitors.
- The inverter control will be very complicated, and the switching frequency and switching losses will be high for real power transmission.

IV. MULTILEVEL CONVERTER USING CASCADED-INVERTERS WITH SEPARATE DC SOURCES

A. Basic Principle

A relatively new converter structure, cascaded-inverters with separate dc sources (SDCs) is introduced here. This new converter can avoid extra clamping diodes or voltage balancing capacitors. Fig. 5(a) shows the basic structure of the cascaded-inverters with SDCs, shown in a single-phase configuration. Each SDC is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series.

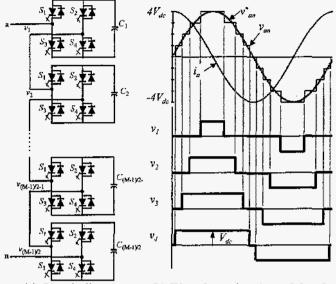
Fig. 5(b) shows the synthesized phase voltage waveform of a 9-level cascaded inverter with four SDCs. The phase output voltage is synthesized by the sum of four inverter outputs, i.e., $v_{am} = v_1 + v_2 + v_3 + v_4$. Each single-phase full bridge inverter can generate three level outputs, $+V_{dc}$, θ , and $-V_{dc}$. This is made possible by connecting the dc sources sequentially to the ac side via the four gate-turn-off devices. Each level of the full-bridge converter consists of four switches, S_1 , S_2 , S_3 , and S_4 . Using the top level as the example, turning on S_1 and S_4 yields $v_1 = +V_{dc}$. Turing on S_2 and S_3 yields $v_1 = -V_{dc}$. Turning off all switches yields $v_1 = 0$. Similarly, the ac output voltage at each level can be obtained in the same manner. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter levels.

With the phase current, i_a , leading or lagging the phase voltage v_{an} by 90°, the average charge to each dc capacitor is equal to zero over one line cycle, shown in Fig. 5(b). Therefore, all SDC capacitor voltages can be balanced.

To comply with the definition of the previously mentioned diode-clamp and flying-capacitor multilevel converters, the "level" in a cascaded-inverters based converter is defined by m=2s+1, where *m* is the output phase voltage level, and *s* is the number of dc sources. For example, a 9-level cascaded-inverters based converter will have four SDCs and four full bridges.

For a three-phase system, the output voltages of the three cascaded inverters can be connected in either Y- or Δ -

configuration [7]. Fig. 6 illustrates the connection diagram for a Y-configured 9-level converter using cascaded-inverters with four SDC capacitors.



(a) Circuit diagram (b) Waveform showing a 9-level converter phase voltage

Fig. 5. Circuit diagram and the phase voltage waveform of a cascadedinverters based converter with separate dc sources.

B. Features

For real power conversions, (ac to dc and dc to ac), the cascaded-inverter needs separate dc sources. The structure of separate dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic, and biomass, etc.

Connecting separated dc sources between two converters in a back-to-back fashion is not possible because a short circuit will be introduced when two back-to-back converters are not switching synchronously.

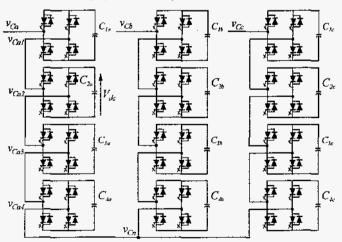


Fig. 6. A three-phase Y-configured cascaded-inverters based converter.

In summary, advantages and disadvantages of the cascaded-inverter based multilevel voltage source converter can be listed below.

Advantages:

- Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.
- Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors.
- Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers.

Disadvantages:

 Needs separate dc sources for real power conversions, and thus its applications are somewhat limited.

V. APPLICATIONS

A. Reactive Power Compensation

When a multilevel converter draws pure reactive power, the phase voltage and current are 90° apart, and the capacitor charge and discharge can be balanced [2,4,5,8]. Such a converter, when serving for reactive power compensation, is called a static var generator (SVG). The multilevel structure allows the converter to be directly connected to a high voltage distribution or transmission system without the need of a step-down transformer. Fig. 7 shows the circuit diagram of a multilevel converter directly connected to a power system for reactive power compensation.

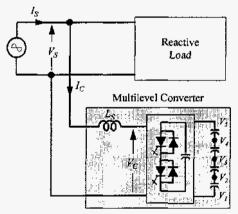


Fig. 7. Circuit diagram showing a multilevel converter connected to a power system for reactive power compensation.

The relationship of the source voltage vector, V_s , and the converter voltage vector, V_c , is simply $V_s = V_c + jI_c X_s$, where I_c is the converter current vector, and X_s is the impedance of the inductor, L_s . Fig. 8 illustrates the phasor diagram of the source voltage, converter voltage, and the converter current. Fig. 8(a) indicates that the converter voltage is in phase with the source voltage with a leading reactive current, while Fig. 8(b) indicates a lagging reactive current. The polarity and the magnitude of the reactive current are controlled by the magnitude of the converter voltage, V_c , which is a function of the dc bus voltage and the voltage modulation index.

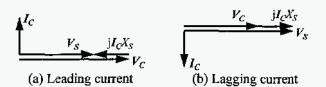


Fig. 8. Phasor diagrams showing the relationship between the source and the converter voltages for reactive power compensation.

All three multilevel converters can be used in reactive power compensation without having the voltage unbalance problem. The operating principle has been verified with computer simulations for all three types of multilevel converters. In hardware implementation, a 6-level diode clamp converter and an 11-level cascade-inverters based converter with 5 separate dc sources have been constructed using the Insulated Gate Bipolar Transistor (IGBT) as the switching device and a digital signal processor, TMS320C31, as a fully digital controller.

Fig. 9 shows the simulation results of a 5-level flying capacitor based converter using the switch combination stated in Table 2 for reactive power compensation. The converter voltage, V_C , is larger than the source voltage, V_S , and the converter current, I_C , is 90° leading the source voltage. As expected, different level capacitor voltages are well balanced without the need to vary the switch combination for middle-voltage levels. In actual implementation, a pure 90° leading or lagging current may not be possible due to the lossy inductor and the device voltage drop.

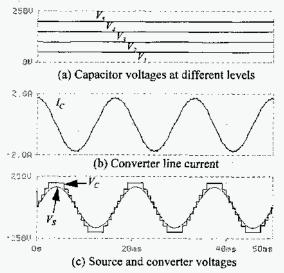


Fig. 9. Simulated results of the flying capacitor based 5-level converter for reactive power compensation.

Fig. 10 shows the experimental voltage and current waveforms of a 3-phase 6-level diode-clamp based converter using the switch combination listed in Table 1 for reactive power compensation. The oscillogram indicates that the input source line voltage, V_{S-ab} , and the converter line voltage, V_{C-ab} , are slightly out of phase. The source phase voltage and the line current, I_C , are not quite 90° apart. This

slight phase difference is due to the lossy component in the inductor and the device voltage drops.

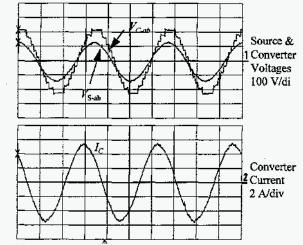


Fig. 10. Experimental results of a diode-clamp 6-level converter for reactive power compensation.

Fig. 11 shows the experimental line voltage and current waveforms of a 3-phase 11-level cascaded-inverters based converter for reactive power compensation. This figure indicates that the line voltage has 2m-1 or 21 levels.

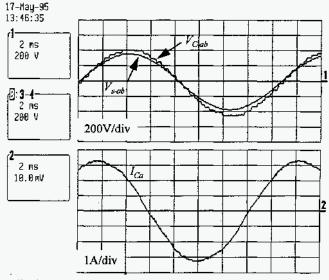
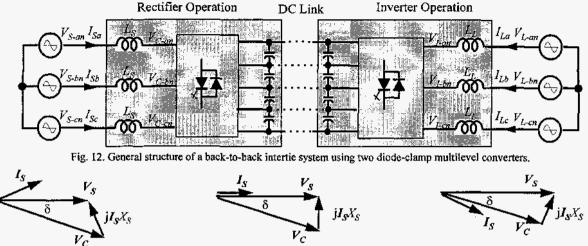


Fig. 11. Experimental results of an 11-level cascaded-inverter based converter for reactive power compensation.

B. Back-to-Back Intertie

When interconnecting two diode-clamp multilevel converters together with a "dc capacitor link," as shown in Fig. 12, the left-hand side converter serves as the rectifier for utility interface, and the right-hand side converter serves as the inverter to supply the ac load. Each switch remains switching once per fundamental cycle. The result is a wellbalanced voltage across each capacitor while maintaining the staircase voltage wave, because the unbalance capacitor voltages on both sides tend to compensate each other. Such a dc capacitor link is categorized as the "back-to-back intertie."



(a) Leading power factor

(b) Unity power factor

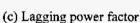


Fig. 13. Phasor diagram of the source voltage, converter voltage, and current showing real power conversions.

THD=0.95%

The purpose of the back-to-back intertie is to connect two asynchronous systems. It can be treated as (1) a frequency changer, (2) a phase shifter, or (3) a power flow controller. The power flow between two systems can be controlled bidirectionally.

Fig. 13 illustrates the phasor diagram for real power transmission from the source end to the load end. This diagram indicates that the source current can be leading or lagging the source voltage. The converter voltage is phase-shifted from the source voltage with a power angle, δ . If the source voltage is constant, then the current or power flow will be controlled by the converter voltage. For $\delta=0$, the current is either 90° leading or lagging, meaning that only reactive power is generated.

A 6-level "back-to-back" intertie hardware unit has been constructed and tested as a phase-shifter and a power flow controller. This unit also employs the IGBT as the switching device and TMS32031 as the controller. The two intertie systems contain a total of 60 switching devices, 60 built-in diodes, and 120 blocking diodes.

Fig. 14 shows experimental results of the utility input source line voltage, V_{S-ab} , the converter terminal line voltage, V_{C-ab} , and the source current, I_{Sar} operating at a lagging power factor condition. The oscillogram indicates that the current, I_{Sar} is 54° lagging the line voltage V_{S-ab} . This implies that phase *a* current is 24° lagging phase *a* voltage V_{S-an} . Fig. 15 shows experimental results at leading power factor condition. The line current is 20° lagging the line voltage or 10° leading the phase voltage. These two experimental results indicate that both real and reactive power flows can be controlled in a multilevel voltage source converter.

To show the superiority of the harmonic performance of the multilevel converter, the voltages and current obtained in Fig. 15 were analyzed with the Fourier series analysis. The resulting total harmonic distortions (THDs) are as follows.

Utility source voltage, V _{S-ab} :	THD=1.39%
Converter terminal voltage, V_{C-ab} :	THD=7.19%

These harmonic analysis results indicate that the THDs obtained from the multilevel converter are well within the limits of IEEE Std 519-1992 [18].

Source current Ise:

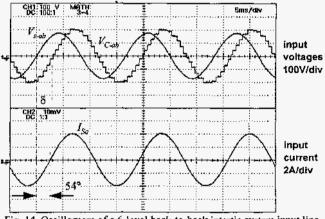


Fig. 14. Oscillogram of a 6-level back-to-back intertie system input line voltages and current operating at a lagging power factor condition.

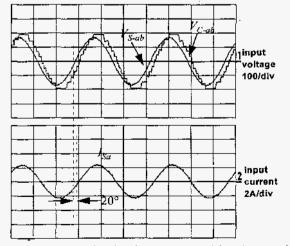
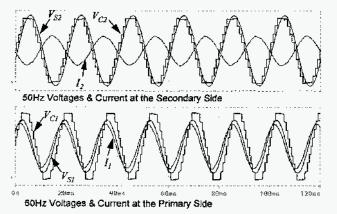


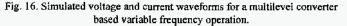
Fig. 15. Experimental results of a 6-level back-to-back intertie system input line voltages and current operating at a leading power factor condition.

C. Utility Compatible Adjustable Speed Drives

An ideal utility compatible system requires unity power factor, negligible harmonics, no EMI, and high efficiency. By extending the application of the back-to-back intertie, the multilevel converter can be used for a utility compatible adjustable speed drive (ASD) with the input from the utility constant frequency ac source and the output to the variable frequency ac load. The major differences, when using the same structure for ASDs and for back-to-back interties, are the control design and the size of the capacitor. Because the ASD needs to operate at different frequencies, the dc link capacitor needs to be well-sized to avoid a large voltage swing under dynamic conditions.

Fig. 16 shows the simulated input and output voltages and currents of a diode-clamp 5-level converter system for ASD applications. The input frequency is 60 Hz, and the output frequency is 50 Hz. The dc bus capacitor voltages are well balanced in the steady state.





VI. DISCUSSION AND CONCLUSION

A. Discussion

The multilevel converters can immediately replace the existing systems that use traditional multipulse converters without the need for transformers. For a 3-phase system, the relationship between the number of levels, m, and the number of pulses, p, can be formulated by $p=(m-1)\times 6$.

The SVG is an excellent target for commercialization of these multilevel converters in high-voltage high-power systems. All three converters introduced in this paper can be used as the static var generator. The second target could be the back-to-back intertie system for a unified power flow controller. The structure that is most suitable for the back-toback intertie is the diode-clamp type. The other two types may also be suitable for the back-to-back intertie, but they require more switchings per cycle and more sophisticated control to balance the voltage.

Table III compares the power component requirements per phase leg among the three multilevel voltage source converters mentioned above. This comparison assumes that all devices have the same voltage rating, but not necessarily the same current rating, and that the cascaded-inverters type uses a full bridge in each level as compared to the half-bridge version used in the other two types. The multilevel converter using cascaded-inverters requires the least number of components and is most promising for utility interface applications because of its capabilities of modularization and soft-switching.

 TABLE III

 Comparison of power component requirements per phase leg among three multilevel converters.

Converter Type	diode-clamp	flying- capacitors	cascaded- inverters
Main switching devices	(<i>m</i> -1)×2	(<i>m</i> -1)×2	(<i>m</i> -1)×2
Main diodes	(m-1)×2	(m-1)×2	$(m-1)\times 2$
Clamping diodes	$(m-1) \times (m-2)$	0	0
DC bus capacitors	(<i>m</i> -1)	(<i>m</i> -1)	(m-1)/2
Balancing capacitors	0	(<i>m</i> -1)×(<i>m</i> -2)/2	0

B. Conclusion

This paper has presented three transformerless multilevel voltage source converters that synthesize the converter voltage by equally divided capacitor voltages. All these converters have been completely analyzed and simulated. Two hardware models have been built and tested to verify the concept. Both simulation and experimental results prove that these multilevel converters are very promising for power system applications.

The application that has been mentioned most frequently in the literature is SVG. All three multilevel converters can be applied to SVGs without voltage unbalance problems because the SVG does not draw real power.

The application on which the multilevel voltage source converter may have the most impact is the adjustable speed drive. The industry recently reported numerous ASD bearing failures and winding insulation breakdowns due to high frequency switching PWM inverters. Using multilevel converters not only solves harmonics and EMI problems, but also avoids possible high frequency switching dv/dt induced motor failures.

With a balanced voltage stress in devices and utility compatible features, the multilevel converters have shed a light in the power electronics arena and are emerging as a new breed of power converters for high-voltage high-power applications.

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