Multilevel Converters for Large Electric Drives

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***Abstract*—This paper presents transformerless multilevel converters as an application for high-power and/or high-voltage electric motor drives. Multilevel converters: 1) can generate near-sinusoidal voltages with only fundamental frequency switching; 2) have almost no electromagnetic interference or common-mode voltage; and 3) are suitable for large voltampere-rated motor drives and high voltages. The cascade inverter is a natural fit for large automotive all-electric drives because it uses several levels of dc voltage sources, which would be available from batteries or fuel cells. The back-to-back diode-clamped converter is ideal where a source of ac voltage is available, such as in a hybrid electric vehicle. Simulation and experimental results show the superiority of these two converters over two-level pulsewidth-modulation-based drives.**

***Index Terms*—Cascade inverter, common-mode voltage, diode-clamped inverter, electric vehicle, motor drive, multilevel converter, multilevel inverter.**

I. Introduction

A. Background

DESIGNS FOR heavy-duty electric and hybrid-electric vehicles (EV's) that have large electric drives will require advanced power electronic inverters to meet the high power demands (>250 kW) required of them. Development of large electric drive trains for these vehicles will result in increased fuel efficiency, lower emissions, and likely better vehicle performance (acceleration and braking).

Transformerless multilevel inverters are uniquely suited for this application because of the high voltampere ratings possible with these inverters [1]. For EV's, a cascaded H-bridges inverter can be used to drive the traction motor from a set of batteries or fuel cells. Where generated ac voltage is available, such as from an alternator or generator, a back-to-back diode-clamped converter can convert this source to variable-frequency ac voltage for the driven motor.

Multilevel inverters also solve problems with some present two-level pulsewidth modulation (PWM) adjustable-speed drives (ASD's). ASD's usually employ a front-end diode rectifier to convert utility ac voltage to dc voltage and an inverter with PWM-controlled switching devices to convert the dc voltage to variable frequency and variable voltage for motor speed control.

Motor damage and failure have been reported by industry as a result of some ASD inverters' high-voltage change rates (dV/dt), which produced a common-mode voltage across the motor windings. High-frequency switching can exacerbate the problem because of the numerous times this common mode voltage is impressed upon the motor each cycle. The main problems reported have been "motor bearing failure" and "motor winding insulation breakdown" because of circulating currents, dielectric stresses, voltage surge, and corona discharge [2]–[4].

Only recently have motor insulation failures become a problem with some ASD's because the increased switching speed of contemporary power semiconductor devices causes steep voltage wavefronts to appear at the motor terminals. The voltage change rate (dV/dt) sometimes can be high enough to induce corona discharge between the winding layers.

Present power semiconductors can be turned on and off within 1 μs for 600 V and higher voltages which can generate broadband electromagnetic interference (EMI). These high-speed semiconductor switches allow faster PWM carrier frequencies. Although the high-frequency switching can increase the motor running efficiency and is well above the acoustic noise level, the dV/dt associated dielectric stresses between insulated winding turns are also greatly increased.

Some PWM-controlled inverters can also cause large instantaneous common-mode voltages to appear at the motor terminals. These common-mode voltages appear across the motor shaft to ground and induce bearing currents, which lead to erosion of the bearing material and early mechanical failure.

Multilevel inverters overcome these problems because their individual devices have a much lower dV/dt per switching, and they operate at high efficiencies because they can switch at a much lower frequency than PWM-controlled inverters.

B. Multilevel Inverters

The multilevel voltage source inverters' unique structure allows them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized-switching devices. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages. For this reason, multilevel inverters can easily provide the high power required of a large electric drive.

As the number of levels increases, the synthesized output waveform has more steps, which produces a staircase wave that approaches a desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels in-

Paper IPCSD 98–68, presented at the 1998 IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, February 15–19, and approved for publication in the IEEE Transactions on Industry Applications by the Industrial Drives Committee of the IEEE Industry Applications Society. Manuscript released for publication September 8, 1998.

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Publisher Item Identifier S 0093-9994(99)00454-5.

creases. As the number of levels increases, the voltage that can be spanned by summing multiple voltage levels also increases. The structure of the multilevel inverter is such that no voltage sharing problems are encountered by the active devices.

Researchers have proposed three main types of transformerless multilevel inverters thus far, the diode-clamped inverter, the flying-capacitor inverter, and the cascade inverter. Proposed uses for these converters have included static var compensation [5]–[12], back-to-back high-voltage intertie [13]–[15], and ASD's [15]–[20].

Using multilevel inverters as drives for electric motors is a much different application than for the utility applications for which they were originally developed. Only reactive power flows between the converter and the system in static var compensation, whereas the converter must handle bidirectional real power flow in the case of motor drives.

Three-, four-, and five-level rectifier-inverter drive systems that have used some form of multilevel PWM as a means to control the switching of the rectifier and inverter sections have been investigated in the literature [16]–[20]. Multilevel PWM has lower dV/dt than that experienced in some two-level PWM drives because switching is between several smaller voltage levels. However, switching losses and voltage total harmonic distortion (THD) are still relatively high for these proposed schemes; the output voltage THD was reported to be 19.7% for a four-level PWM inverter without any output filters [19].

This paper proposes two multilevel inverter configurations where devices are switched only at the fundamental frequency and the inverter output line voltage THD is 5% without the use of any filtering components. In addition, a control scheme will be demonstrated in the multilevel diode-clamped converter that obtains well-balanced voltages across the dc-link capacitors.

II. CASCADED H-BRIDGES INVERTER

A. General Structure and Operation

A cascaded multilevel inverter consists of a series of H-bridge (single-phase full-bridge) inverter units. The general function of this multilevel inverter is to synthesize a desired voltage from several separate dc sources (SDCS's), which may be obtained from batteries, fuel cells, or solar cells. Fig. 1 shows a single-phase structure of a cascade inverter with SDCS's [6]. Each SDCS is connected to a single-phase full-bridge inverter. Each inverter level can generate three different voltage outputs, $+V_{\rm dc}$, 0, and $-V_{\rm dc}$, by connecting the dc source to the ac output side by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{\rm dc}$, switches S_1 and S_4 are turned on. Turning on switches S_2 and S_3 yields $-V_{\rm dc}$. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0.

The ac outputs of each of the different level full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels in a cascade inverter is defined by $m = 2s+1$, where s is the number of dc sources. An example phase voltage waveform for an 11-level cascaded inverter with five SDSC's and five full bridges is shown in Fig. 2. The phase voltage $v_{an} = v_{a1}+v_{a2}+v_{a3}+v_{a4}+v_{a5}$.

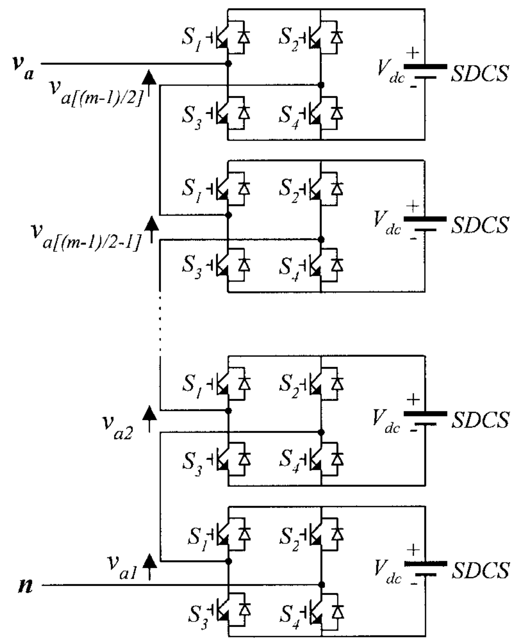


Fig. 1. Single-phase structure of a multilevel cascaded H-bridges inverter.

The output voltage of the inverter is almost sinusoidal, and it has less than 5% THD with each of the H-bridges switching only at fundamental frequency. Each H-bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase legs' switching timings. Fig. 2(b) shows the switching timings to generate a quasi-square waveform. Note that each switching device always conducts for 180° (or 1/2 cycle), regardless of the pulsewidth of the quasi-square wave. This switching method makes all of the active devices' current stress equal.

For a stepped waveform such as the one depicted in Fig. 2 with s steps, the Fourier transform for this waveform is as follows:

$$V(\omega t) = \frac{4V_{\rm dc}}{\pi}\sum_n [\cos(n\theta_1)+\cos(n\theta_2)+\cdots+\cos(n\theta_s)] \times \frac{\sin(n\omega t)}{n}, \quad \text{where } n = 1,3,5,7,\cdots. \tag{1}$$

From (1), the magnitudes of the Fourier coefficients when normalized with respect to $V_{\rm dc}$ are as follows:

$$H(n) = \frac{4}{\pi n}[\cos(n\theta_1)+\cos(n\theta_2)+\cdots+\cos(n\theta_s)], \quad \text{where } n = 1,3,5,7,\cdots. \tag{2}$$

The conducting angles $\theta_1, \theta_2, \ldots \theta_s$ can be chosen such that the voltage total harmonic distortion is a minimum. Normally, these angles are chosen so as to cancel the predominant lower frequency harmonics [6], [12]. For the 11-level case in Fig. 2, the 5th, 7th, 11th, and 13th harmonics can be eliminated with the appropriate choice of the conducting angles. One degree of freedom is used so that the magnitude of the output waveform corresponds to the reference amplitude modulation index m_a which is defined as $V_L^*/V_{L\max}$, where V_L^* is the amplitude command of the inverter output phase voltage, and $V_{L\max}$

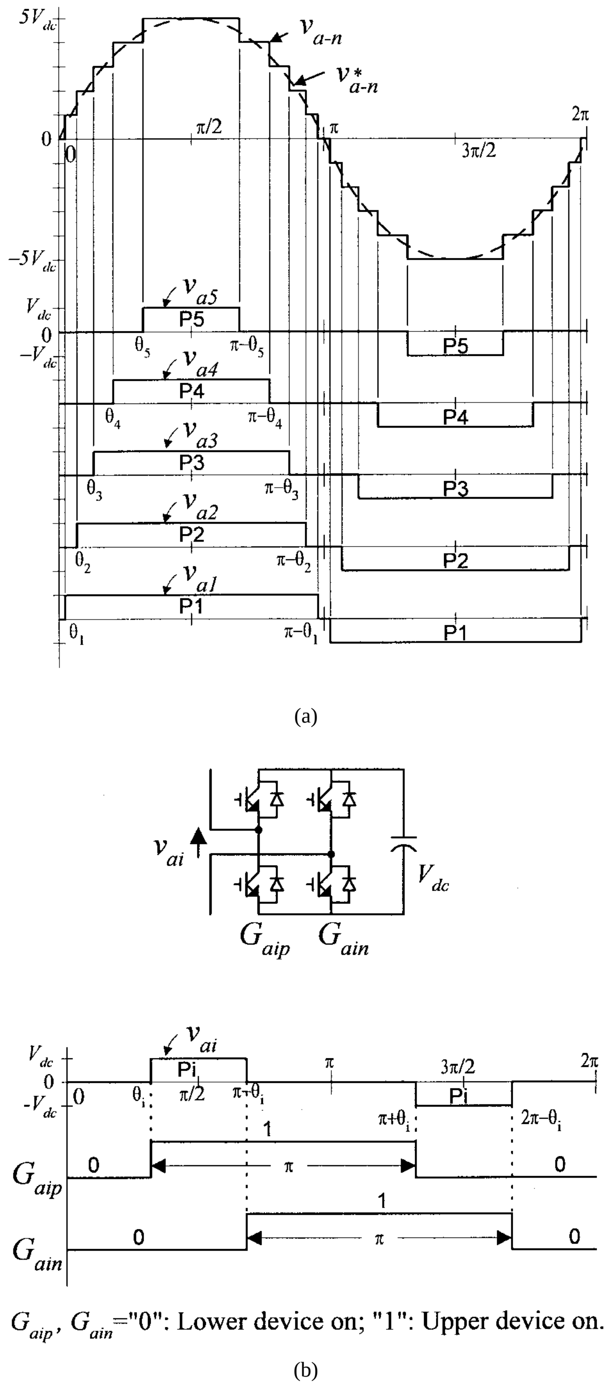


Fig. 2. Waveforms and switching method of the 11-level cascade inverter.

is the maximum attainable amplitude of the converter, i.e., $V_{L\max} = s \cdot V_{\rm dc}$ [15]. Let the equations from (2) be as follows:

$$\begin{aligned} &\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0 \\ &\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0 \\ &\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) \\ &\qquad + \cos(11\theta_5) = 0 \\ &\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) \\ &\qquad + \cos(13\theta_5) = 0 \\ &\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) = 5m_a. \end{aligned} \tag{3}$$

The set of nonlinear transcendental equations (3) can be solved by an iterative method such as the Newton–Raphson method. For example, using a modulation index m_a of 0.8 obtains

$$\theta_1 = 6.57^\circ, \quad \theta_2 = 18.94^\circ, \quad \theta_3 = 27.18^\circ$$
$$\theta_4 = 45.15^\circ, \quad \theta_5 = 62.24^\circ.$$

This means that, if the inverter output is symmetrically switched during the positive half cycle of the fundamental voltage to $+V_{\rm dc}$ at 6.57°, $+2V_{\rm dc}$ at 18.94°, $+3V_{\rm dc}$ at 27.18°, $+4V_{\rm dc}$ at 45.14°, and $+5V_{\rm dc}$ at 62.24°, and similarly in the negative half cycle to $-V_{\rm dc}$ at 186.57°, $-2V_{\rm dc}$ at 198.94°, $-3V_{\rm dc}$ at 207.18°, $-4V_{\rm dc}$ at 225.14°, and $-5V_{\rm dc}$ at 242.24°, the output voltage of the 11-level inverter will not contain the 5th, 7th, 11th, and 13th harmonic components.

From Fig. 2, note that the duty cycle for each of the voltage levels is different. If this same pattern of duty cycles is used on a motor drive continuously, then the level-1 battery (or other SDCS) is cycled on for a much longer duration than the level-5 battery. This means that the level-1 battery will discharge much sooner than the level-5 battery. However, by using a switching pattern-swapping scheme among the various levels every 1/2 cycle, as shown in Fig. 3, all batteries will be equally used (discharged) or charged.

The combination of the 180° conducting method [Fig. 2(b)] and the pattern-swapping scheme (Fig. 3) make the cascade inverter's voltage and current stresses the same and keeps the batteries' charge state balanced. Identical H-bridge inverter units can be utilized, thus improving modularity and manufacturability and greatly reducing production costs.

B. Three-Phase Motor Drive

For a three-phase system, the output voltages of three single-phase cascaded inverters can be connected in either a wye or delta configuration. Fig. 4 illustrates the connection diagram for a wye-configured 11-level converter using cascaded inverters with five SDCS's per phase. In the motoring mode, power flows from the batteries through the cascade inverters to the motor. In the charging mode, the cascade converters act as rectifiers, and power flows from the charger (ac source) to the batteries.

Fig. 5 shows the system configuration and control block diagram of an ASD using an 11-level cascade inverter. The duty cycle lookup table contains switching timings to generate the desired output voltage, as shown in Fig. 2. The five switching angles θ_i, $(i = 1, 2, 3, 4, 5)$ are calculated off-line to minimize harmonics for each modulation index, m_a.

A prototype three-phase 11-level wye-connected cascaded inverter has been built using insulated gate bipolar transistors (IGBT's) as the switching devices. A battery bank of 15 SDCS's of 48 Vdc each fed the inverter (5 SDCS's per phase). The control of the inverter was via a 32-bit digital signal processor. The switching timing angles θ_i $(i = 1, 2, 3, 4, 5)$ were calculated off-line for the following modulation indexes: $(m_a = 0.1, 0.2, \cdots, 1.0)$. A table of ten switching patterns corresponding to these modulation indexes was stored in

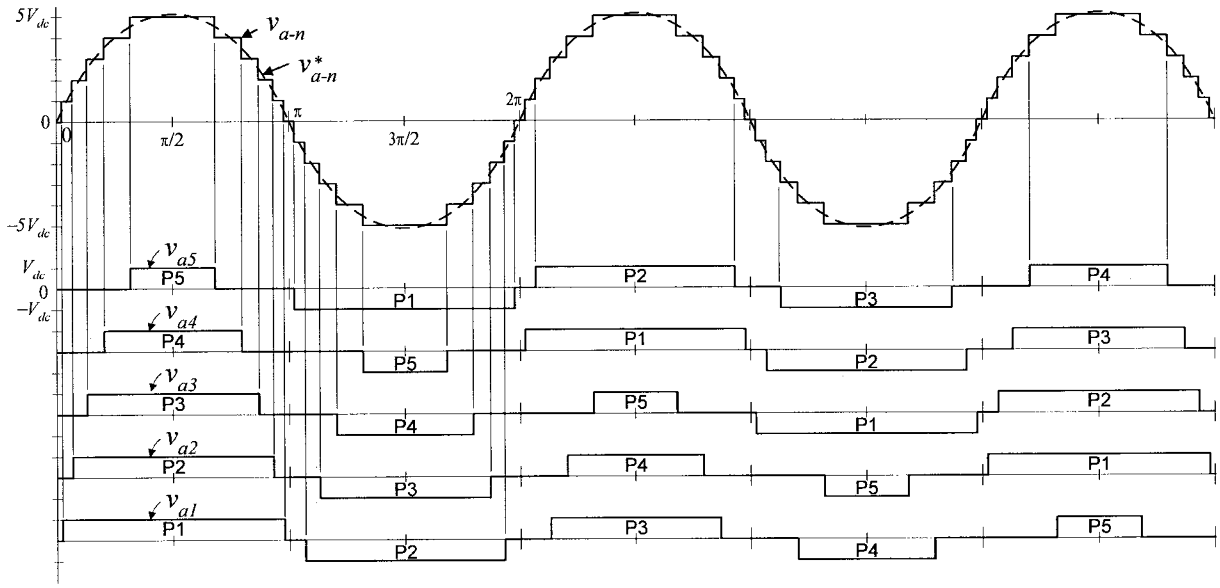


Fig. 3. Switching pattern swapping of the 11-level cascade inverter for balancing battery charge.

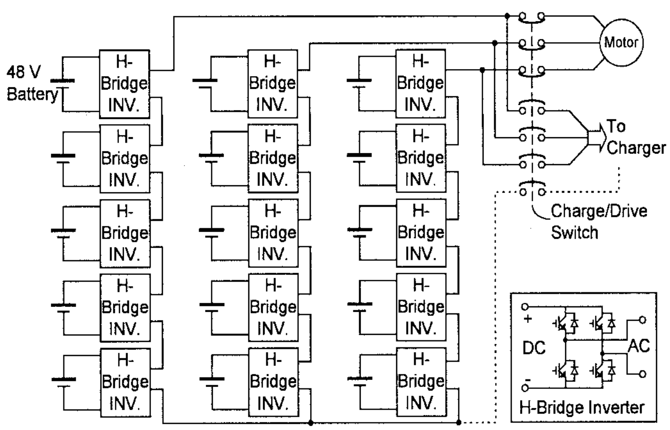


Fig. 4. System configuration of an EV motor drive using a cascade inverter.

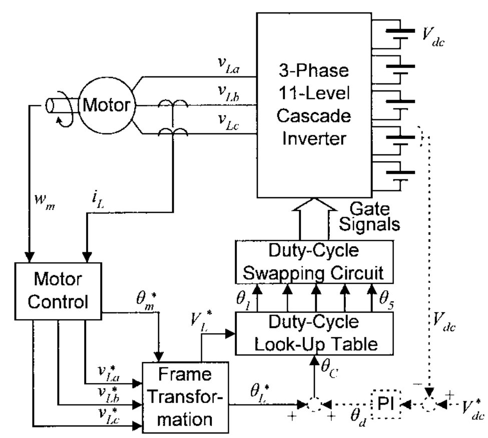


Fig. 5. System configuration of an ASD using the cascade inverter.

the controller as 1024 states per cycle. A constant voltage/frequency control technique was applied to the motor drive system. As a user interface, a potentiometer was adjusted to apply an external 0–3-V signal to the controller. The 0–3-V signal mapped directly to a 0–60-Hz fundamental frequency for the gate signals sent to the inverter. Also, the switching patterns corresponding to the various modulation indexes were mapped from the 0–3-V external control signal.

Fig. 6 shows experimental waveforms of the 11-level battery-fed cascade inverter prototype driving a 208-V three-phase induction motor at 50% and 80% rated speed using the aforementioned fundamental frequency switching scheme. As can be seen from the waveforms, both the line–line voltage and current are almost sinusoidal. EMI and common-mode voltage are also much less than what would result from a two-level PWM inverter because of the inherently low dV/dt (21 times less than a two-level drive) and sinusoidal voltage output.

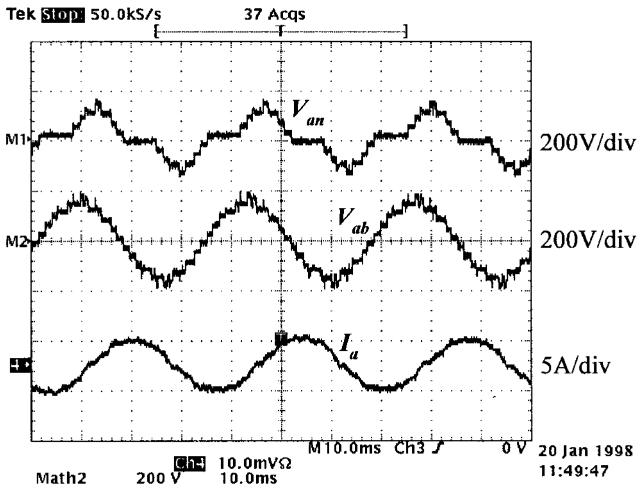
III. Back-to-Back Diode-Clamped Converter Drive

While cascade inverters are ideal where separate dc sources are available, in most instances, an ac voltage source is the only convenient power supply. For these cases, a multilevel back-to-back diode-clamped converter can best interface with the source of ac power and yet still meet the high-power and/or high-voltage requirements of the driven motor.

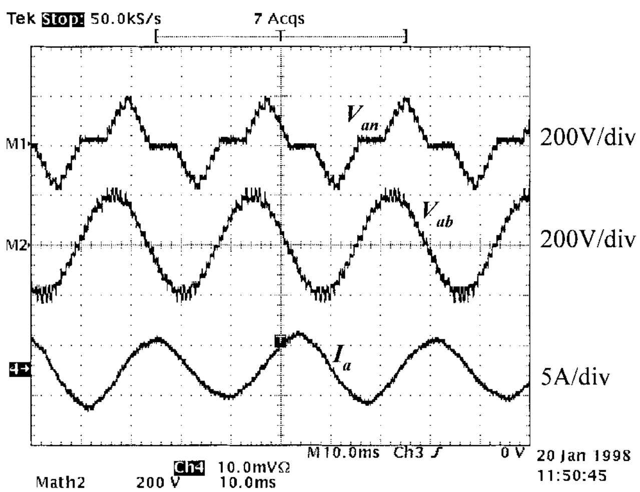
Two six-level diode-clamped inverters connected back-to-back are shown in Fig. 7. The dc bus for these two inverters consists of a series of electric energy storage devices—batteries or capacitors. The voltage across each storage device is $V_{\rm dc}$. The voltage stress across each switching device is limited to $V_{\rm dc}$ through the clamping diodes.

A. General Structure and Operation

Table I lists the voltage output levels possible for one phase of the diode-clamped inverter using the negative dc rail V_0 as a reference voltage. State condition 1 means the corresponding



(a)



(b)

Fig. 6. Experimental waveforms of a battery-fed cascade inverter prototype driving an induction motor at (a) 50% rated speed and (b) 80% rated speed.

switch is on, and 0 means the switch is off. Note that each active device is only switched once per cycle. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires that the other switch be turned off. The complementary switch pairs for phase leg a are $(S_{a1}, S_{a'1})$, $(S_{a2}, S_{a'2})$, $(S_{a3}, S_{a'3})$, $(S_{a4}, S_{a'4})$, and $(S_{a5}, S_{a'5})$.

Fig. 8 shows the voltage waveform for one phase of a six-level inverter. The line voltage V_{ab} consists of a phase-leg a voltage and a phase-leg b voltage. The resulting line voltage is an 11-level staircase waveform. This means that an m-level diode-clamped inverter has an m-level output phase voltage and a $(2m-1)$-level output line voltage [15].

Although each active switching device is only required to block a voltage level of $V_{\rm dc}$, the clamping diodes require different voltage ratings for reverse voltage blocking. Using phase a of Fig. 7 as an example, when all the lower switches $S_{a'1}$–$S_{a'5}$ are turned on, D_4 must block four voltage levels, or $4V_{\rm dc}$. Similarly, D_3 must block $3V_{\rm dc}$, D_2 must block $2V_{\rm dc}$, and D_1 must block $V_{\rm dc}$. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, D_n will require n diodes in series; consequently, the number of diodes required for each phase is $(m-1) \times (m-2)$. Thus, the number of blocking diodes are quadratically related to the number of levels in a diode-clamped converter [13]–[15].

B. Experimental Results

A six-level back-to-back 10-kW diode-clamped converter prototype that was designed to operate at a three-phase line voltage of 208 V has been built and experimentally tested as an ASD for an induction motor load. The controllable switching devices used for the converter were 100-V 100-A MOSFET's. Each internal dc level of the converter had a capacitance of 6.72 mF.

Fig. 9 shows the source voltage V_{Sab}, the source current I_{Sa}, drawn by the converter, the inverter output load voltage V_{Lab}, and the load current I_{La}, drawn by a 5-hp induction motor operating at 75% rated speed. This prototype diode-clamped rectifier drew a source current that had a THD of 3% and could be controlled such that the input power factor was 1.0. The output voltage at the motor terminals had a THD that varied between 4.5%–5.3%, and the converter output current had a THD of 3%.

Additionally, the experiment shows that the output line voltage dV/dt is reduced by 11 times with the six-level converter as compared to a traditional two-level PWM drive. The dramatic reduction in dV/dt by one order in magnitude and two orders in repetition (switching frequency) can prevent motor windings and bearings from failure. This 11-step staircase output voltage waveform approaches a sinewave, thus having no common-mode voltage and no voltage surge to the motor windings.

C. Efficiency

To compare the efficiencies of a multilevel inverter operating with fundamental frequency switching and a two-level inverter using PWM, the losses in the two inverters have to be characterized.

The losses in an inverter can be described by

$$P_{\rm loss} = P_c + P_{\rm sw} \tag{4}$$

where P_c is the conducting loss and $P_{\rm sw}$ is the switching loss.

In the fundamental frequency-controlled multilevel inverter, the switching power losses can be approximated by

$$P_{\text{sw-MFF}} = \left(A \cdot I_R + B \cdot I_R^2\right) f_m \tag{5}$$

where f_m is the frequency of the modulation, or reference, waveform. The switching power losses in a two-level PWM inverter can be approximated by

$$P_{\text{sw-PWM}} = \left(A \cdot I_R + B \cdot I_R^2\right) f_c, \tag{6}$$

where f_c is the frequency of the PWM carrier waveform [21]. If A and B are assumed to be the same for the active devices in the multilevel inverter and two-level PWM inverter, the difference in (5) and (6) is the factor f_c/f_m, which is known as

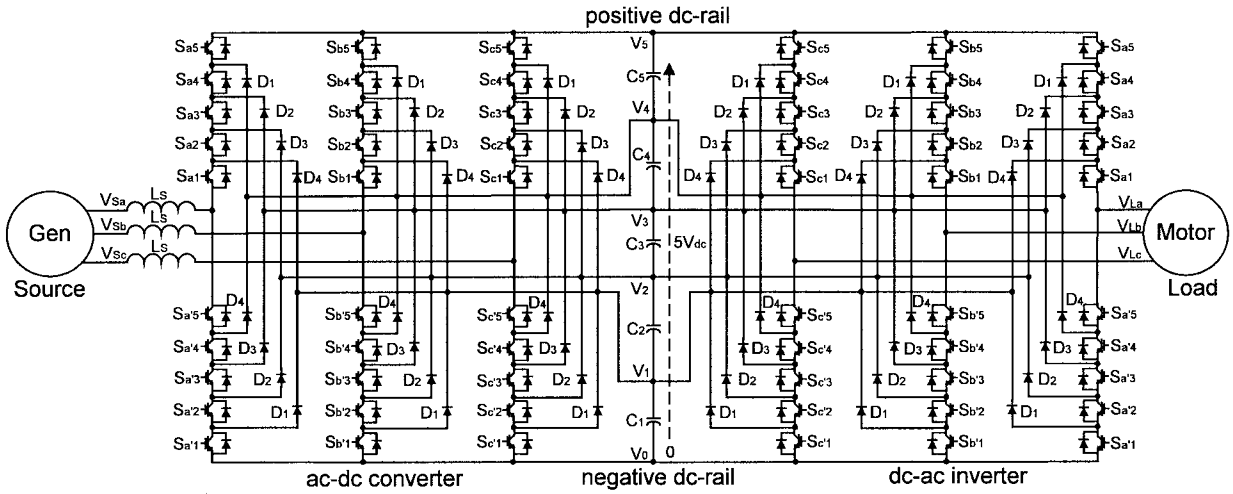


Fig. 7. Six-level diode-clamped back-to-back converter structure for adjustable-speed motor drive system.

TABLE I
DIODE-CLAMPED SIX-LEVEL CONVERTER VOLTAGE LEVELS AND CORRESPONDING SWITCH STATES

Output	Switch State									
V_{La}	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_1 = V_{dc}$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

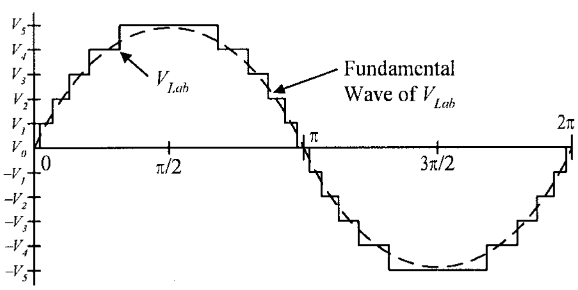


Fig. 8. Voltage waveform for six-level diode-clamped inverter.

the frequency modulation index m_f. Therefore, the switching losses in a two-level PWM inverter would be m_f times the switching losses in a comparable multilevel inverter using fundamental frequency switching techniques.

A simplified model of the solid-state devices is used in the derivation of the conduction losses in the two inverters. The model assumes that a constant voltage drop in series with a linear resistive element represents the device. These simplified models for an IGBT and diode, respectively, are given in (7) and (8) as

$$V_{CE} = V_t + I_R R_{CE} \tag{7}$$

$$V_{AK} = V_f + I_R R_{AK}. \tag{8}$$

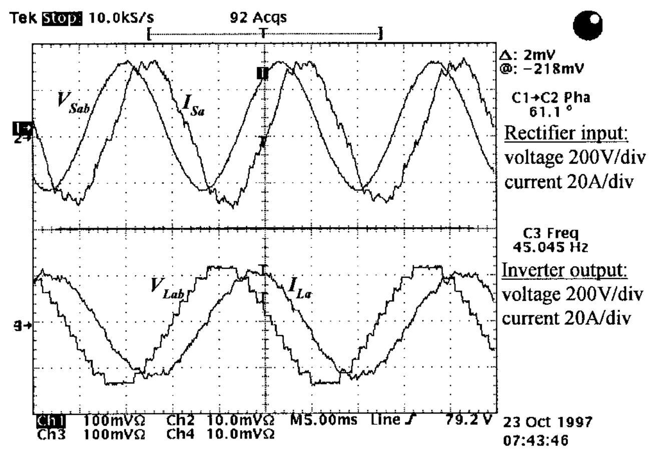


Fig. 9. Experimental voltage and current waveforms at the input and output of the back-to-back diode-clamped converter prototype.

The on-state voltage drops of the IGBT and diode, V_{CE} and V_{AK}, consist of voltage drops at zero-current condition, V_t and V_f, and the voltage drops because of the device current I_R flowing through resistive elements R_{CE} and R_{AK}. These device-dependent parameters can be obtained from manufacturers' data sheets [22].

In a three-phase full-bridge two-level PWM inverter, the conduction losses, for one active switching device and one antiparallel diode, respectively, are given by

$$P_{c\text{-sw}} = \frac{1}{2} I_R V_t \left(\frac{1}{\pi} + \frac{m_a}{4} p_f\right) + I_R^2 R_{CE} \left(\frac{\sqrt{3}}{8\sqrt{\pi}} + \frac{m_a}{3\pi} p_f\right) \tag{9}$$

$$P_{c\text{-}D} = \frac{1}{2} I_R V_f \left(\frac{1}{\pi} - \frac{m_a}{4} p_f\right) + I_R^2 R_{AK} \left(\frac{\sqrt{3}}{8\sqrt{\pi}} - \frac{m_a}{3\pi} p_f\right) \tag{10}$$

where p_f is the displacement power factor of the current with respect to the fundamental of the inverter's output voltage. The amplitude modulation index m_a and p_f in (9) and (10)

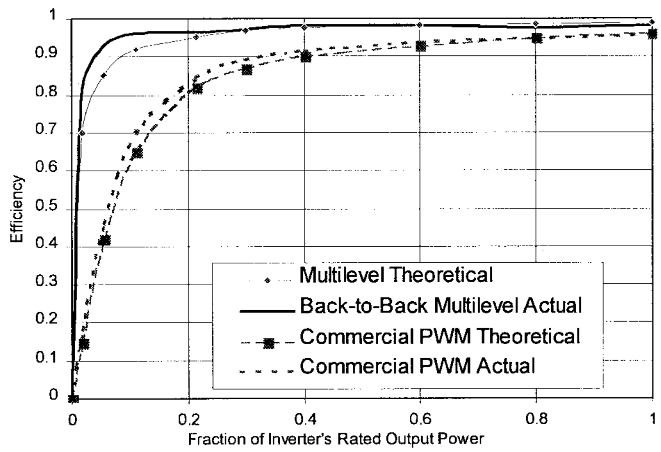


Fig. 10. Plot of inverter efficiency as a function of rated output power.

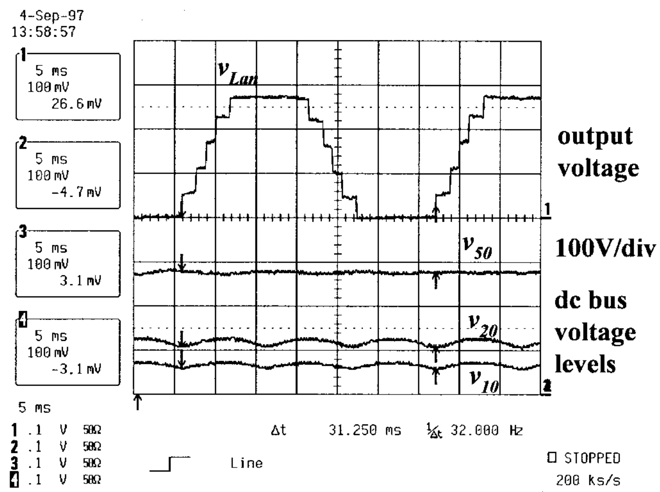


Fig. 11. Internal dc-bus voltage levels of the prototype diode-clamped back-to-back converter operating at an output frequency of 32 Hz.

affect the percentage of current that flows through the active devices and the percentage that flows through the diodes in a two-level inverter. The total conduction loss for all six devices in the full-bridge inverter can then be calculated from

$$P_{c\text{-PWM}} = 6(P_{c\text{-sw}} + P_{c\text{-}D}). \tag{11}$$

The unique structure of a multilevel inverter allows it to use active devices with lower voltage ratings. If the clamping diodes are assumed to have the same lower voltage rating as the active switches, the conduction losses are approximately

$$P_{c\text{-MFF}} = 6m_a(m-1)P_{c\text{-sw}} + 6(1-m_a)(m-1)P_{c\text{-}D}. \tag{12}$$

The amplitude modulation index and the power factor affect how many clamping diodes and how many active devices the current is flowing through on average for the multilevel inverter.

Equation (12) for the multilevel inverter under fundamental frequency switching control has an additional $(m-1)$ factor that (11) for the two-level PWM inverter does not have. However, a comparison of the conducting losses for the two inverters is largely dependent on the specific devices used in each because the saturation voltage V_{CE} and diode forward voltage V_{AK} are device dependent. Because the multilevel inverter can use switches and diodes with lower voltage ratings, these two values will usually be lower in the multilevel inverter. In general, the conducting losses in the two different inverters with the same power ratings will be similar in magnitude.

Fig. 10 shows a graph comparing the efficiency of the back-to-back multilevel converter to a typical industry PWM inverter (operating with a carrier frequency of 3 kHz) as a function of their fraction of rated output power. Using (4)–(11) and IGBT and MOSFET manufacturers' data sheets, the theoretical efficiency for the two different inverters was calculated at several different operating points from no load to full load. The actual efficiency for each of these two inverters, which was calculated from measured test data, was also plotted in Fig. 10. The actual efficiency for the multilevel converter, in fact, was for two multilevel inverters connected back-to-back.

In this instance, the theoretical equations tended to slightly underestimate the losses of the two inverters near full load and overestimate the losses of the inverters when they are lightly loaded. However, the equations did fairly accurately predict the actual losses in the two inverters.

The multilevel converter has an efficiency greater than or equal to 96% for loads greater than 10% rated power, whereas the PWM inverter did not achieve 90% efficiency until it was loaded to greater than 30% rated power. The multilevel converter had an efficiency greater than 98% for loads greater than 40% rated power, but the PWM inverter had a maximum efficiency of 95.6% which was achieved at a loading factor of 95%. The efficiency for a single multilevel inverter is greater than 99% over most of its operating range.

D. Capacitor Voltage Balance

One of the keys to using multilevel converters is balancing the voltage across the series-connected dc-bus capacitors. Capacitors will tend to overcharge or completely discharge, at which condition the multilevel converter will revert to a three-level converter unless an explicit control is devised to balance the capacitor charge. The method used to accomplish voltage balancing in this back-to-back configuration was to use proportional switching patterns for the rectifier and the inverter portions of the converter. Thus, the real power flow into a capacitor was the same as the real power flow out of the capacitor, and the net charge on the capacitor over one cycle remained the same.

If the dc capacitors start to have an unbalance in their voltage levels, a modification to the previously described control scheme can be implemented, as shown by the dashed lines in Fig. 5. By monitoring the voltages of each of the dc-link levels, minor adjustments can be made to either the inverter switching angles or the rectifier switching angles, which will transfer a net charge into or out of a particular voltage level to adjust the voltage level.

The output of the inverter was connected to a 5-hp 208-V three-phase induction motor. Three of the dc voltage levels are shown in Fig. 11 for an output frequency of 32 Hz with the

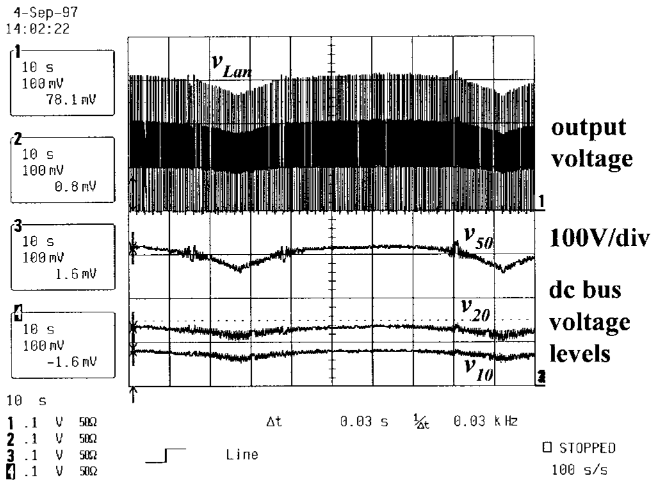


Fig. 12. Internal dc-bus voltage levels as diode-clamped converter output frequency is varied between 30–60 Hz.

converter operating without active dc-bus voltage control. The waveforms show that the overall bus voltage remains fairly constant over a cycle, and the internal bus voltages vary only slightly. The figure shows that, if the prototype multilevel converter is applied to loads with speed that does not change often or rapidly, the 6.72 mF of capacitance is sufficient for good dc-bus voltage regulation.

The inverter was controlled to deliver a continuously varying frequency between 30–60 Hz; it took approximately 35 s to change between these frequency limits. Fig. 12 shows the same waveforms as Fig. 11 but for a period of 100 s. Without active dc-bus voltage control, the overall bus voltage varied from 258 to 304 Vdc. The internal dc voltage levels varied by as much as 16 Vdc. Deceleration of the motor by regenerative braking caused the voltage to increase from its nominal value, and acceleration caused the voltage to decrease from its nominal value. The experimental results have shown that active control of the dc-bus voltage by the converter or a larger capacitance is required for the dc voltage levels if the motor speed is going to change fairly rapidly and less variation in the overall dc-bus voltage is desired.

IV. Conclusion

A multilevel cascade inverter with separate dc sources and a multilevel diode-clamped back-to-back converter have been proposed for use in large electric drives. Simulation and experimental results have shown that, with a control strategy that operates the switches at fundamental frequency, these converters have low output voltage THD and high efficiency and power factor.

In summary, the main advantages of using multilevel converters for large electric drives include the following.

1) They are suitable for large voltampere-rated and/or high-voltage motor drives.
2) These multilevel converter systems have higher efficiency because the devices can be switched at minimum frequency.
3) Power factor is close to unity for multilevel inverters used as a rectifier to convert generated ac to dc.
4) No EMI problem or common-mode voltage/current problem exists.
5) No charge unbalance problem results when the converters are in either charge mode (rectification) or drive mode (inversion).

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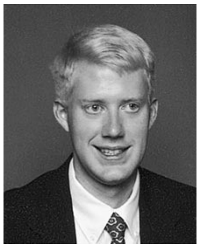

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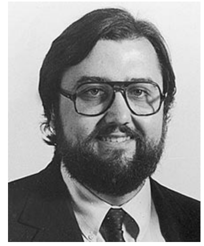

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