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MULTILEVEL INVERTER SWITCHING CONTROLLER USING A FIELD PROGRAMMABLE GATE ARRAY (FPGA)

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ABSTRACT

This paper presents the design and development of a switching controller using a field programmable gate array (FPGA) for a multilevel inverter application. SHE with PSO switching strategy was chosen and pre-calculated offline to obtain optimized switching angles for the power switches in the 5-level transistor-clamped H-bridge (TCHB) multilevel inverter. The designed switching controller produced 5-bit control signals, which connected to the power switches of the 5-level TCHB multilevel inverter. The switching controller utilized less than 1% of the total FPGA logic elements (LEs), which was equivalent to 96 out of 114,480 LEs. The execution speed of the switching controller using the FPGA chip was found to be 99.9% faster than microcontroller (PIC16F877A). Conducted simulation and measurement results verified and validated the switching controller design functionality and requirement.

Keywords: multilevel inverter, switching controller; FPGA, general purpose processor (GPP);digital signal processing (DSP); IGBT; Verilog, power consumption; selective harmonic elimination (SHE).

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1. INTRODUCTION

Over the past few years, multilevel inverters have gained significant research interest in high voltage and high-power applications due to their simple structure, modularity and transformer less circuit [1-4]. Basically, the function of multilevel inverter is to convert direct current (DC) input into alternating current (AC) output by providing a staircase of AC output waveform with low value of high frequency distortion [5-7]. Due to the limited supply voltage, the semiconductor power switches are connected to several low DC sources which are then configured into multilevel structures to achieve high power output [7-8]. With the aid of a digital controller, these power switches perform power conversion by synthesizing the multiple DC voltage sources into a high voltage stepped output waveform. Multilevel inverters are mostly employed in medium-to-high-voltage range in utility and drive applications namely high-power motor drive, power conditioning, renewable energy conversion and power distribution [7, 9-10]. The advantages of multilevel inverter over two-level inverter are enhanced output voltage quality, low switching losses, high voltage capability, reduced total harmonic distortion and reduced dv/dt stresses on semiconductor switches which indirectly reduces electromagnetic compatibility (EMC) problems [5-7, 10-12].

Several topological structures of multilevel inverters have been employed by considering some important requirements such as low number of switching device, ability to endure high voltage signals and lower switching frequency for the switching devices [1]. The three major multilevel inverter topologies that have gained much research attention are diode clamped multilevel inverter [4, 13-14] , flying capacitor multilevel inverter [15-17] and cascaded H-bridge (CHB) multilevel inverter [3, 5, 8, 11, 18-19]. Among the three topologies, cascaded H-bridge multilevel inverter is the most preferred because of its simplicity, reliability, modularity, minimum number of required components and the best fault tolerance [5, 19]. The modular structure of the H-bridge inverter enables the inverter to be cascaded and stacked up for high power and voltage application. Additionally, the cascaded H-bridge inverter still can operate at low power levels despite failure generated from other cells [8, 19]. However, the drawback of CHB inverter is it requires separate DC source for each module. Therefore, to further increase the number of stepped voltage output levels in one DC source, researchers

had proposed a new H-bridge structure by adding a bidirectional switch to the existing single phase H-bridge cell. The bidirectional switch consists of power switches, diodes and capacitors. The extended new family of multilevel inverter is known as transistor-clamped H-bridge inverter (TCHB) [8, 11, 20]. The advantage of the new TCHB over the conventional CHB is reduction in the number of DC supply and power switches for similar number of stepped output voltage. For example, a single TCHB topology (five power switches) could generate five output levels instead of three output levels when compared with a single conventional CHB topology (four power switches) [3]. Thus, minimum number of cells is required to produce the same output quality which indirectly reduces power consumption of the circuit.

The performance of power electronic converter depends on the switching strategies (modulation techniques), since it determines the efficiency of the inverter by reducing switching losses and minimizing the harmonic contents in output voltage and current. It is important to note that the harmonic contents of the AC stepped output waveform need to be reduced to prevent distortion in the power grid and to obtain maximum energy efficiency. The switching strategy can be divided into two main categories; high-frequency and low-frequency (fundamental frequency) switching strategies. For fundamental switching strategy, the power switches are switched at low fundamental frequency. This technique is desirable to minimize switching losses. Meanwhile, in high frequency switching, the harmonics are pushed into higher frequency range and will be filtered out by a filter circuit.

The biggest challenge associated with the power switching strategy is to reduce or eliminate the lower order harmonic using a simple modulation technique [21]. Numerous modulation techniques have been proposed and published by researchers to provide better performance for different applications. The three most common switching schemes are multilevel sinusoidal pulse width modulation (MSPWM), space vector modulation (SVM) and selective harmonic elimination (SHE). Among the three modulation technique, the SHE technique was found to be feasible for a multilevel inverter circuit since it allows low switching frequency, efficient DC source utilization and direct control over low harmonic orders without any filter circuit [11, 21-23]. In SHE technique, the switching angles of power switches are pre-calculated and pre-defined to eliminate or reduce low harmonic orders (3rd, 5th, 7th, 9th,

11th, 13th, 17th) that are near to the fundamental frequency. A set of transcendental equation has to be solved to selectively eliminate specific harmonic orders. The examples of algorithm used to solve the transcendental equations are Newton-Raphson, genetic algorithm (GA), particle swarm optimization (PSO) and evolutionary programming (EP) [11, 23].

Digital controllers such as microprocessor, digital signal processor (DSP), field programmable gate array (FPGA) and application specific integrated circuit (ASIC) are widely used in modern power converters applications[1-3, 5-6, 8-9, 11-12, 23-27]. Although the microprocessor and DSP have reached maturity and are widely used in power converter applications, the major problems faced by these controllers are limitation in sampling rate, low processing speed for complex computation, require huge revision for software portability/re-usability and limited number of I/O pins for large number of controlling signals [1, 12, 25, 27-28]. The software-based solutions of microprocessor and DSP execute the given tasks sequentially which consequently limit the processing speed, especially for complex computation algorithm. Additionally, limited number of processing units in the processor prevents concurrent execution of the given tasks [2, 11]. The specific programming codes for microprocessor or DSP are restricted to one particular device. Therefore, any changes to a new digital processor, demand a huge revision in the programming codes which indirectly increases the design phase duration and cost. In contrast, the digital hardware-based FPGA provides effective alternative solutions than its counterparts such as reconfigurable and reprogramming, parallel hardware execution, higher processing speed for complex computation algorithm, effortless software portability/re-usability and large number of I/O pins [1, 12, 25, 28-29]. The reconfigurable and reprogramming capability of the FPGA shorten the design phase duration and enables rapid prototyping. The usage of hardware description language (HDL), which has generic syntax features, allows the design to be independent from any particular device family. The hardware parallelism nature of the FPGA provides significance improvement on the processing speed for complex computation algorithm compared to the software-based solutions of the microprocessor and DSP [30]. The higher number of I/O pins in the FPGA device is able to satisfy the demand of increasing I/O controlling signals for the multilevel inverter application. Therefore, the implementation of switching controller in FPGA device for multilevel inverter application provides an attractive

solution for efficient hardware design and rapid prototyping.

Motivated by the advantages provided by the FPGA chip, a switching controller designed using an Altera's Cyclone IV FPGA is proposed. It is to note that the current research work is an improvement from the previous work [23], which used microcontroller (PIC16F877A) to implement the switching controller design. Details of design and development of the switching controller using the FPGA chip for multilevel inverter application are presented in this paper.

This paper is organized as follows. Section 2 provides system overview of the multilevel inverter and the internal architecture of the 5-level TCHB inverter. Section 3 explains the design methodology and implementation of the multilevel inverter and the switching controller using FPGA. The flow of the overall design methodology, the offline pre-calculated SHE switching technique, the internal design architecture, the design implementation and test measurement setup of the switching controller are explained in detail in section 3. Then, section 4 discusses the simulation results, the measurement results, the area consumption and the execution speed of the switching controller implemented in FPGA. Additionally, the performance of the execution speed and total harmonic distortion (THD) of the switching controller implemented in the FPGA was compared with the microcontroller (PIC16F877A) from the previous design work [23].

2. METHODOLOGY

2.1. System Overview of Multilevel Inverter

The overall system overview of a multilevel level inverter as depicted in Fig. 1, mainly consists of a switching controller and 5 level transistor-clamped H-bridge (TCHB) inverter. The switching controller was designed and implemented using Altera's Cyclone IV FPGA chip on the DE2-115 board. The 5-level TCHB inverter was developed using five solid state insulated-gate bipolar transistor (IGBT) switches.

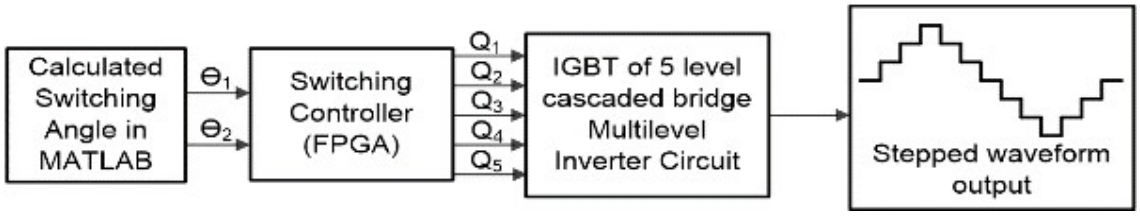


Fig.1. System overview of multilevel inverter

Selective harmonic elimination (SHE) technique was adopted to efficiently control the switching angles at each power switch in the 5-level TCHB inverter. The switching angles were pre-calculated offline using particle swarm optimization (PSO) in MATLAB software. The obtained switching angles (θ_1 and θ_2) from the PSO algorithm were first converted into switching times and were then hardcoded into the switching controller (Altera's Cyclone IV FPGA chip) to generate output control signals (Q_1-Q_5). The generated output signals were used to control the power switches in the 5-level TCHB inverter. Details on design methodology and implementation of the switching controller in FPGA are explained in the next following sections.

The 5-level TCHB inverter was constructed using five IGBT switches as depicted in Fig. 2. The supply voltage of this multilevel inverter was 12 VDC. To turn on the IGBT switches, the output signals from the switching controller (Q_1-Q_5) were first amplified to 10V by gate drivers HCPL-0302. The basic operation of 5-level TCHB inverter depends on the switching pattern of the IGBT switches to generate a full cycle of AC stepped output waveform. Table 1 lists the required switching patterns to produce the stepped sine wave output waveform of 50 Hz for the 5-level TCHB multilevel inverter.

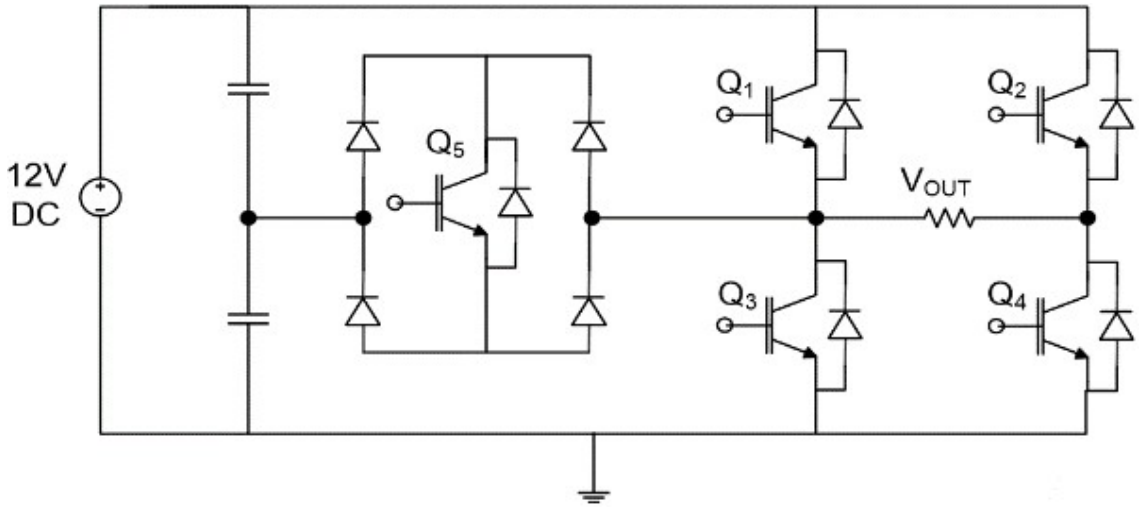


Fig.2. 5-level TCHB inverter [23]

Table 1. Switching pattern of 5-level TCHB multilevel inverter (OFF =1, ON = 0) [23]

Q5	Q4	Q3	Q2	Q1	Vout
0	1	0	0	1	+Vdc
1	1	0	0	0	+1/2Vdc
0	0	0	0	0	0
1	0	0	1	0	-1/2Vdc
0	0	1	1	0	-Vdc

2.2. Design Methodology and Implementation of Switching Controller

This section discusses the design methodology and implementation of the switching controller using the FPGA chip. Initially, the overall design flow and the conversion of pre-calculated switching angles into switching times are briefly explained and illustrated. Thereafter, the design architecture and the design implementation of the digital switching controller in the FPGA chip will be thoroughly explained in detail.

2.3.Design Flow Methodology

The overall design methodology for the implementation of switching controller in multilevel inverter application is illustrated in Fig. 3. The design process starts with finding the optimized switching angles for the 5-level TCHB inverter. The switching angles were pre-calculated offline using the SHE technique with PSO algorithm in MATLAB software. Detailed information on the SHE technique with PSO algorithm can be referred here [22]. Thereafter, the obtained switching angles were converted into switching times and the step

time durations were pre-calculated before they were hardcoded into the FPGA chip. The pre-calculated step time durations were used as references by the switching controller design to produce output signals according to the switching patterns as listed in Table 1. During the design phase of switching controller, functional simulations were conducted to ensure that the controlling output signals (Q_1-Q_5) produced accurate step time durations as had been pre-calculated according the optimized switching angles. Once the design completed and complied with the timing requirements, the design was downloaded into Altera's Cyclone IV FPGA chip on the DE2-115 board. The output signals from the FPGA board were connected to the 5-level TCHB inverter for hardware measurement. Finally, the hardware test measurement setup was conducted to measure the stepped output waveform.

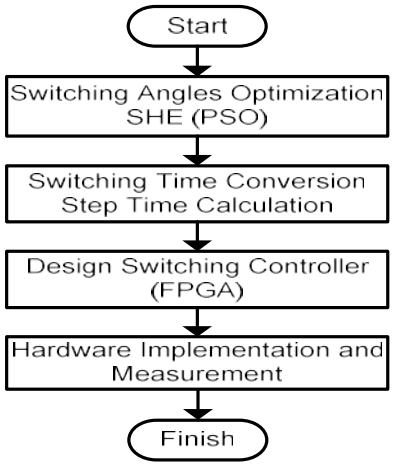


Fig.3. Design flow methodology

2.4. Switching Time Conversion and Step Time Calculation

The optimized switching angles (θ_1 and θ_2) obtained from the PSO [32-35] algorithm was first converted into switching times (T_1 and T_2). The equation for the switching time conversion is given in Equation (1). The switching angle (θ) is first divided with 180° and then multiplied with 10ms, which is the duration of half-period cycle for a 50Hz sine wave signal. The optimized switching angles (θ_1 and θ_2) and the converted switching times (T_1 and T_2) are listed in Table 2.

$$T = (\theta/180) \times 10\text{ms} \quad (1)$$

Table 2. Switching times conversion from optimized switching angles [23]

Optimized Switching Angles (θ)	Switching Times, (μs)
θ_1 =14.89	T_1 = 827
θ_2 =34.71	T_2 = 1928

Fig. 4 illustrates the locations of the switching times (T_1 and T_2) for the corresponding switching angles (θ_1 and θ_2) with respect to the full cycle of stepped sine wave output waveform. It is important to note that the 5-level stepped output waveform is a symmetrical sine wave which consists of positive and negative cycles as illustrated in Fig. 5. Therefore, the step time durations ($\mathbf{t_1}$- $\mathbf{t_4}$) are similar for both positive and negative cycles. The only difference is the direction of voltage or current (positive or negative cycle). Detail calculations for all step time durations with their corresponding stepped output levels are listed in Table 3.

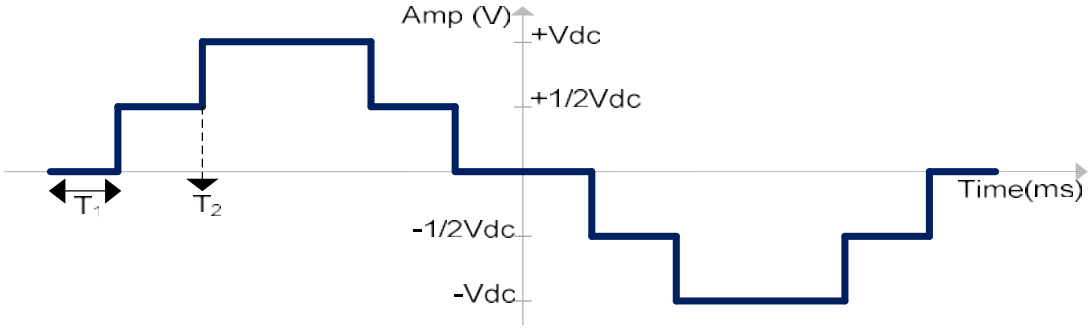


Fig.4. Location of switching times (T_1 and T_2) in the stepped sine wave output waveform

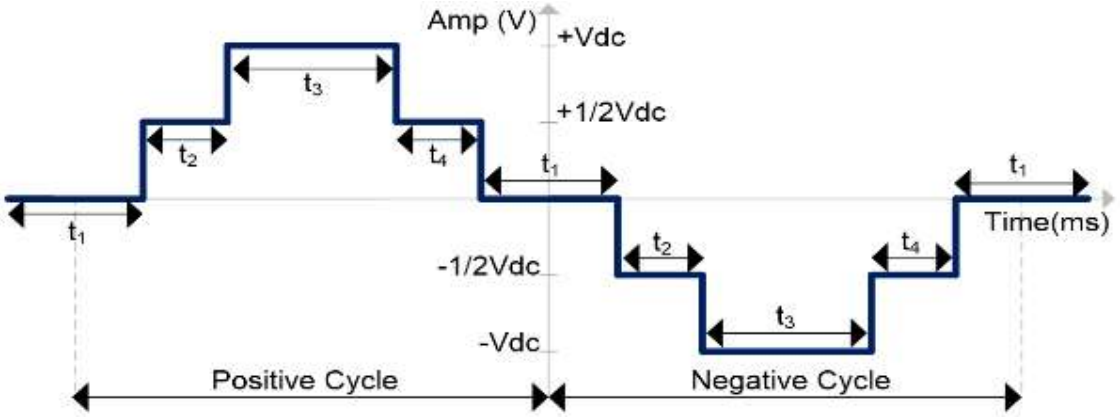


Fig.5. Label of time step delay ($\mathbf{t_1}$-$\mathbf{t_4}$) for one complete cycle

Table 3. Calculation of Time step duration

Level	Step Time, (t)	Calculation	Time, (μs)
0	t_1	$2T_1$	1654
$\pm 1/2V_{DC}$	t_2	T_2-T_1	1101
$\pm V_{DC}$	t_3	10 -2(T_2)	6144
$\pm 1/2V_{DC}$	t_4	T_2-T_1	1101

As can be observed in Table 3, the step time duration of $\mathbf{t_1}$ is twice of the converted switching time T_1. As illustrated in Fig. 5, half of the step time $\mathbf{t_1}$ duration covers the positive cycle and the other half covers the negative cycle. For step time $\mathbf{t_2}$, the duration is the difference between the converted switching times (T_2 - T_1). Similar step time duration of $\mathbf{t_2}$ is repeated for both stepped levels ($\pm 1/2V_{DC}$). The step time duration for $\mathbf{t_3}$ is obtained by subtracting the half-period cycle of 50Hz signal (10ms) with twice of the converted switching time (T_2). Similar step time duration of $\mathbf{t_3}$is repeated for both stepped levels ($\pm V_{DC}$). Lastly, the step time duration of $\mathbf{t_4}$ is similar with $\mathbf{t_2}$, thus the same formula is applied. The calculated step times are used as reference values by the switching controller to control the switching pattern duration of the IGBT switches.

2.5. Switching Controller Design Architecture and Protocol

The switching controller was designed using HDL Verilog and implemented in Altera's Cyclone IV FPGA chip on the DE2-115 board. The internal architecture of the switching controller is depicted in Fig. 6. The design architecture of the switching controller mainly consists of a clock divider, a counter and a Finite State Machine (FSM). The function of the clock divider is to provide a 1MHz clock frequency to the counter and FSM modules.

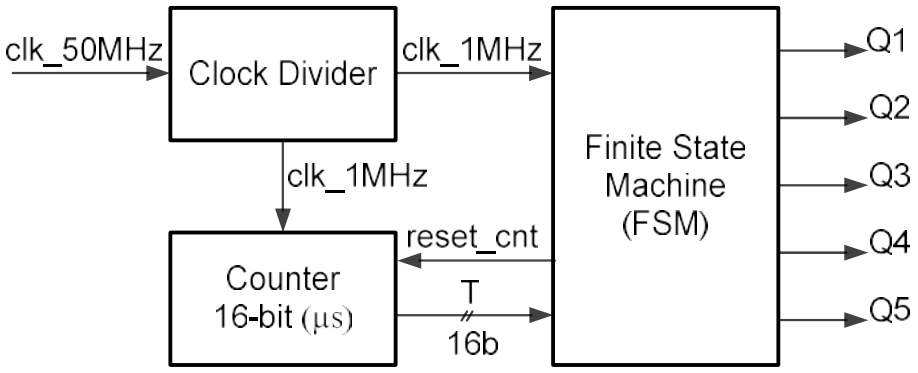


Fig.6. The internal architecture of switching controller implemented on Altera FPGA DE2-115 board

The available 50MHz system clock from the FPGA DE2-115 board is first divided and down converted into a low frequency of 1MHz clock by the clock divider module. The generated 1MHz clock (clk_1MHz) is used by the counter and FSM modules to execute the controlling operation. The clk_1MHz clock is used by the counter module for the count up process with a time resolution of 1µs. Upon power on reset, the counter module starts to count up continuously and provide a 16-bit counted output value (T) to the FSM module. The function of the FSM module is to control the step time durations ($\mathbf{t_1}$- $\mathbf{t_4}$) for a full cycle stepped output waveform generation. The 16-bit counted value (T) is used by the FSM module to compare with the referenced step time durations ($\mathbf{t_1}$- $\mathbf{t_4}$) as listed in Table 3. Once the counted value reaches the referenced step time duration, the FSM will send an internal reset signal ("reset_cnt") to the counter module to reset the counted value to "0". The FSM module provides 5 output signals (Q_1-Q_5), which are connected to the five IGBT switches.

The stepped waveform protocol of FSM module is depicted in Fig. 7. In this design, only four states (S0-S3) are required to generate a complete cycle of stepped sine wave output waveform. Therefore, only 2 bits are required to generate the four states. As illustrated in Fig. 6, the FSM uses the 16-bit counted value (T) to compare with the referenced step time durations ($\mathbf{t_1}$- $\mathbf{t_4}$) to control the movement of states.

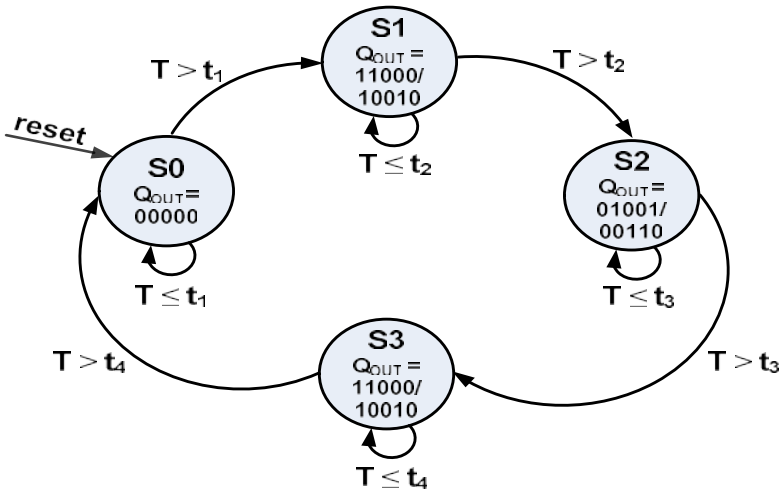


Fig.7. Finite state diagram of the FSM module

At each state, the FSM produces 5-bit Q_{OUT}, signals which represent the output signals of Q_1, Q_2, Q_3, Q_4 and Q_5. After the system is power on reset, the FSM enters state S0 and remains in that state for a step time duration of "T= $\mathbf{t_1}$(1654 μs)". When the counted value T is above t_1, the FSM moves to the next state S1 and activates "reset_cnt" signal. The "reset_cnt" will reset the counted value (T) in the Counter module and will repeat the count up process again. The FSM will remain in state S1 until the 16-b counted value T reaches step time duration of $\mathbf{t_2}$ (1101 μs). Then, the FSM moves to state S2. The process of comparing the 16-b counted value T with dedicated step time duration ($\mathbf{t_1}$- $\mathbf{t_4}$) at each state is repeated until state S3 as depicted in Fig. 7. Thus, a complete switching pattern (Q_1-Q_5) for positive stepped cycle will be generated. For negative stepped cycle, at state S3, the FSM will activate an internal polarity signal before it repeats similar consecutive states again (S0-S3).

This polarity signal is used as a reference signal by each state to produce the respective switching patterns or logic values (Q_{OUT}) accordingly. The repetition of similar consecutive state movements (S0-S3) in the FSM module resulted in continuous generation of positive and negative switching patterns at the output signals (Q_{OUT}). Thus, a continuous stepped sinusoidal waveform will be generated at the output of 5-level TCHB inverter. Table 4 tabulates the details of state movements with their respective switching output patterns (Q_{OUT}) in the FSM module. Different switching patterns are produced for positive and negative cycles.

Table 4. Finite state table of the FSM module. Cycle notation (positive = 0, negative =1)

Present State	Input(Counter, T)	Next State	Cycle	Output($Q_{out} = Q_5$-Q_1)
S0	$> t_1$	S1	0	11000
			1	10010
	$\leq t_1$	S0	0	00000
			1	00000
S1	$> t_2$	S2	0	01001
			1	00110
	$\leq t_2$	S1	0	11000
			1	10010
S2	$> t_3$	S3	0	11000
			1	10010
	$\leq t_3$	S2	0	01001
			1	00110
S3	$> t_4$	S0	0	00000
			1	00000
	$\leq t_4$	S3	0	11000
			1	10010

2.6. Switching Controller Design Implementation and Test Measurement Setup

The digital design flow of the switching controller implemented in Altera FPGA DE2-115 board is illustrated in Fig. 8. The design specification and functionality of the switching controller was first described in HDL Verilog code in the design entry of Altera Quartus II software. Once the design was completed, it was synthesized into a circuit that consists of logic elements (LEs) provided by the Altera's FPGA chip. Thereafter, a testbench, written in HDL Verilog code was used to test the switching controller functionality. The testbench provided relevant input signals to the device under test (DUT), which was the switching controller. During the functional simulation, Altera ModelSim simulator was used to observe the simulated output waveform and other the internal signals of the design.

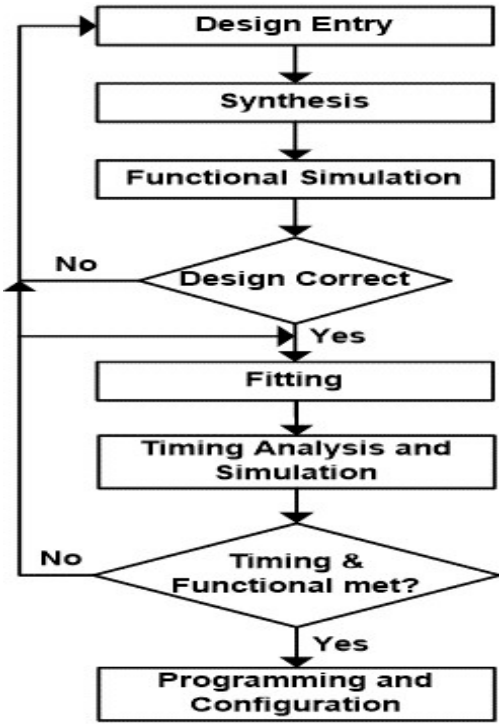


Fig.8. Digital design flow of switching controller implemented in Altera's FPGA chip

If the functionality of the switching controller design was incorrect, the written Verilog [31] code would be modified in the design entry until it complied with the design requirements. If the design passed the functional simulation, a fitting process would be conducted. In the fitting process, the LEs from the netlist were placed and routed to the actual FPGA chip. Then the timing analysis and post route simulations were conducted to verify that the design complied with the timing and functional requirements. Finally, after the design passed the timing and functional requirements, the design was implemented into the physical FPGA chip by programming and configuring the LEs switches with the required wiring connections.

After the implementation of digital hardware switching controller in the FPGA chip, a test measurement setup was constructed as depicted in Fig. 9. The output signals (Q_1-Q_5) from the switching controller FPGA board were connected with the IGBT power switches in the 5-level TCHB inverter circuit. The stepped sine wave output waveform was observed in the oscilloscope. The actual test measurement setup is shown in Fig. 10. The type of components used in the 5-level TCHB inverter circuit is listed in Table 5.

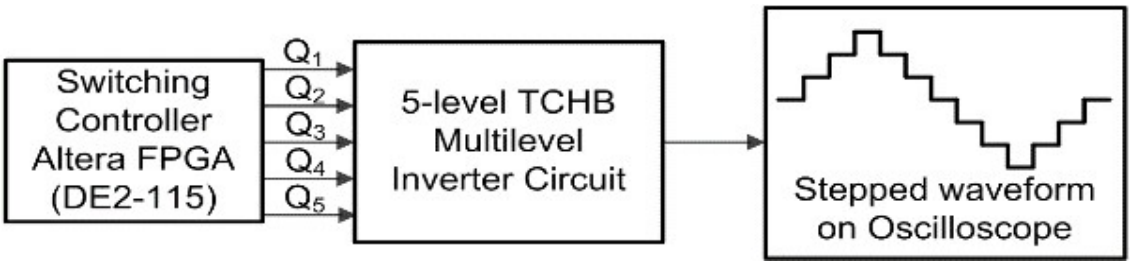


Fig.9. Test measurement setup for 5-level TCHB multilevel inverter

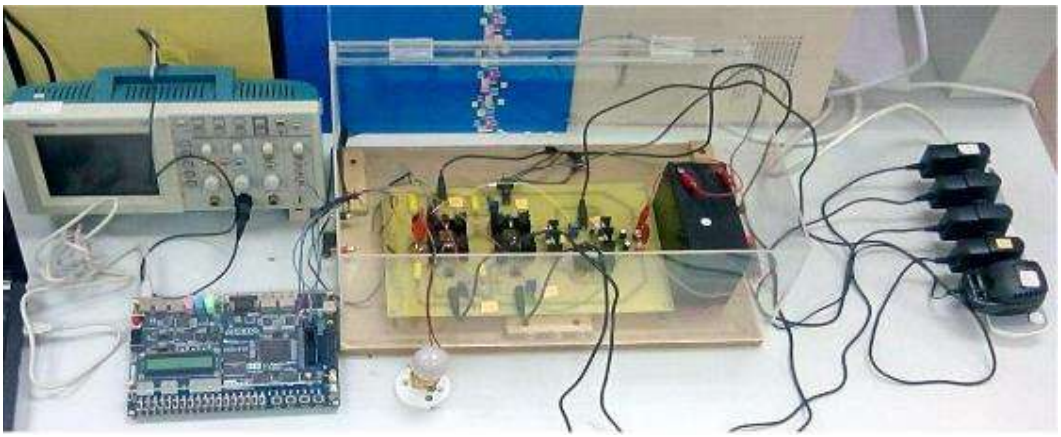


Fig.10. Actual test measurement setup for 5-level TCHB multilevel inverter

Table 5. Type of components in 5-level TCHB inverter circuit

Type of Components	Component Code	Quantity
Power switches (IGBT)	IKP1ON60T, $V_{CE(sat)}$ = 1.5V	5
Capacitor (C1, C2)	100 µF, 100V	2
Diodes (D1, D2, D3,D4)	DSEI 12-0.6A	4
RC Snubber	R = 10 Ω, 0.001 µF,1000V	5
Gate Drivers	HCPL-3020, Optocoupler	5

3. RESULTS AND DISCUSSION

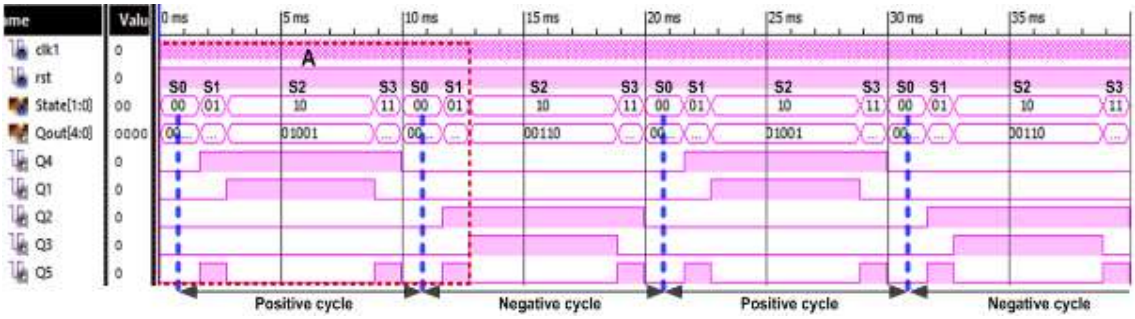
This section discusses the simulation results, the measured results of control output signals from the FPGA board, the stepped output waveform from the 5-level TCHB inverter, the THD of the output waveform and the execution speed comparison between FPGA and PIC controller.

3.1. Simulation Results

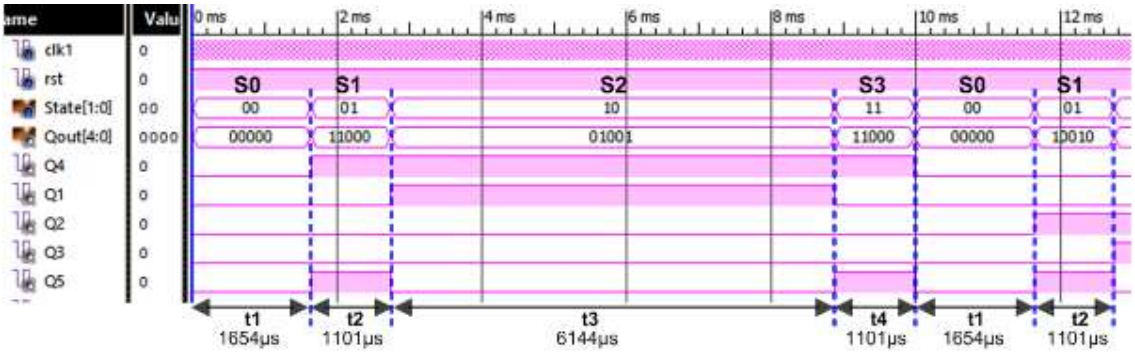
Fig. 11(a) depicts the overall switching controller output signals for positive and negative cycles. In this simulation results, the output signals (Q_5-Q_1) are arranged accordingly to

indicate the switching pattern and duration for each cycle. The 2-bit states (S0-S3) activate certain output signals (Q_5-Q_1) to realize the stepped output waveform generation. As can be seen in Fig. 11(a), initially, output signals Q_4, Q_1 and Q_5 are activated by FSM states (S0-S3) at certain timing duration for the positive cycle of stepped waveform. Thereafter, output signals Q_2, Q_3 and Q_5 are activated at certain timing duration for the negative cycle of stepped waveform. These positive and negative switching patterns are repeatedly generated to produce a continuous stepped sine wave output waveform.

The zoom view into marked area A is depicted in Fig. 11(b). In this simulation result, we can observe that each state has certain timing duration which directly controls the output signals (Q_5-Q_1) duration. The simulated step time duration for each state is observed to comply with the pre-calculated step time durations ($\mathbf{t_1}$- $\mathbf{t_4}$) as listed in Table 3. The output signals (Q_5-Q_1) are activated at certain timing duration to generate the 5-level stepped output waveform. The simulation results validate the functionality of the designed switching controller according to the design requirements.



(a) Output signal Q_{OUT} (Q_5-Q_1) patterns from the switching controller



(b) Zoom view into marked area A. Step time durations ($\mathbf{t_1}$– $\mathbf{t_4}$) generated from each state (S0-S3)

Fig.11. Simulation results of switching controller using Altera ModelSim simulator

3.2. Measurement Results

Fig. 12 depicts the output signals (Q_5-Q_1) measured from the switching controller implemented in the FPGA DE2-115 board. These output signals are arranged according to their cycle's activation. Output signals Q_4, Q1and Q_5 are activated for the positive stepped cycle while output signals Q_2, Q_3 and Q_5 are activated for the negative stepped cycle. The switching patterns of output signals from the measurement results are observed to be similar to that of the simulation results.

Fig. 13(a) depicts the measured stepped sine wave output waveform from the 5-level TCHB output load (V_{OUT}), as indicated in Fig. 2. The stepped sine wave output waveform with frequency 50Hz and $12V_{PP}$ is continuously generated from the 5-level TCHB output load (V_{OUT}). The positive and negative half-cycle of stepped output waveforms are depicted in Fig. 13(b) respectively. Five levels of stepped output waveform are generated accordingly ($+V_{DC}$, $+1/2\ V_{DC}$, 0, $-1/2V_{DC}$, $+V_{DC}$). The measured time step durations ($\mathbf{t_1}$-$\mathbf{t_4}$) for the stepped output waveform are according to the pre-calculated value listed in Table 3.

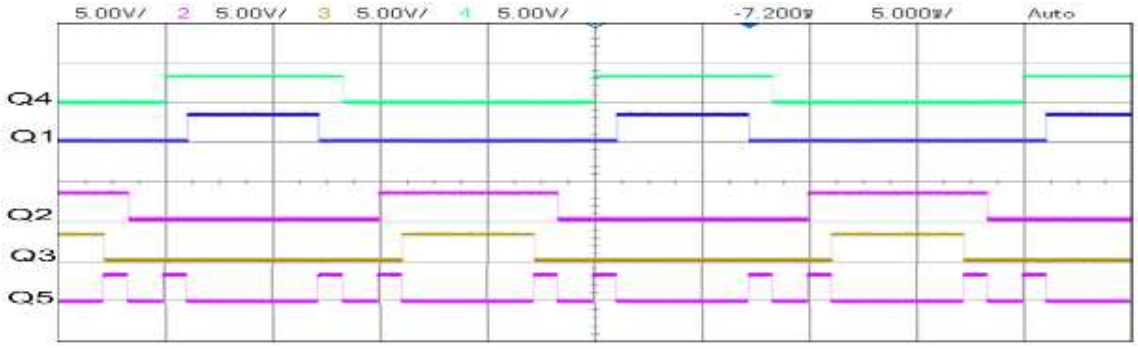
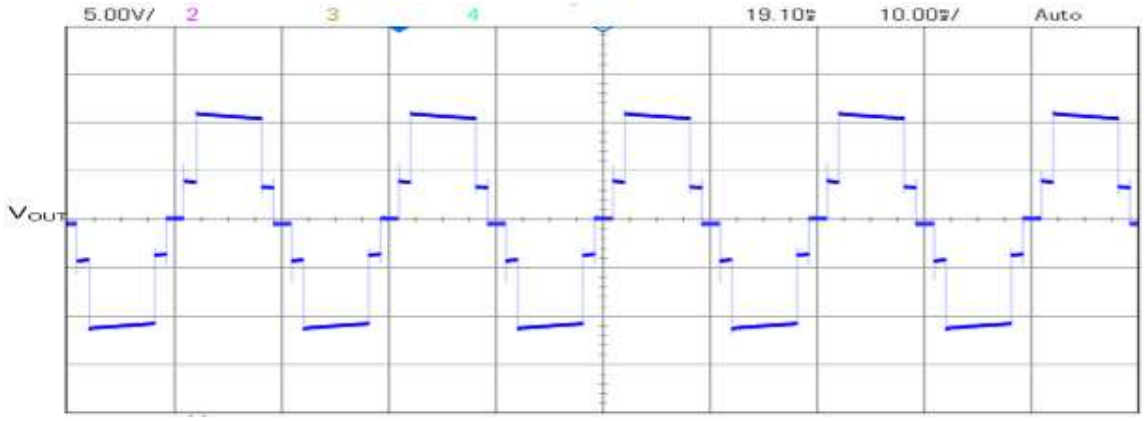
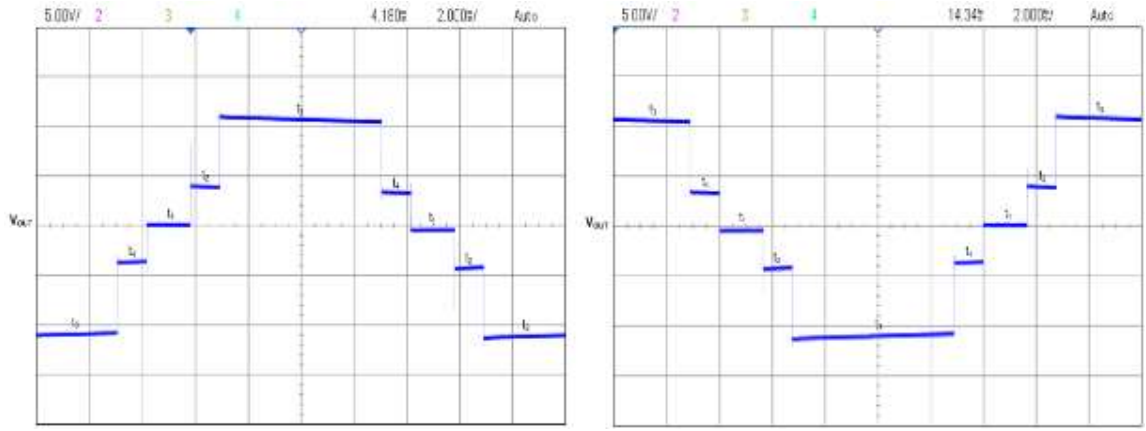


Fig.12. Measured output control signals from the FPGA switching controller



(a) Continuous stepped sine wave output voltage (V_{OUT}) waveform



(b) Positive and negative half-cycle of stepped output waveform

Fig.13. Measured stepped output voltage waveform from 5-level TCHB inverter

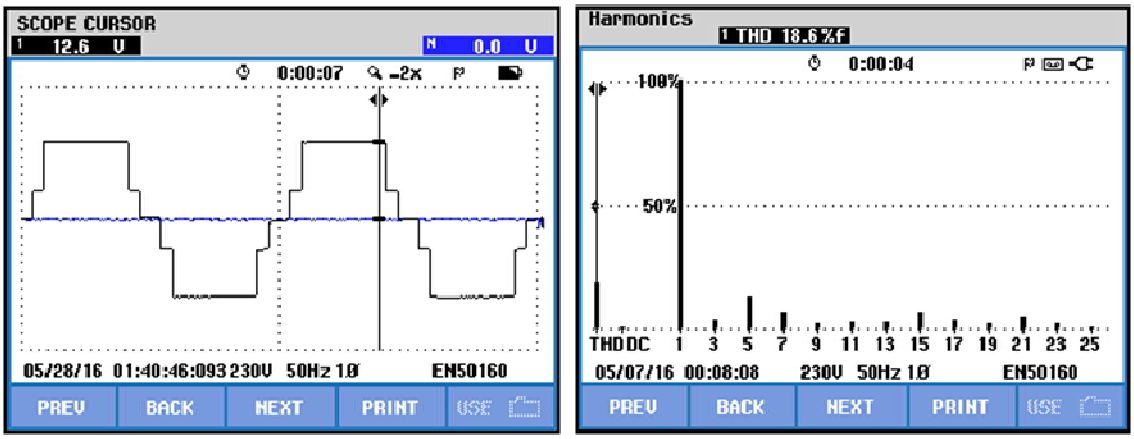


Fig.14. Measured stepped output waveform and THD from FPGA (Altera Cyclone IV) using power quality analyzer

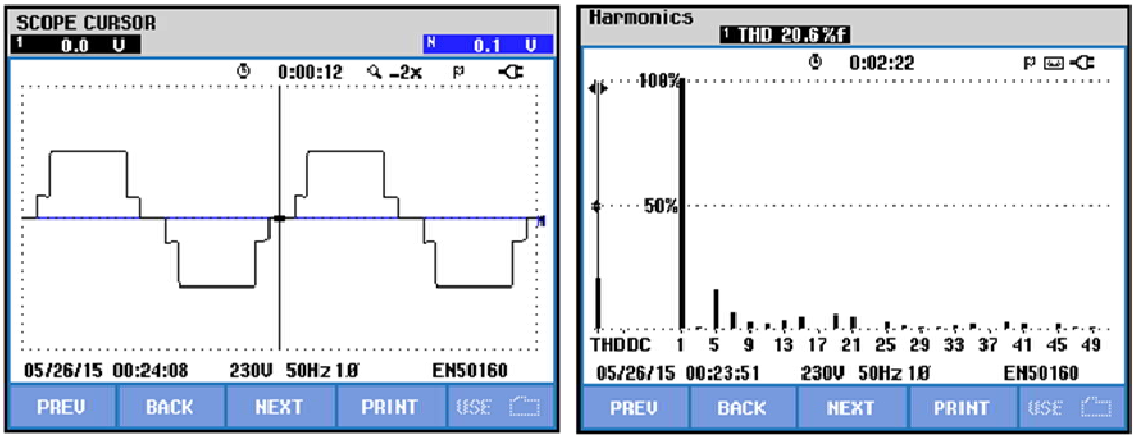


Fig.15. Measured stepped output waveform and THD from microcontroller (PIC16F877A) using power quality analyzer

Therefore, the simulation and measurement results validate the design functionality of the switching controller implemented in the FPGA DE2-115 board.

The stepped output waveforms were also measured using power quality analyzer (Fluke 435) instrument for total harmonic distortion (THD) measurement. Fig. 14 depicts the measurement results of the stepped output waveform with a voltage THD value of 18.6% for the switching controller implemented in Altera's FPGA chip. For comparison purposes, the previous measurement results of the switching controller implemented in microcontroller (PIC16F877A) are also shown here as depicted in Fig. 15. The voltage THD value of the switching controller implemented in microcontroller was 20.6%. From the shown THD results, it is observed that the voltage THD reading of the switching controller implemented in FPGA shows slight improvement than the microcontroller (PIC16F877A).

3.3. FPGA Implementation Result

This section discusses the FPGA utilization and the execution speed of the designed switching controller. Table 6 lists the FPGA chip utilization. The total number of logic elements (LEs) and combinational function used in the design was 96, the total number of register was 54 and the total pin was 7. From the obtained results, the overall utilization of the FPGA chip was less than 1% which is equivalent to 96 out of 114,480 LEs.

Table 6. FPGA (Altera Cyclone IV) utilization

Item	Utilization
Total logic elements	96/114,480 (< 1%)
Total Combinational Function	96/114,480 (< 1%)
Total register	54/114,480 (< 1%)
Total Pin	7/529 (1%)

From the timing analyzer in Quartus II software, the maximum clock speed for this design was 136.52MHz. Therefore, to calculate the execution speed of the designed switching controller in producing the stepped sinusoidal waveform is by considering the number of states that the FSM has to repeat. In this design, the 4 states (S0-S3) need to be repeated twice to produce a single stepped sinusoidal waveform. Thus, 8 states are required to produce a single stepped sinusoidal waveform. The execution speed for this design in FPGA chip can be calculated as shown in Equation (2).

$8 \text{ states x } 1/136.52\text{MHz} = 0.0586\mu\text{s}$ (2)

The execution speed from this FPGA is further compared with microcontroller PIC16F877A which was used from previous research work by [22]. The execution speed for a microcontroller depends on the number machine cycles and the oscillator frequency used. The number of machine cycles can be obtained by calculating the total number of instructions or machine codes required in the design. Then, the total number of machine cycles is multiplied with the machine clock period. Therefore, for the previous switching controller design, the high-level of C language code was first converted into machine codes and machine cycles. It is to note that each machine code may require a few machine cycles to complete the task. Table 7 lists the detail information of the microcontroller (PIC16F877A) clock frequency (F_{OSC}) and the total number of machine cycles required from the previous design.

Table 7. PIC16F877A clock frequency and total number of machine cycles

Item	
PIC16F877A Clock Frequency (F_{OSC})	4MHz
Total number of machine cycle	238 cycles

The period of a machine cycle is calculated by taking the reciprocal of clock frequency (F_{osc}) divided by four as indicated in Equation (3).

$$\text{Period of a machine cycle} = 1 / ((F_{OSC}) / 4)) \quad (3)$$

The total execution time can be calculated by multiplying the total number of machine cycles (mch.cycles) with the period of each machine cycle as shown in Equation (4)

$$\text{Execution time} = \text{No. of mch. cycles} \times \text{Period of a mch. cycle} \quad (4)$$

By referring to information of clock frequency (F_{osc}) in Table 7 and equation (3), the period for a machine cycle (mch.cycle) is 1µs as indicated in Equation (5).

$$\text{Period of the mch. cycle} = 1 / ((4\text{MHz}) / 4) = 1\mu\text{s} \quad (5)$$

Hence, the total execution time for the Switching Controller implemented in microcontroller (PIC16F877A) is 238µs as calculated in Equation (6).

$$\text{Execution time} = 238 \text{ cycles x } 1\mu\text{s} = 238\mu\text{s} \quad (6)$$

The execution times of the Switching Controller implemented in FPGA (Altera Cyclone VI) and microcontroller (PIC16F877A) are tabulated in Table 8. From the results, it is obviously

seen that the Switching Controller implemented in FPGA has a significantly low execution time compared to microcontroller (PIC16F877A). Thus, the execution speed of the Switching Controller implemented in FPGA is 99.9% faster compared to the microcontroller (PIC16F877A).

Table 8. Execution speeds of switching controller implemented in FPGA and microcontroller

Switching Controller	Execution Time (s)
FPGA (Altera Cyclone IV)	0.0586μs
Microcontroller (PIC16F877A)	238μs

4. CONCLUSION

The design and development of a switching controller using Altera's Cyclone IV FPGA chip for the 5-level TCHB multilevel inverter has been thoroughly expounded. The switching controller was designed to synthesize AC signal from DC source by controlling the switching pattern of the 5-level TCHB inverter. Detailed internal design architecture, switching pattern protocol and design implementation flow have also been illustrated and elucidated. The utilization of logic elements (LEs) in the FPGA chip was found to be less than 1%, in which only 96 out of 114,480 LEs were used by the designed switching controller. In addition the execution speed of the designed switching controller using the FPGA chip was found to be 99.9% faster than the microcontroller (PIC16F877A) [41-42]. Thus, the switching controller designed in FPGA chip was found to be far more superior to the microcontroller [39-40]. Additionally, the FPGA chip provides a promising solution for the multilevel inverter application that requires a complex switching algorithm embedded into the controller and for the application that requires a large number of controlling signals as the number of power [36-38] switches increases. The shown simulation and measurement results for the control output signals, the stepped sine wave output waveform, the THD reading of 18.6% validate the switching controller design functionality and requirement.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

[1]Ahmad A, Gupta R. Digital PWM of cascaded multilevel voltage source inverter using FPGA. In IEEE Students Conference on Engineering and Systems, 2013, pp. 1-5

[2] Azli N A, Teng L Y, Lim P Y. Implementation of a single-carrier multilevel PWM technique using field programmable gate array (FPGA). In 7th IEEE International Conference on Power Electronics and Drive Systems, 2007, pp. 836-841

[3] Elias M F, Rahim N A, Ping H W, Uddin M N. Asymmetrical cascaded multilevel inverter based on transistor-clamped H-bridge power cell. IEEE Transactions on Industry Applications, 2014, 50(6):4281-4288

[4] Gao C, Jiang X, Li Y, Chen Z, Liu J. A DC-link voltage self-balance method for a diode-clamped modular multilevel converter with minimum number of voltage sensors. IEEE Transactions on Power Electronics, 2013, 28(5):2125-2139

[5] Gautam S, Gupta R. Switching frequency derivation for the cascaded multilevel inverter operating in current control mode using multiband hysteresis modulation. IEEE Transactions on Power Electronics, 2014, 29(3):1480-1489

[6] Gautam S, Kundu S, Basu P, Gupta R. FPGA implementation of generalized modulation for hybrid multilevel inverter with fixed ratio DC link voltage. In IEEE International Conference on Power Electronics, Drives and Energy Systems, 2012, pp. 1-5

[7] Adithya S N. Study of multilevel sinusoidal PWM methods for cascaded h-bridge multilevel inverters. In IEEE 2nd International Conference on Electrical Energy Systems, 2014, pp. 249-254

[8] Rahim N A, Elias M F, Hew W P. Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing. IEEE Transactions on Industrial Electronics, 2013, 60(8):2943-2956

[9] Reddy V N, Rao S N, Babu C S. Emphasis of modulated techniques for cascaded multilevel inverters fed drive using FPGA. In IEEE International Conference on Power, Energy and Control, 2013, pp. 686-692

[10]Edpuganti A, Rathore A K. Fundamental switching frequency optimal pulsewidth modulation of medium-voltage cascaded seven-level inverter. IEEE Transactions on Industry Applications, 2015, 51(4):3485-3492

[11]Halim W A, Rahim N A, Azri M. Selective harmonic elimination for a single-phase 13-level TCHB based cascaded multilevel inverter using FPGA. Journal of Power Electronics, 2014, 14(3):488-498

[12]Sanchez P M, Machado O, Peña E J, Rodríguez F J, Meca F J. FPGA-based implementation of a predictive current controller for power converters. IEEE Transactions on Industrial Informatics, 2013, 9(3):1312-1321

[13]Shu Z, Ding N, Chen J, Zhu H, He X. Multilevel SVPWM with DC-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM. IEEE Transactions on Industrial Electronics, 2013, 60(5):1884-1896

[14]Hosseini S H, Sadeghi M. Reduced diode clamped multilevel converter with a modified control method. In IEEE 7th International Conference on Electrical and Electronics Engineering, 2011, pp. I-302

[15]Khazraei M, Sepahvand H, Corzine K A, Ferdowsi M. Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters. IEEE Transactions on Industrial Electronics, 2012, 59(2):769-778

[16]Teixeira C A, Holmes D G, McGrath B P. Single-phase semi-bridge five-level flying-capacitor rectifier. IEEE Transactions on Industry Applications, 2013, 49(5):2158-2166

[17]Ibrayeva A, Ten V, Familiant Y L, Ruderman A. PWM strategy for improved natural balancing of a four-level H-bridge flying capacitor converter. In IEEE International Aegean Conference on Electrical Machines and Power Electronics, International Conference on Optimization of Electrical and Electronic Equipment andInternational Symposium on Advanced Electromechanical Motion Systems, 2015, 311-316

[18]Sarkar I, Fernandes B G. High resolution m-cell symmetric cascaded H-bridge multilevel inverter with one transistor clamped H-bridge per phase. In 41st Annual Conference of the IEEE Industrial Electronics Society, 2015, pp. 1-6

[19]Coppola M, Di Napoli F, Guerriero P, Iannuzzi D, Daliento S, Del Pizzo A. An FPGA-based advanced control strategy of a gridtied PV CHB inverter. IEEE Transactions on Power Electronics, 2016, 31(1):806-816

[20]Schweizer M, Friedli T, Kolar J W. Comparative evaluation of advanced three-phase

three-level inverter/converter topologies against two-level systems. IEEE Transactions on Industrial Electronics, 2013, 60(12):5515-5527

[21]Gobinath K, Mahendran S, Gnanambal I. Novel cascaded H-bridge multilevel inverter with harmonics elimination. In IEEE International Conference on Green High Performance Computing, 2013, pp. 1-7

[22]Ibrahim I R, Omar A M, Hussain Z. Control strategy of power converter system in the dual-power PV-grid system energy utilizing cascaded multilevel inverter. In 8th IEEE Conference on Industrial Electronics and Applications, 2013, pp. 848-853

[23] Ibrahim M A A R I R, Omar A M. A new adaptive selective harmonic elimination technique for 5-level cascaded H-bridge multilevel inverter. In International Conference on Advance Mechanic, Power and Energy, 2015, pp. 1-5

[24]Juárez-Abad J A, Linares-Flores J, Guzmán-Ramírez E, Sira-Ramirez H. Generalized proportional integral tracking controller for a single-phase multilevel cascade inverter: An FPGA implementation. IEEE Transactions on Industrial Informatics, 2014, 10(1):256-266

[25]Ahmad M I, Husin Z, Ahmad R B, Rahim H A, Hassan M A, Isa M M. FPGA based control IC for multilevel inverter. In IEEE International Conference on Computer and Communication Engineering, 2008, pp. 319-322

[26]Lima E F, Pereira Filho N, Pinto J O. FPGA realization of multilevel space vector PWM using non-orthogonal moving reference frame. In IEEE Brazilian Power Electronics Conference, 2009, pp. 151-158

[27]Karuppanan P, Mahapatra K K. FPGA based cascaded multilevel pulse width modulation for single phase inverter. In 9th IEEE International Conference on Environment and Electrical Engineering, 2010, pp. 273-276

[28]e Silva R N, Barreto L H, Barbosa A U, Joca D R, Praça P P. Digital implementation of a modulation technique for a multilevel inverter on FPGA. In 10th IEEE/IAS International Conference on Industry Applications, 2012, pp. 1-6

[29]Jawahar M R, Kumar V A, Moorthi S, Selvan M P. FPGA based SHEPWM switching scheme for single phase cascaded H-bridge multi-level inverter. In IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems, 2016, pp. 1-6

[30] Schaefer M, Goetze W, Hofmann M, Bayer F, Montesinos-Miracle D, Ackva A. Direct

current control for grid-connected diode-clamped inverters. IEEE Transactions on Industrial Electronics, 2017, 64(4):3067-3074

[31] Yeap K H, Nisar H, Chong K H, Rizman Z I, Yang C C, Yong Y T, Lai K C. Design of a keyless coded home lock system using Verilog hardware description language. International Journal of Electronics, Computer and Communications Technologies, 2012, 3(1):10-16

[32] Indera N I, Yassin I M, Zabidi A, Rizman Z I. Non-linear autoregressive with exogeneous input (NARX) Bitcoin price prediction model using PSO-optimized parameters and moving average technical indicators. Journal of Fundamental and Applied Sciences, 2017, 9(3S):791-808

[33] Zabidi A, Yassin I M, Tahir N M, Rizman Z I, Karbasi M. Comparison between binary particles swarm optimization (BPSO) and binary artificial bee colony (BABC) for nonlinear autoregressive model structure selection of chaotic data. Journal of Fundamental and Applied Sciences, 2017, 9(3S):730-754

[34] Masrom S, Abidin S Z, Omar N, Rahman A S, Rizman Z I. Dynamic parameterizations of particle swarm optimization and genetic algorithm for facility layout problem. ARPN Journal of Engineering and Applied Sciences, 2017, 12(10):3195-3201

[35] Yassin I M, Zabidi A, Ali M S, Tahir N M, Hassan H A, Abidin H Z, Rizman Z I. Binary particle swarm optimization structure selection of nonlinear autoregressive moving average with exogenous inputs (NARMAX) model of a flexible robot arm. International Journal on Advanced Science, Engineering and Information Technology, 2016, 6(5):630-637

[36] Zaman F H, Shukur N A, Hamzah N, Zaini N M, Rizman Z I. Performance of modified power spectral density features in EEG signal classification. Journal of Fundamental and Applied Sciences, 2017, 9(3S):830-843

[37] Hussain M M, Zakaria Z, Rizman Z I, Yasin M A. Power loss estimation due to difference transformer tap changer position at interface. Journal of Fundamental and Applied Sciences, 2017, 9(3S):685-696

[38] Dahalan W M, Othman A G, Zoolfakar M R, Khalid P Z, Rizman Z I. Optimum DNR and DG sizing for power loss reduction using improved meta-heuristic methods.ARPN Journal of Engineering and Applied Sciences, 2016, 11(20):11925-11929

[39] Abdullah R, Rizman Z I, Dzulkefli N N, Ismail S, Shafie R, Jusoh M H. Design an

automatic temperature control system for smart tudung saji using Arduino microcontroller. ARPN Journal of Engineering and Applied Sciences, 2016, 11(16):9578-9581

[40] Nawi B, Sulaini B, Mohd Z A, Shamsul A Z, Zairi I R. PID voltage control for DC motor using MATLAB Simulink and Arduino microcontroller. Journal of Applied Environmental and Biological Sciences, 2015, 5(9):166-173

[41] Dzulkefli N N, Abdullah R, Jaafar A N, Shafie R, Yassin I M, Rizman Z I, Abidin H Z. Design an automatic temperature control system based on PIC controller for smart ventilation fan. Journal of Fundamental and Applied Sciences, 2017, 9(3S):779-790

[42] Rizman Z I, Yeap K H, Ismail N, Mohamad N, Husin N H. Design an automatic temperature control system for smart electric fan using PIC. International Journal of Science and Research, 2013, 2(9):1-4

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