MULTILEVEL INVERTER WITH LEVEL SHIFTING SPWM TECHNIQUE USING FEWER NUMBER OF SWITCHES FOR SOLAR APPLICATIONS

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Abstract

A multilevel inverter (MLI) is a popular inverter for solar based high power applications. The drawback of conventional H-bridge inverter is non-sinusoidal output voltage, which reduces the output quality of inverter. Later, the drawback of conventional H-bridge was overcome by conventional MLI. But, conventional MLI needs maximum number of diodes and switches. In order to overcome this drawback proposed MLI topology with level shifting sinusoidal pulse width modulation (SPWM) technique can be employed. Proposed MLI contain fewer number of switches and diodes, which helps in optimizing the circuit layout, reducing gate driver circuit for those switches. SPWM technique uses multicarrier waveforms with level shifting ensuring the reduction in total harmonics distortion (THD). In this Paper level shifting SPWM technique has been incorporated in which 5 kHz carrier wave is compare with 50Hz of sinusoidal wave with a modulation index of 0.8. THD of proposed 9-level inverter is 17.27% without filter and 4.29% with LC filter. Simulation of proposed inverter is carried out in MATLAB/SIMULINK.

Key Words: *Solar, 9-level inverter, Level shifting SPWM, Power diodes and switches, Total Harmonics Distortion (THD)*

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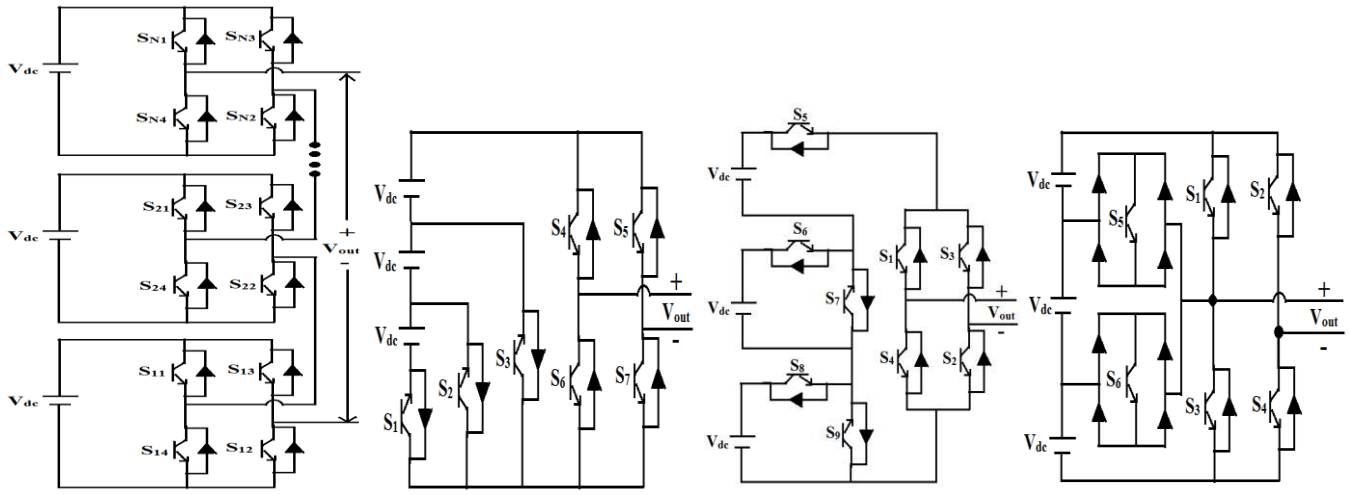
1. INTRODUCTION

Renewable energy sources have gained wide importance due to the depletion of fossil fuels. Also the problem of pollution caused by fossil fuels can be solved by using clean and freely available renewable energy. Solar energy is one of the renewable energy in which most of the researchers are showing interests as it can be responsible for green energy concept.

In case of solar energy system, voltage generated from solar array is needed to be converted into ac signal for high power AC application. Conventional H-bridge inverter is not a practical solution for DC-AC conversion because of large harmonics distortion and switching losses. Later, the drawbacks of conventional inverter are overcome by multilevel inverter (MLI) [1]-[2]. The increased number of level reduces the harmonic content and brings the output voltage waveform closer to sinusoidal. Conventional MLI include diode clamped, flying capacitors and cascaded H-bridge. In diode clamped MLI, diodes are used in majority and number of diode increases with increase in levels. In flying capacitor MLI, number of capacitor is increases with increase in levels. In cascaded MLI, as the cascade stage increases, certainly the number of switches and sources also increases [3]-[6]. In Fig.1 (a), cascaded MLI for N-stages is shown. But, these conventional MLI's requires large number of power devices to generate maximum number of levels. Further, this drawback is overcome by modifying the conventional MLI's circuits. Diode clamped MLI has been discussed with lesser number of diodes in [7]. Modified flying capacitor topology is discussed in [8]. In [9], cascade MLI topology with reduced number of switches is discussed. In [10]-[12], 7-level inverter using 7 switches and 9 switches has been discussed. In Fig.1 (b) and Fig.1 (c), 7-level with 9-switches and 7-level with 7-switches are shown respectively. In [13], 7-level with 6-switches MLI is explained. In Fig.1 (d), the schematic of 7-level with 6-switches MLI is shown. In [13], though the number of switches is less; but the number of diodes increases with number of levels. The above discussed MLI's gives more number of levels as compared to conventional MLI using minimum number of switches. In the above topology, the emphasis is on minimizing the number of switches but it still requires large number of voltage sources. This drawback is overcome by advanced MLI [14] and asymmetrical MLI. Single phase MLI with single PV source and less number of switches is proposed in [15]. The drawback of advance MLI is that it requires inductor and a switch operating at high frequency. The cost and design complexity of advance MLI is increased due to the use of inductor.

Generally, asymmetrical multilevel inverters are used to increase the number of levels. In [16], 25-level asymmetrical inverter with 12 switches for renewable power grid applications is proposed. In [17], 25-level asymmetrical inverter with 10 switches for solar application is proposed. In [18], modified cascaded H-bridge inverter is proposed with three different algorithms to generate 9, 13 and 17 levels. It is observed that THD for 9-level, 13-level and 17-level inverter without filter is 17.22%, 10.74% and 7.76% respectively. Also the THD for 9-level, 13-level and 17-level inverter with filter is 5.86%, 5.18% and 4.71% respectively.



(a) Conventional Cascaded MLI (b) 7-level with 7-switches (c) 7-level with 9-switches (d) 7-level with 6-switches

Fig.1 (a)-(d) Existing multilevel Inverter

Asymmetric multilevel inverter is more advantageous than symmetric multilevel inverter in obtaining more number of output levels using same number of voltage sources. But the main drawback of asymmetrical inverter is that it increases the complexity of gate triggering pulses. The other drawback is that the required rating of the power devices is not same. Due to complexity of gate triggering pulses asymmetrical MLI's are not beneficial to use. The proposed MLI requires fewer number of power devices and nearly removes all major above discussed drawbacks. In this paper, a novel 9-level MLI with 7-switches is proposed. The SPWM technique is used to reduce the THD and improve the quality of output voltage.

2. PROPOSED TOPOLOGY

The proposed MLI is designed for 9-level using 7 switches as shown below in Fig. 2. This topology is modification of conventional H-bridge inverter where number of levels can be increased by stacking specific combination of diode, switch and voltage source. Switches S_1, S_5, S_6 and S_7 represent H-bridge in which S_1, S_5 are used for generating negative voltage levels whereas S_6, S_7 are used for positive voltage levels. In addition switches S_2, S_3 and S_4 are used to increase the number of levels. The proposed scheme 9-level inverter requires 7-switches, 3-diodes and 4-voltage sources. Fig. 3 shows circuit diagram of N-level proposed MLI.

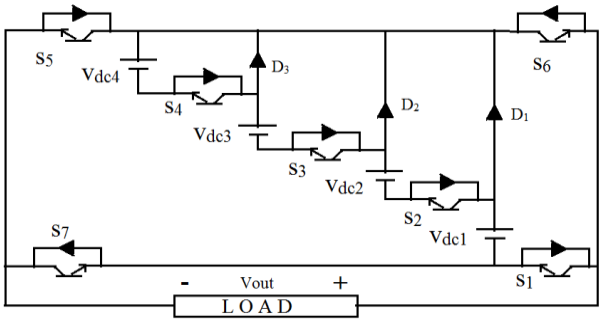


Fig.2 Circuit diagram of proposed 9- level inverter.

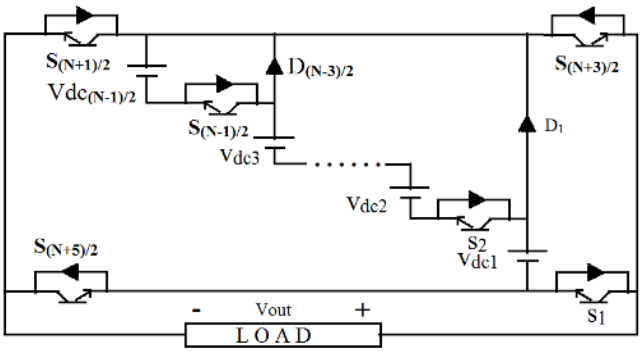


Fig.3 N-level proposed MLI.

The relationship between number of output levels, switches, diodes and voltage sources is stated in TABLE-I. It can be depicted that this topology is suitable only for odd number of output levels. (N+5)/2 switches with anti-parallel diodes, (N-3)/2 clamping diodes and (N-1)/2 sources are needed to design N-Level proposed inverter.

Table-I Relationship between number of output levels, switches, diodes and voltage sources

No. of levels	No. of switches	No. of clamping diodes	No. of sources
3	4	0	1
5	5	1	2
7	6	2	3
9	7	3	4
N	(N+5)/2	(N-3)/2	(N-1)/2

3. OPERATION OF PROPOSED TOPOLOGY

The operation for 9-level MLI with 7-switches as shown in Fig. 2 is discussed below. Switches S_1 and S_5, S_6 and S_7 are complementary to each other. S_1, S_5 are turned 'ON' to generate negative output levels and S_6, S_7 are turned 'ON' to generate positive output levels. The switches S_2, S_3 and S_4

are turned 'ON' and turned 'OFF' accordingly to increase the number of output levels.

Table-II Switching states with corresponding voltage levels

Voltage Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7
$Vdc_4+Vdc_3+Vdc_2+Vdc_1$	0	1	1	1	0	1	1
$Vdc_3+Vdc_2+Vdc_1$	0	1	1	0	0	1	1
Vdc_2+Vdc_1	0	1	0	0	0	1	1
Vdc_1	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0
$-Vdc_1$	1	0	0	0	1	0	0
$-Vdc_2-Vdc_1$	1	1	0	0	1	0	0
$-Vdc_3-Vdc_2-Vdc_1$	1	1	1	0	1	0	0
$-Vdc_4-Vdc_3-Vdc_2-Vdc_1$	1	1	1	1	1	0	0

Switches S2, S3, and S4 are turned 'ON' when maximum positive and negative output level is required and are turned 'OFF' with corresponding levels as shown in TABLE-II. The current flow direction through the circuit for positive and negative voltage levels is shown in Fig.4 (a)-(d) and Fig.5 (a)-(d) respectively.

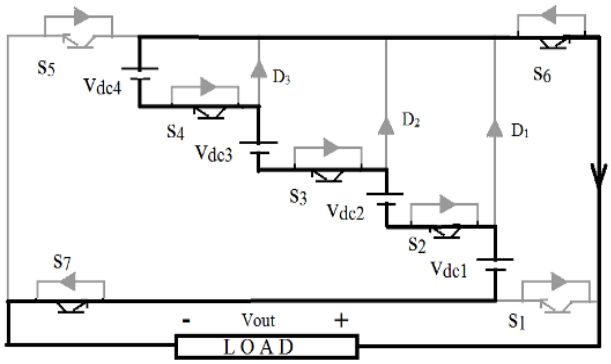
3. SPWM TECHNIQUE FOR PROPOSED TOPOLOGY

Sinusoidal pulse width modulation (SPWM) technique is used for pulse generation where reference wave is sinusoidal and carrier wave is high frequency triangular wave. The comparison of both these waves gives rise to the pulses to trigger the switches. Level shifting SPWM technique is employed in order to reduce THD. Multiple carrier waves are compared with single reference wave with 0.8 modulation index. Three schemes of level shifting SPWM involve phase disposition, phase opposition disposition and alternate phase opposition disposition. In this paper phase disposition has been used for the pulse generation for the proposed MLI.

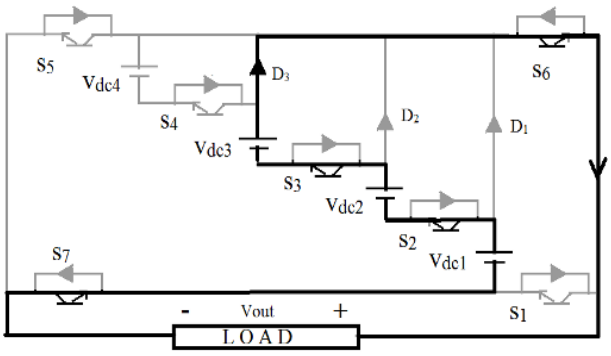
Fig.6 (a) shows the internal circuitry of SPWM pulse logic block for 9-level proposed MLI. The internal circuitry of SPWM block contains bias, relational operator, followed by logic operators. The inputs for SPWM logic block are sinusoidal waveform and triangular waveform. Pulses are generated according to switching logic and amplitude modulation index. The methodology of generating pulses for 9-level MLI is shown in Fig.6 (b). Phase opposition disposition and alternate phase opposition disposition SPWM techniques are also suitable for proposed converter.

The modulation index for SPWM Technique is the ratio of Amplitude of reference wave (A_R) to the product of number of positive or negative level and amplitude of carrier wave (A_C).

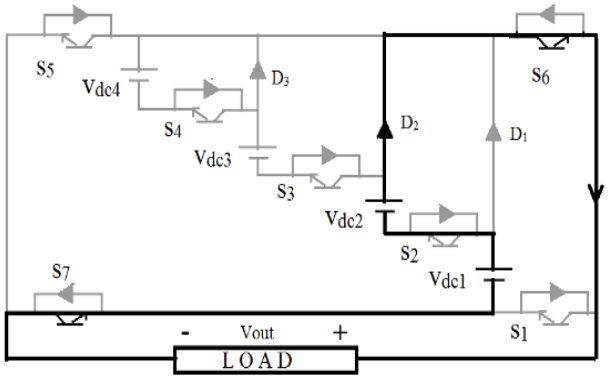
$$\text{Modulation Index} = \frac{A_R}{\frac{(N-1)}{2} \times A_C} \quad (1)$$



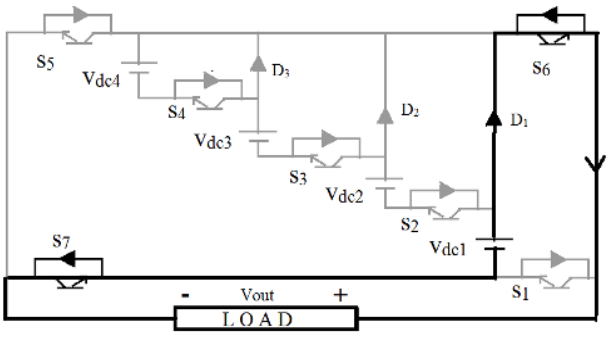
(a) $V_{out} = Vdc_4+Vdc_3+Vdc_2+Vdc_1$



(b) $V_{out} = Vdc_3+Vdc_2+Vdc_1$

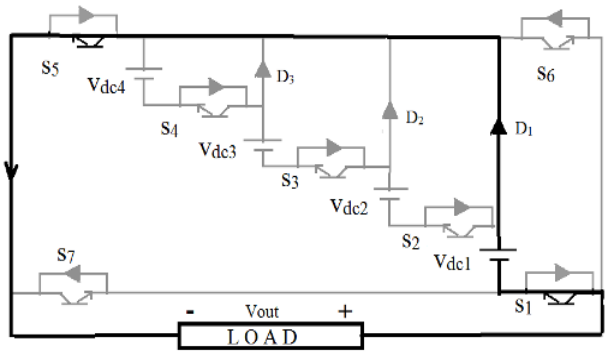


(c) $V_{out} = Vdc_2+Vdc_1$

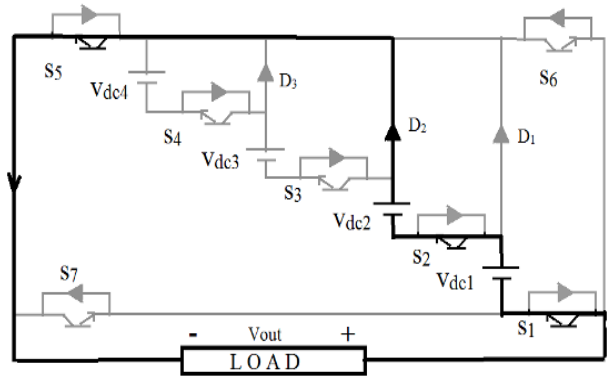


(d) $V_{out} = Vdc1$

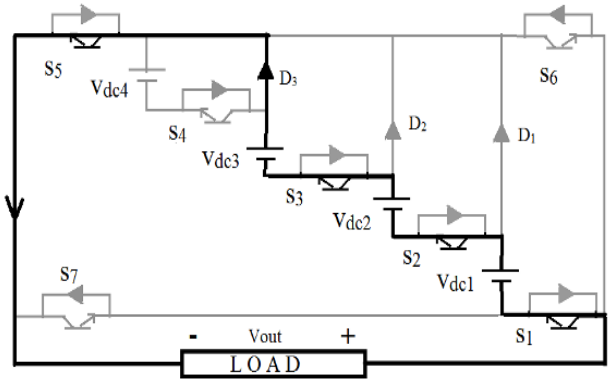
Fig.4 (a)-(d) positive levels current direction



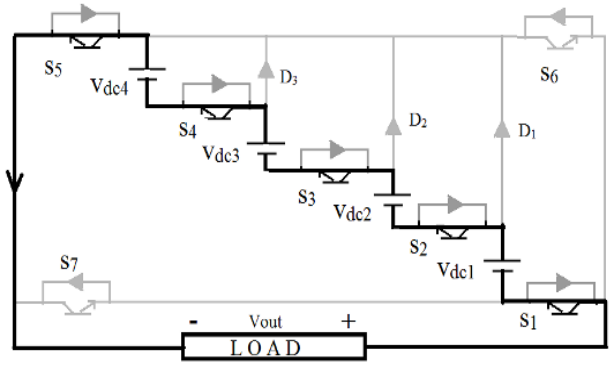
(a) $V_{out} = -Vdc_1$



(b) $V_{out} = -Vdc_2-Vdc_1$

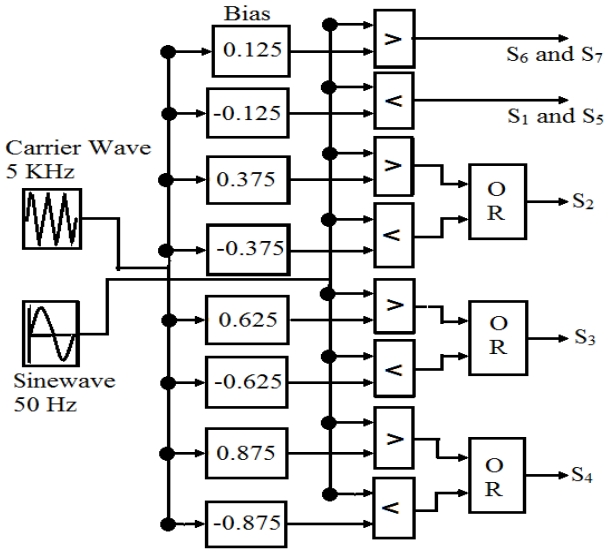


(c) $V_{out} = -Vdc_3-Vdc_2-Vdc_1$

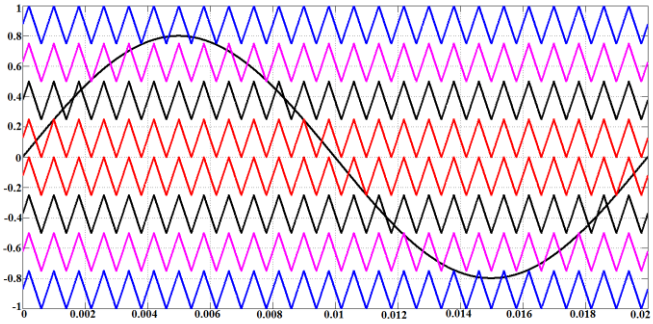


(d) $V_{out} = -Vdc_4-Vdc_3-Vdc_2-Vdc_1$

Fig.5 (a)-(d) Negative levels current direction



(a) SPWM pulse logic block



(b) methodology

Fig.6 (a)-(b) methodology for generation of pulses.

4. SIMULATION RESULTS

The proposed MLI has been designed for 2kW, 9-level output voltage using 7-switches for solar application. Four input voltage sources are used and each voltage source is equal to 60V. Phase disposition level shifting SPWM technique is used with 50 Hz reference sinusoidal wave and 5 KHz carrier wave with modulation index 0.8. The proposed 9-level inverter is designed with or without filter LC Filter. LC filter has been used with inductance of 0.5mH and capacitance of 15µF to reduce higher order harmonics. The simulation has been performed in MATLAB/SIMULINK. The switching pulse generation for switches S_1 and S_5, S_2, S_3, S_4, S_6 and S_7 has been shown in Fig.7 to Fig.11 respectively. It is observed that switches S_2, S_3 and S_4 required two carrier waveforms to obtain switching pulses whereas S_1, S_5, S_6 and S_7 required single carrier waveform. 9-level output voltage and output current waveforms without LC filter are shown in Fig.12. It is observed that 4 positive, 4 negative and 1 zero level is obtained with amplitude of each level is 60V. The highest positive level is 240V which is the positive addition of all input voltage sources. The highest negative level is -240V which is the negative addition of all input voltage sources. Fig.13 shows the output voltage and output current sinusoidal.

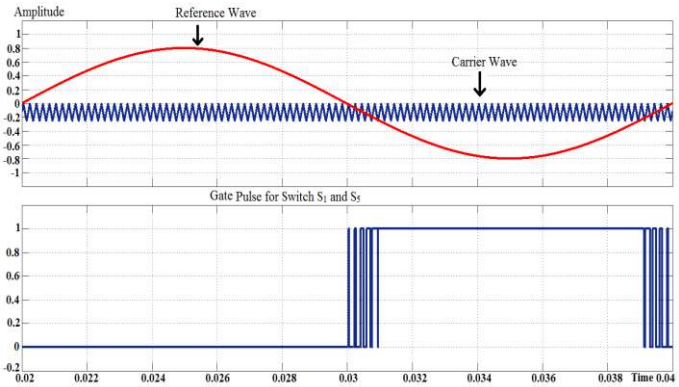


Fig.7 Pulse generation for switch S_1 and S_5

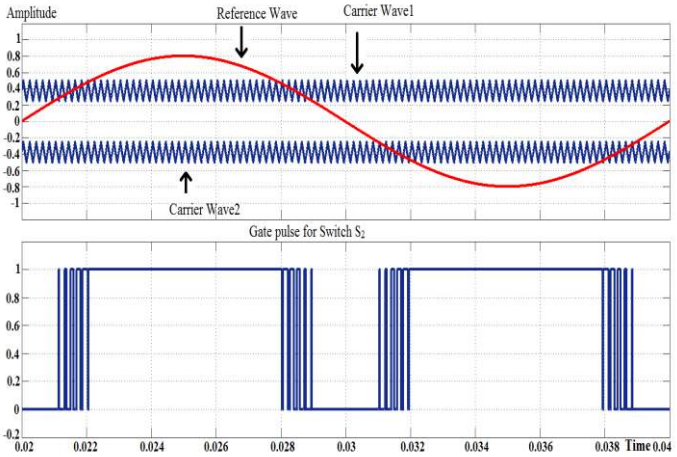


Fig.8 Pulse generation for switch S_2

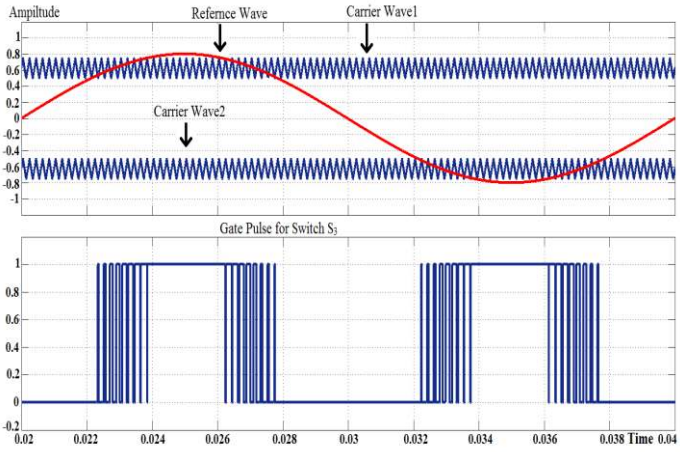


Fig.9 Pulse generation for switch S_3

The voltage stress across each switch is shown in Fig.14. It is observed that the voltage stress across switches S1, S5, S6 and S7 is 240V which is equal to the addition of all input voltage source. The voltage stress across switches S2, S3 and S4 is 60V which is equal to single input voltage source. The THD of output voltage without filter is 17.27% which is calculated by using Fast Fourier Transform (FFT) analysis window shown in Fig.15. Afterwards, higher order harmonics are eliminated by using LC filter. Fig.16 shows the THD of filtered output is 4.29%.

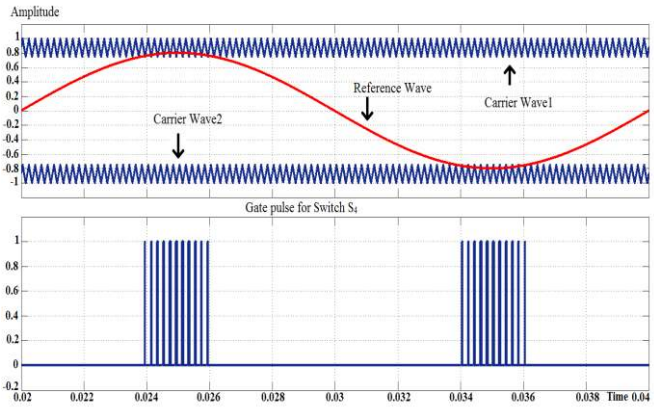


Fig.10 Pulse generation for switch S_4

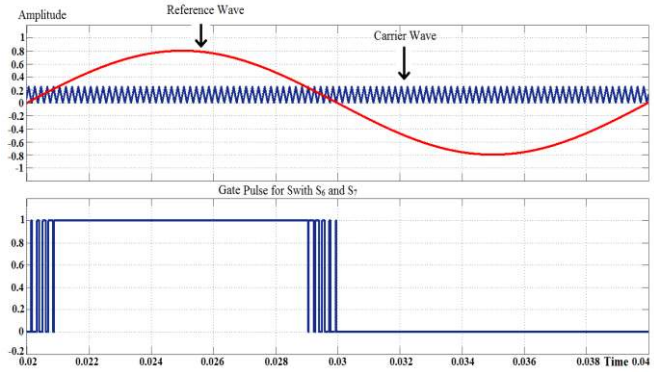


Fig.11 Pulse generation for switch S_6 and S_7

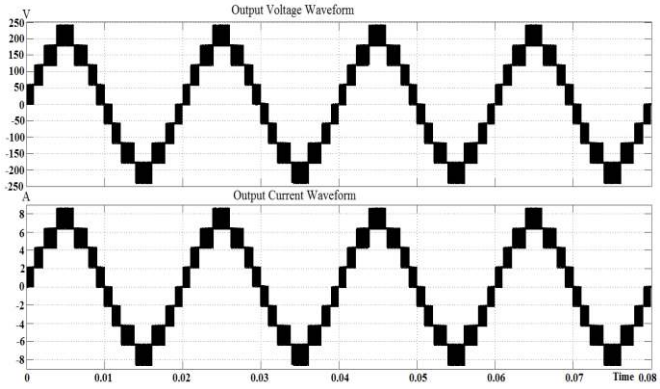


Fig.12 Output Voltage and Output Current Waveform without filter

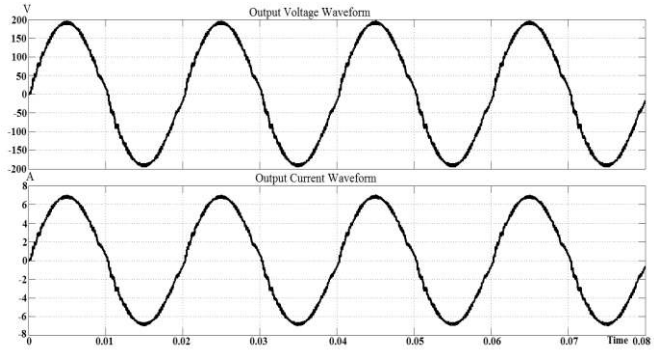


Fig.13 Output Voltage and Output Current Waveform with filter

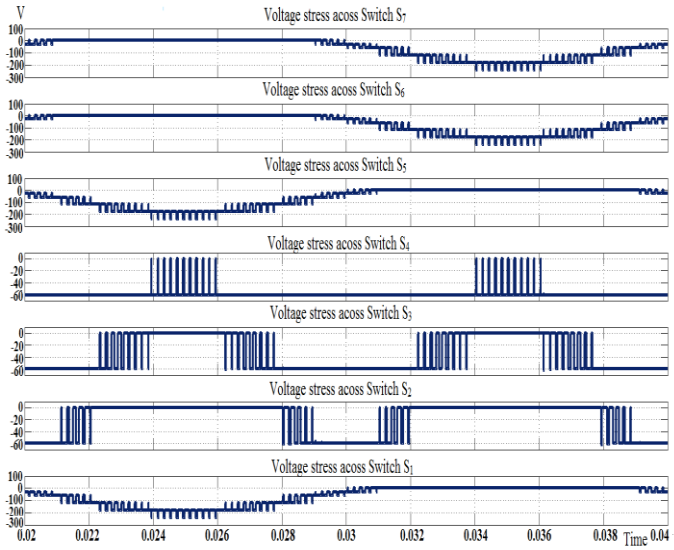


Fig.14 Voltage stress across switches

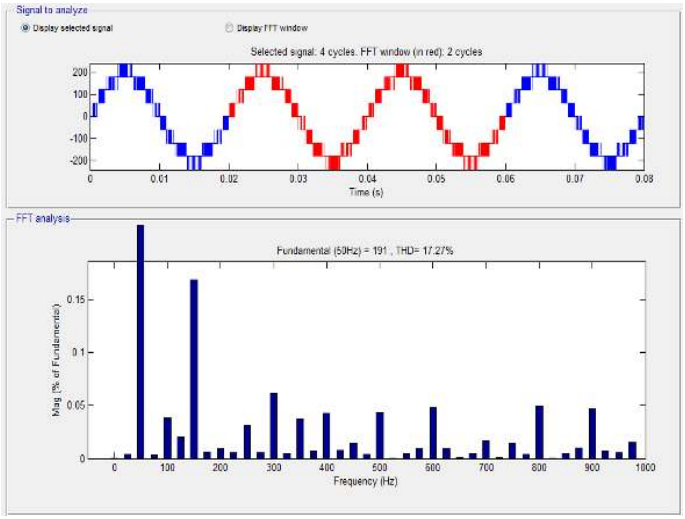


Fig.15 THD of proposed topology without filter

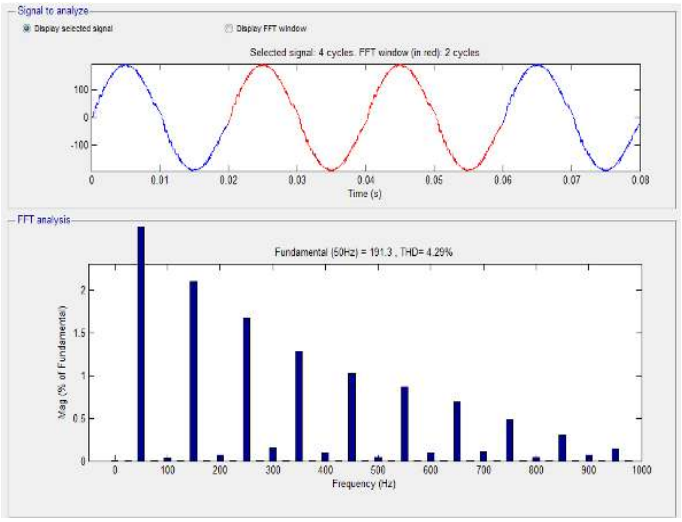


Fig.16 THD of proposed topology with filter

5. COMPARISON OF PROPOSED MLI WITH CONVENTIONAL AND EXISTING MLI

Conventional MLI includes diode clamped, flying capacitors and cascaded MLI. Diode clamped MLI required more number of diodes and switches. Flying capacitor MLI required more number of clamping capacitors and switches. Cascaded MLI required separate DC source and more number of switches. Later the above discussed drawback is overcome by modifying conventional MLI. The proposed modified H-bridge cascaded MLI consists of fewer diodes than diode clamped MLI, fewer capacitors than flying capacitor MLI, fewer switches than conventional cascaded MLI. TABLE-III shows the comparison between diode clamped, flying capacitance, cascaded H-bridge MLI and proposed MLI, where N is the level generated by single phase MLI.

Table-III COMPARISON BETWEEN SINGLE PHASE MLI

MLI Types	Switches	clamping and anti- parallel diodes	capacitor	source
Diode clamped	$2(N-1)$	$\frac{N^2-1}{2}$	$\frac{N-1}{2}$	1
Flying Capacitor	$2(N-1)$	$2(N-1)$	$\frac{(N-1)^2}{4}$	1
Cascaded H-Bridge	$2(N-1)$	$2(N-1)$	$\frac{N-1}{2}$	$\frac{N-1}{2}$
Proposed MLI	$\frac{N+5}{2}$	N+1	$\frac{N-1}{2}$	$\frac{N-1}{2}$

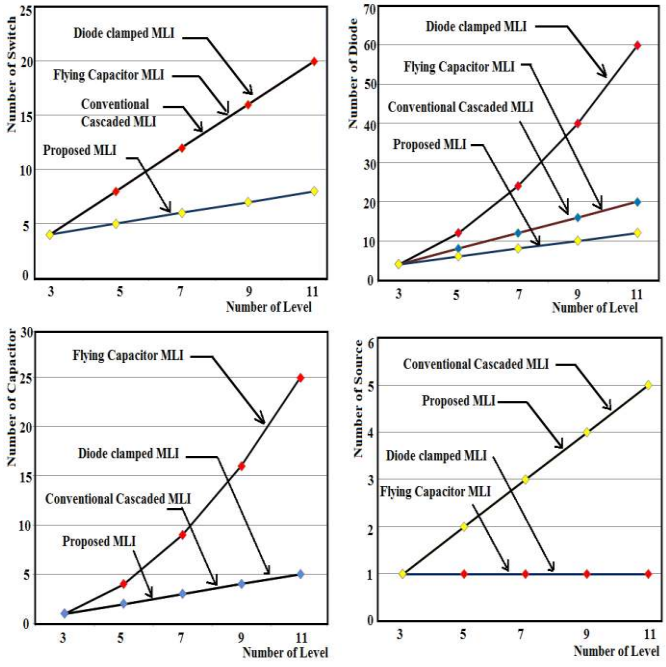


Fig.17 Graphs between numbers of power devices versus number of Levels

Fig.17 shows the graphs between required number of switches, diodes, capacitors and sources versus number of levels for proposed and conventional MLI. Proposed MLI reduces the complexity of circuit design and cost because less number of power devices required for designing the proposed MLI.

6. CONCLUSION

In this paper, a new topology of Multilevel Inverter (MLI) with fewer number of switches is designed for solar applications which overcomes the drawbacks of conventional multilevel inverter. (N+5)/2 switches with anti-parallel diodes, (N-3)/2 clamping diodes and (N-1)/2 sources are needed to design N-Level proposed inverter. The proposed MLI advantages include fewer number of switches which in turn reduced the corresponding gate driving circuitry, made the circuit compact in size. Due to which optimization of circuit layout is possible. The proposed MLI is designed for 9-level with power 2kW and In-Phase level shifting SPWM technique is used for the generate switching pulses for switches of the MLI. It is observed that output voltage total harmonics distortion (THD) of 9 level proposed MLI without filter is 17.27% whereas with filter is 4.29%. The simulation results and pulse generation using SPWM technique also discussed. The simulation results show that proposed MLI has the characteristics which are desirable for solar based high power applications.

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