Multilevel Inverters: A Comparative Study of Pulse Width Modulation Techniques

B.Urmila, D.Subbarayudu

ABSTRACT— The multilevel inverter topology gives the advantages of usage in high power and high voltage application with reduced harmonic distortion without a transformer. This paper presents a comparative study of nine level diode clamped inverter for constant Switching frequency of sinusoidal Pulse width Modulation and sinusoidal Natural Pulse width Modulation with switching frequency Optimal Modulation.

INDEX TERMS— Multicarrier Pulse Width Modulation, diode clamped inverter, Switching frequency optimal Pulse Width Modulation, Sub-Harmonic Pulse Width Modulation, Constant switching frequency, Sinusoidal Natural Pulse Width Modulation, Sinusoidal Pulse Width Modulation, multilevel converter, multilevel inverter Total harmonic distortion.

1 INTRODUCTION

MULTILEVEL Pulse Width Modulation (PWM) inverters have been gained importance in high performance power applications without requiring high ratings on individual devices, as static var compensators, drives and active power filters. A multilevel inverter divides the dc rail directly or indirectly, so that the output of the leg can be more than two discrete levels. As both amplitude modulation and pulse width modulation are used in this, the quality of the output waveform gets improved with low distortion. The advantages of multilevel inverter are good power quality, low switching losses, reduced output dv / dt and high voltage capability. Increasing the number of voltage levels in the inverter increases the power rating. The three main topologies of multilevel inverters are the Diode clamped inverter, Flying capacitor inverter, and the Cascaded H-bridge inverter [1][2]. The PWM schemes of multilevel inverters are classified in to two types the multicarrier sub-harmonic PWM (MC-SHPWM) and the Multicarrier switching frequency optimal pulse width modulation (MC-SFOPWM) [4][5]. The MC-SHPWM diode clamped multilevel inverter strategy reduced total harmonic distortion and the MC-SFOPWM technique for multilevel inverter strategy enhances the fundamental output voltage [6]. This paper considered the most popular structure among the transformerless voltage source multilevel inverters, the diode-clamped converter based on the neutral point converter proposed by Akagea et al [1].

2 MULTILEVEL INVERTER SCHEMATIC DIAGRAMS

Fig 1(a) shows a two level inverter. Fig 1(b) shows a three level inverter. Fig 1(c) shows N level inverter. All the capacitors comprises to a voltage of V_{dc}.

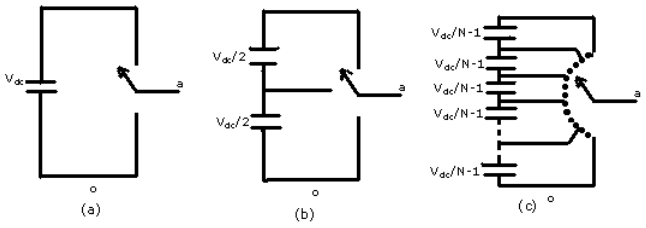

Figure 1 Schematic Diagram of (a) Two level Inverter (b) Three Level Inverter (c) N Level Inverter

Fig 2(a) shows the output voltage of a two level inverter. Fig 2(b) shows the output voltage a three level inverter. Fig 2(c) shows the output voltage of an N level inverter.

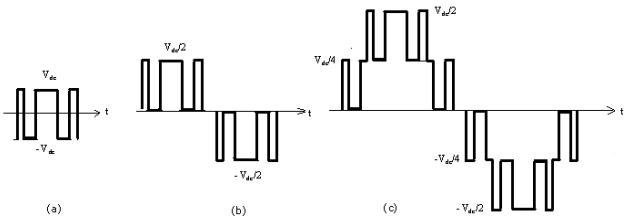

Figure 2 Output Voltage of (a) Two Level Inverter (b) Three Level Inverter (c) Five Level Inverter

3 DIODE CLAMPED MULTILEVEL INVERTER

For an N level (between the phase and the negative rail) diode clamped inverter,

The number of levels in the line-to-line voltage waveform will be k=2N-1 (1)

The number of levels in the line to load neutral of a star or wye load will be p=2k-1 (2)

The number of capacitors required, independent of the number of phase, is N_{cap}=N-1 (3)

While the number of clamping diodes per phase is D_{clamp}=2(N-1) (4)

The number of possible switch states is

$$n_{states}=N^{phases} \quad (5)$$

and the number of switches in each leg is

$$S_n=2(N-1) \quad (6)$$

4 PWM METHODS FOR MULTILEVEL INVERTERS

The two basic approaches used to generate the PWM signals for multilevel inverters are

- Sub harmonic or Sub-Oscillation carrier based PWM-modulating waveform comparison with offset triangular carriers
- Space Vector PWM-space vector modulation based on a rotating vector in multilevel space

and these are the extensions of traditional two level control strategies to several levels.

The two main advantages of PWM inverters in comparison to square-wave inverters are (i) control over output voltage magnitude (ii) reduction in magnitudes of unwanted harmonic voltages. Good quality output voltage in SPWM requires the modulation index (m) to be less than or equal to 1.0. For m>1 (over-modulation), the fundamental voltage magnitude increases but at the cost of decreased quality of output waveform. The maximum fundamental voltage that the SPWM inverter can output (without resorting to over-modulation) is only 78.5% of the fundamental voltage output by square-wave inverter. In this paper one more PWM techniques have been considered. The merits and demerits of these two PWM techniques are compared under comparable circuit conditions on the basis of factors like (i) quality of output voltage (ii) obtainable magnitude of output voltage (iii) ease of control etc. The peak obtainable output voltage from the given input dc voltage is one important figure of merit for the inverter.

Carrara considered different methods of disposing the many carrier bands required in multilevel PWM.

Four alternative carrier PWM strategies with differing phase relationships for a multilevel inverter [15] are as follows:

1) In-phase disposition (IPD), where all the carriers are in phase- Technique A1;
2) Phase opposition disposition (POD), where the carriers above the zero reference are in phase, but shifted by 180^0 from those carriers below the zero reference- Technique A2;
3) Alternative phase opposition disposition (APOD), where each carrier band is shifted by 180^0 from the adjacent bands- Technique A3;
4) Phase Disposition (PD), all the carriers are phase shifted by $2\pi/(N-1)$ radians- Technique B.

PD strategy is used most frequently because it produces minimum harmonic distortion for the line–to–line output voltage [13],[14],[15],[16],[17].

4.1 SubHarmonic Pulse Width Modulation SHPWM Technique

In SHPWM technique the intersection of the triangular carrier and the modulation wave determines the generation of the pulse. This requires a carrier of much higher frequency than the modulation frequency. The generated rectilinear output voltage pulses are modulated such that their duration is proportional to the instantaneous value of the sinusoidal waveform at the centre of the pulse; that is, the pulse area is proportional to the corresponding value of the modulating sine wave.

If the carrier frequency is very high, an averaging effect occurs, resulting in a sinusoidal fundamental output with high-frequency harmonics, but minimal low-frequency harmonics.

4.2 Switching Frequency Optimal Pulse width Modulation SFOPWM Technique

Steinke [12] proposed SFOPWM, a carrier based method where addition of triplen harmonic to the fundamental frequency Sinusoidal lowers the peak magnitude, thus allowing operating in over modulation region. This increases the inverter output voltage without compromising on the quality of the output waveform [3][4].

Equations (9) to (12) are used to obtain the modulating wave.

$$V_{offset} = (\max(V_a,V_b,V_c) + \min(V_a,V_b,V_c))/2 \quad (9)$$
$$V_{aSFO} = V_a - V_{offset} \quad (10)$$
$$V_{bSFO} = V_b - V_{offset} \quad (11)$$
$$V_{cSFO} = V_c - V_{offset} \quad (12)$$

The zero sequence modification made by the SFOPWM technique restricts its use to three phase three wire system; however it enables the modulation index to be increased by 15.47% before over modulation or pulse dropping occurs.

The amplitude modulation index and frequency modulation index are given in (13) and (14) respectively.

$$m_a = A_m / (m-1)A_c \quad (13)$$
$$m_f = f_c / f_m \quad (14)$$

Where m is the number of carrier waves also the level of the inverter, required for pulse generation.

A sinusoidal and its modulated wave obtained from (13), (14) are shown in Fig.3 for a modulation index of 1.

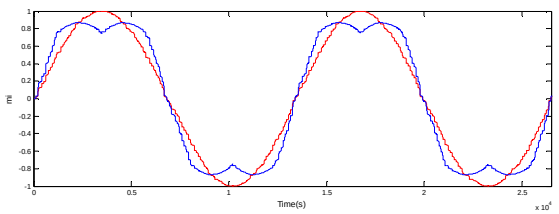

Figure 3 Single Phase Modulating Wave

4.3 Sinusoidal Natural PWM and Sinusoidal PWM Techniques

Operation of a multilevel inverter at low switching frequency is the Sinusoidal natural PWM and alternately sinusoidal PWM technique is operation at high switching frequency.

5 Analysis Of Nine Level Diode Clamped Inverter

A three-phase nine-level diode-clamped inverter is shown in Fig.4 [15][17]. Each phase is constituted by 16 switches (eight switches for upper leg and eight switches for lower leg). Switches S_{a1} through S_{a8} of upper leg form complementary pair with the switches S_{a1}' to S_{a8}' lower leg of the same phase. The complementary switch pairs for phase 'A' are (S_{a1}, S_{a1}'), (S_{a2}, S_{a2}'), (S_{a3}, S_{a3}'), (S_{a4}, S_{a4}'), (S_{a5}, S_{a5}'), (S_{a6}, S_{a6}'), (S_{a7}, S_{a7}'), (S_{a8}, S_{a8}') and similarly for B and C phases [1],[2],[3],[4],[5],[6],[7],[8],[17]. Clamping diodes are used to carry the full load current.

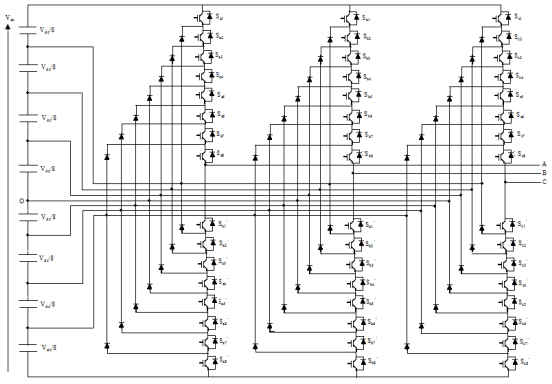

Figure 4 Circuit Diagram of 3 Phase Nine Level Diode Clamped Inverter

Table 1 shows phase to fictitious midpoint 'o' of capacitor string voltage (V_{AO}) and line to line voltage (V_{AB}) for various switchings'.

TABLE 1
POLE VOLTAGE AND LINE VOLTAGE OF A NINE LEVEL INVERTER

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	V_{AB}	V_{AO}
1	1	1	1	1	1	1	1	V_{dc}	V_{dc}
0	1	1	1	1	1	1	1	$V_{dc}/8$	$3V_{dc}/4$
0	0	1	1	1	1	1	1	$2V_{dc}/8$	$2V_{dc}/4$
0	0	0	1	1	1	1	1	$3V_{dc}/8$	$V_{dc}/4$
0	0	0	0	1	1	1	1	$4V_{dc}/8$	0
0	0	0	0	0	1	1	1	$5V_{dc}/8$	$-V_{dc}/4$
0	0	0	0	0	0	1	1	$6V_{dc}/8$	$-2V_{dc}/4$
0	0	0	0	0	0	0	1	$7V_{dc}/8$	$-3V_{dc}/4$
0	0	0	0	0	0	0	0	0	$-V_{dc}$

This paper provides analytical methods for the study, performance evaluation, and design of the modern carrier-based PWM's, like bipolar and unipolar suboscillation carrier PWM methods which are widely employed in PWM multilevel voltage-source inverter drives due to the low-harmonic distortion waveform characteristics with well-defined harmonic spectrum, the fixed switching frequency, and implementation simplicity. Simple techniques for generating the modulation waves of the high-performance PWM methods are described. The two novel methodologies Natural Sinusoidal PWM and Sinusoidal PWM for 3rd harmonic injected modulated wave called SFOPWM using constant switching frequency are compared[4],[5]. The one most important modulator characteristics—the total harmonic distortion is analytically modeled and compared for various carrier pwm methods applied to a nine level Neutral point clamped or Diode clamped inverter. Simulations of the controller and of the inverter have been made in the MATLAB SIMULINK environment.

A nine level inverter is simulated for a normal modulation index of 0.8 and over modulation index of 1.1 at a switching frequency of 450Hz for Sinusoidal natural PWM and 1050Hz for Sinusoidal PWM technique.

6 Simulation Results and Discussions

Table 2 show at normal modulation index of 0.8 improved performance with reduced harmonic distortion is observed with SPWM technique for A1through B techniques for nine level diode clamped inverter.

TABLE 2
LINE-LINE VOLTAGE AND THD FOR NORMAL MODULATION INDEX

	SNPWM		SPWM	
	Vab	THD	Vab	THD
A1	44.94	10.27	46.55	9.46
A2	45.53	12.24	46.72	9.29
A3	45.59	11.38	46.63	9.49
B	59.58	17.32	60.61	13.50

A table 3 show at over modulation index of 1.1 improved performances with reduced harmonic distortion is observed with SPWM technique for A1through B techniques for nine level diode clamped inverter.

TABLE 3
LINE-LINE VOLTAGE AND THD FOR OVER MODULATION INDEX

	SNPWM		SPWM	
	Vab	THD	Vab	THD
A1	65	7.89	65.67	6.89
A2	65.78	9.13	66.09	7.93
A3	65.84	8.55	66.02	7.42
B	66.49	16.51	67.1	13.39

Fig 5 to Fig 10 shows the pole voltage, line voltage and its THD for normal modulation index of 0.8 for phase disposition technique A1 for SNPWM tecchnique with a frequency of 450Hz and SPWM for 1050Hz frequency.

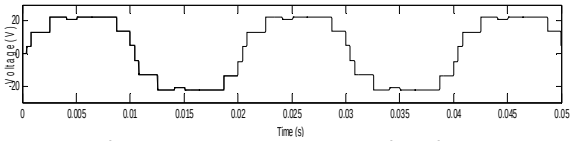

Figure 5 0.8 A1 SNPWM Pole Voltage

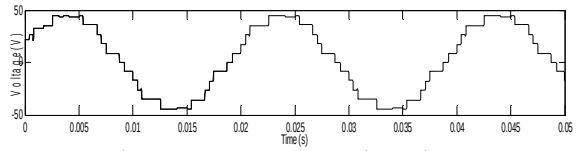

Figure 6 0.8 A1 SNPWM Line Voltage

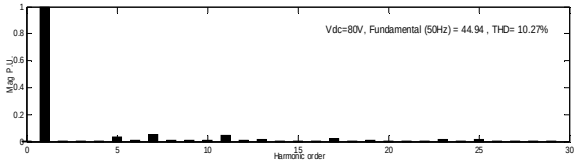

Figure 7 0.8 A1 SNPWM Line Voltage THD

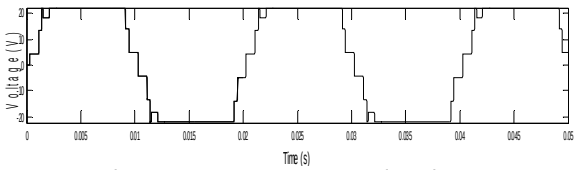

Figure 8 0.8 A1 SPWM Pole Voltage

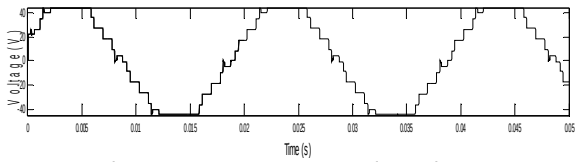

Figure 9 0.8 A1 SPWM Line Voltage

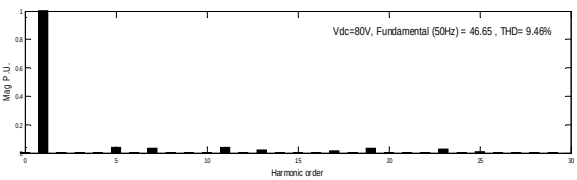

Figure 10 0.8 A1 SPWM Line Voltage THD

Fig 10 to Fig 16 shows the pole voltage, line voltage and its THD for over modulation index of 1.1 for phase disposition technique A1 for SNPWM tecchnique with a frequency of 450Hz and SPWM for 1050Hz frequency.

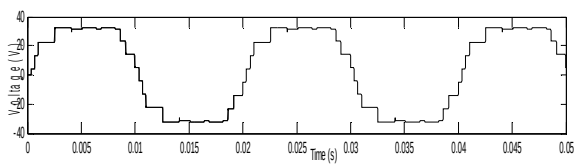

Figure 11 1.1 A1 SNPWM Pole Voltage

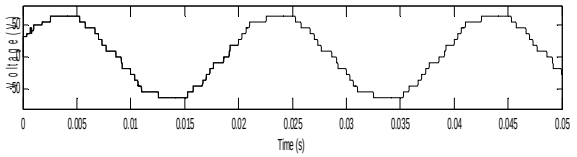

Figure 12 1.1 A1 SNPWM Line Voltage

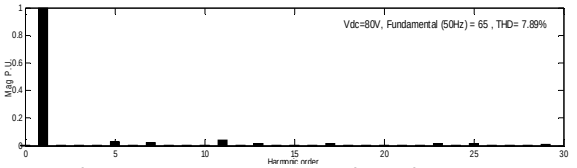

Figure 13 1.1 A1 SNPWM Line Voltage THD

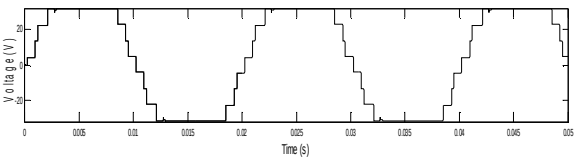

Figure 14 1.1 A1 SPWM Pole Voltage

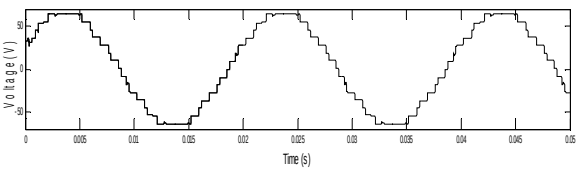

Figure 15 1.1 A1 SPWM A1 Line Voltage

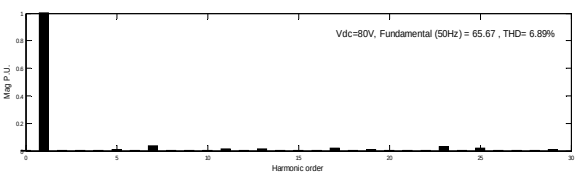

Figure 16 1.1 A1 SPWM Line Voltage THD

7 CONCLUSION

A third harmonic injected modulated wave is used to generate the gating signals for a modeled nine level diode clamped multilevel inverter. The technique SPWM has shown improved performance over SNPWM technique.

REFERENCES

[1] José Rodríguez, Jih-Sheng Lai, Fang Zheng Peng "*Multilevel Inverters: A Survey of Topologies, Controls, and Applications",* IEEE Trans., VOL. 49, NO. 4, AUGUST 2002

[2] G.Carrara, S.Gardella, M.Marchesoni, R.Salutari and G.Sciutto, " A New Multilevel PWM Method: A theoretical Analysis", IEEE Transactions on Power Electronics, Vol. 7, No. 3, July 1992, pp.497-505.

[3] A. Nabae, I. Takahashi, H. Akagi. "*A neutral-point clamped PWM inverter*", IEEE Trans. on I.A., Vol. IA-17, No. 5, 1981, pp. 518-523.

[4] P.Palanivel1, Subhransu Sekhar Dash, "*Comparative Study of Constant Switching Frequency and Variable Switching Frequency Multicarrier Pulse width Modulation for Three Phase Cascaded Mul-*

tilevel Inverter"., International Journal of Recent Trends in Engineering, Vol 2, No. 7, November 2009.

[5] P.Palanivel1, Subhransu Sekhar Dash, "*Multicarrier Pulse Width Modulation Based Three Phase Cascaded Mulitilevel Inverter Including Over Modulation and Low Modulation Indices"*, International Journal of Engineering Studies ISSN 0975- 6469 Volume 1, Number 2 (2009), pp. 71–82

[6] A. Nabae, I. Takahashi, and H. Akagi, "*A new neutral-point-clamped PWM inverter,*" IEEE Trans. Ind. Applicat., pp. 518–523, Sept./Oct.1981.

[7] J. S. Lai and F. Z. Peng, "*Multilevel converters—A new breed of power converters*," IEEE Trans. Ind. Applicat., Vol. 32, pp. 509–517, May/June 1996.

[8] M. Carpita, M. Fracchia. S. Tenconi. "*A novel multilevel structure for voltage source inverter*", Proceedings of the 4th European Conf, on Power Electronics and Applications (EPE'91), Firenze, Italy, September 1991, pp.1-090/1-094.

[9] J. Holtz, "*Pulsewidth modulation—A survey*," IEEE Trans. Ind. Electron., Vol. 39, pp. 410–420, Oct. 1992.

[10] Nguyen Van Nho, Quach Thanh Hai, Hong Hee Lee," *Carrier Based Single-State Pwm Technique In Multilevel Inverter*", International Symposium on Electrical & Electronics Engineering 2007 - Oct 24, 25 2007

[11] B. P. McGrath, D.G. Holmes, M. Manjrekar, T. A. Lipo, "*An Improved Modulation Strategy For A Hybrid Multilevel Inverter"*2000.

[12] J.K. Steinke, "*Control Strategy for a Three Phase AC Traction Drive with a 3-level GTO PWM Inverter*", IEEE PESC, 1988, pp. 431-438.

[13] Ivo Pereira, António Martins, "*Experimental Comparison of Carrier and Space Vector PWM Control Methods for Three-Phase NPC Converters"* International Conference on Renewable Energies and Power Quality (ICREPQ'09), Valencia (Spain), 15th to 17th April, 2009.

[14] A.Tahri, A.Draou "A Comparative Modelling Study of PWM Control Techniques for Multilevel Cascaded Inverterr", Leonard Journal of Sciences ,Jan-Jun 2005 , pp 42-58.

[15] leon M. Tolbert, Fang Z.Peng, ,Thomas G. Habetler, "Multilevel PWM Methods at Low Modulation Indices" APEC '99, Dallas, Texas, March 14-18, pp 1032-1039.

[16] Leon M. Tolbert, Fang Z.Peng, ,Thomas G. Habetler, "*Novel Multilevel Inverter Carrier-Based PWM"* IEEE IAS 1998, Missouri, October 10-15, 1998, pp. 1424-1431.

[17] Samir Kouro, *IEEE*, Pablo Lezana, Mauricio Angulo, and José Rodríguez, "*MulticarrierPWMWith DC-Link Ripple Feedforward compensation for Multilevel Inverters"* IEEE Transactions On Power Electronics, VOL. 23, NO. 1, JANUARY 2008.

[18] Jang-Hwan Kim, Seung-Ki Sul and Prasad N. Enjeti, "*A Carrier-Based PWM Method with Optimal Switching Sequence for a Multi-level Four-leg VSI"* IEEE , June 2005, pp 99-105. for spwm,sfopwm ,npc.