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Multilevel Voltage-Source Duty-cycle Modulation: Analysis and Implementation

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***Abstract*—Multilevel converters have become increasingly popular in recent years due to high power quality, high-voltage capability, low switching losses, and low electromagnetic compatibility concerns. Considering these advantages, the multilevel converter is a suitable candidate for implementation of future naval ship propulsion systems. This paper focuses on modulation techniques for the multilevel converter. In particular, a novel voltage-source method of multilevel modulation is introduced and compared to existing methods. The proposed method is discrete in nature and can therefore be readily implemented on a digital signal processor. The method is also readily extendable to any number of voltage levels. Results of experimental implementation are demonstrated using a four-level rectifier/inverter system, which incorporates diode-clamped multilevel converters and an 11-level cascaded multilevel H-bridge inverter.**

***Index Terms*—Multilevel converters, pulsewidth modulation, sine triangle, space vector, voltage source.**

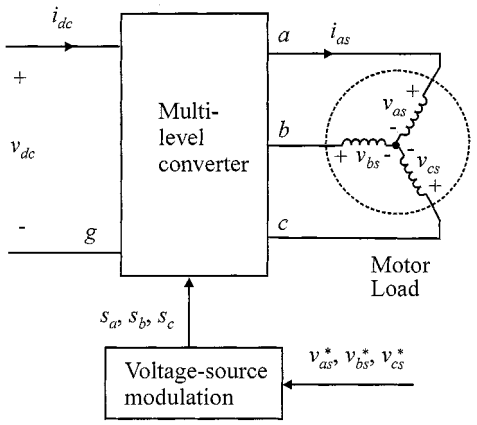

Fig. 1. General multilevel converter structure.

I. Introduction

MULTILEVEL power conversion, introduced in 1981 [1], has gained much attention in recent years [2]–[18] and is the subject of state-of-the-art power electronic research. The general concept involves producing ac waveforms from small voltage steps by utilizing isolated dc sources or a bank of series capacitors. The small voltage steps yield waveforms with low harmonic distortion as well as low dv/dt's. Further advantages include high-voltage capability and low switching losses due to the arrangement of the semiconductor devices. The primary disadvantage of multilevel converters is that a larger number of semiconductor devices are required when compared to traditional power converters. This does not lead to an increase in semiconductor costs since lower voltage rated transistors may be used. However, it does increase the required gate drive circuitry and lead to a more complex mechanical layout.

Pulsewidth modulation (PWM) of multilevel converters is typically an extension of two-level methods [19]–[22]. The most common types of multilevel voltage-source PWM are sine-triangle modulation and space-vector modulation (SVM). Multilevel sine-triangle modulation relies on defining a number of triangle waveforms and switching rules for the intersection of these waveforms with a commanded voltage waveform [2]–[4]. This method is fairly straightforward and insightful for description of multilevel systems. Multilevel SVM is performed by considering the converter switching states in the q–d stationary reference frame [5]–[8]. Although more mathematically cumbersome than sine-triangle modulation, the method is more readily implemented on a digital signal processor (DSP). Recent SVM research has focused on methods of simplifying the nearest voltage vector selection [13], [14]. Other research has demonstrated the equivalence of SVM and sine-triangle modulation [15], [16] and that changing free parameters in the SVM method (such as dwell time or switching sequence) can be done as well in sine-triangle modulation by choosing the shape of the sine and triangle waveforms.

In this paper, a method is presented which is based on time-domain duty cycles. The equivalence of switching state production to that of sine-triangle modulation and SVM is shown. However, the method introduced herein does not require the definition of triangle waveforms or voltage vectors. The method is mathematically straightforward but discrete in nature for DSP implementation.

II. Multilevel Power Conversion

Fig. 1 shows a general structure that is typical of most multilevel conversion systems. Therein, the power conversion is performed between a single dc source and a motor load. In this paper, the term converter will be used to denote a power section, which may convert power from a dc source to an ac load or vise-versa. Although inverter examples will be primarily shown here, it should be pointed out that the modulation method is applicable to both inverter and rectifier applications and may be connected to an electric utility or other type of load. At this

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stage in the development, the type of converter is not significant. A diode-clamped [2]–[9], [11], flying capacitor [10], or other novel topologies [5], [6] may be inserted in the multilevel converter block in Fig. 1. The primary exception to this is the cascaded H-bridge converter, which is supplied from several isolated sources. However, it will be shown in the development that the modulation method applies to these converters as well with a slight modification to one equation.

The first step in the converter analysis involves definition of the load voltages in terms of the inverter line-to-ground voltages, which may be expressed as [23]

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}. \tag{1}$$

Under proper multilevel converter operation, the line-to-ground voltages may be directly controlled to be some fraction of the dc-link voltage. In particular, the line-to-ground voltage for phase x is

$$v_{xg} = \frac{s_x}{(n-1)} v_{\rm dc}, \qquad s_x = 0, 1, \ldots (n-1) \tag{2}$$

where n is the number of voltage levels that the converter is capable of producing and s_x is the switching state determined by the modulator for phase x. As can be seen from (2), the switching state defined herein is directly related to the voltage level. It is also directly related to the transistor signals for a given converter topology [5],[6], [18]. It should be pointed out that (2) is an idealized equation in that it is assumed that a capacitor bank with balanced voltages or isolated dc voltage sources are available. In practice, this may be readily ensured as will be demonstrated in the laboratory examples shown below. It is sometimes helpful to express the switching states for all three phases compressed into one variable. For this reason, the overall switching state will be defined as

$$\text{sw} = n^2 s_a + n s_b + s_c. \tag{3}$$

Using (3), the switching state sw is a number in the mathematical base of the number of converter levels. For example, if a four-level converter is considered, sw will be a base four representation of the switching states of the individual phases. For a p phase converter, the total number of switching states is

$$n_{\rm sw} = n^p. \tag{4}$$

For converter analysis purposes, it is often convenient to view the voltages in the q–d stationary reference. Transformation to this reference frame is accomplished through [23]

$$v_{qs}^s = \frac{2}{3}\left(v_{as} - \frac{1}{2}v_{bs} - \frac{1}{2}v_{cs}\right) \tag{5}$$

$$v_{ds}^s = \frac{1}{\sqrt{3}}\left(v_{cs} - v_{bs}\right). \tag{6}$$

Plotting v_{qs}^s and v_{ds}^s for all possible switching states, results in the voltage vector plot [6], [7]. As an example, consider the four-level converter ($n = 4$). According to (4), there are 64 unique switching states. Fig. 2 shows the voltage vector plot for this converter. Therein, each voltage vector is represented by a dot with the vector number $v_{\rm sw}$. As can be seen, some switching states produce the same voltages in the q-d stationary plane (i.e., v_{36} and v_{57}). Due to these redundant switching states, there are only 37 unique voltage vectors produced from the 64 switching states. In general, the number of voltage vectors for a three-phase converter can be calculated from

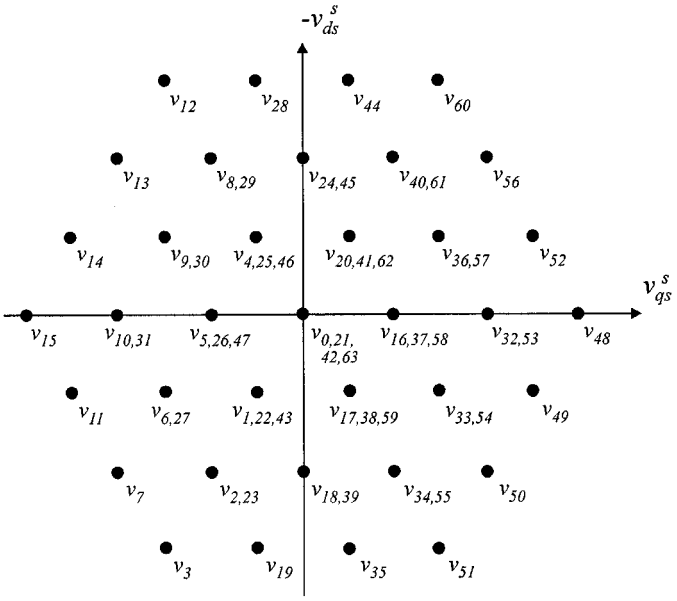

Fig. 2. Voltage vector plot for the four-level converter.

$$n_v = 3n(n-1) + 1. \tag{7}$$

Fig. 1 also depicts the modulation section of the converter. As can be seen, the switching states are based on commanded phase voltages v_{as}^*, v_{bs}^*, and v_{cs}^*.

III. Multilevel Voltage-Source Modulation

A. Duty Cycles

The basis of the modulation method introduced herein is to define duty cycles for each phase, which will be based on commanded line-to-ground voltages. However, a supervisory control (such as an induction motor vector control) will typically output commanded phase voltages, which may be expressed

$$v_{as}^* = \sqrt{2} v_s^* \cos(\theta_c) \tag{8}$$

$$v_{bs}^* = \sqrt{2} v_s^* \cos\left(\theta_c - \frac{2\pi}{3}\right) \tag{9}$$

$$v_{cs}^* = \sqrt{2} v_s^* \cos\left(\theta_c + \frac{2\pi}{3}\right) \tag{10}$$

where v_s^* is the commanded magnitude and θ_c is the electrical angle. Since the determinate of the matrix in (1) is zero, there are an infinite number of commanded line-to-ground voltage sets that will yield the commanded phase voltages. This is due to the fact that zero-sequence terms in the commanded line-to-ground voltages cancel in (1). In a three-phase system, the zero-sequence components of v_{ag}^*, v_{bg}^* and v_{cg}^* are dc offsets and triplen harmonics of the fundamental frequency. The quantity and amplitude of triplen harmonics added to the commanded line-to-ground voltages may be selected in order to maximize

converter output voltage [22], reduce switching losses [21], or improve harmonic distortion [21]. Herein, a third harmonic will be added in order to maximize the output voltage resulting in commanded line-to-ground voltages of

$$v_{ag}^* = \frac{v_{\rm dc}}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \quad (11)$$

$$v_{bg}^* = \frac{v_{\rm dc}}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \quad (12)$$

$$v_{cg}^* = \frac{v_{\rm dc}}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \quad (13)$$

where m is a modulation index. The PWM will achieve these commanded voltages (if the switching frequency component is neglected). The resulting phase voltages may be determined by substituting (11)–(13) into (1) which results in

$$\hat{v}_{as} = \frac{m v_{\rm dc}}{2}\cos(\theta_c) \quad (14)$$

$$\hat{v}_{bs} = \frac{m v_{\rm dc}}{2}\cos\left(\theta_c - \frac{2\pi}{3}\right) \quad (15)$$

$$\hat{v}_{cs} = \frac{m v_{\rm dc}}{2}\cos\left(\theta_c + \frac{2\pi}{3}\right). \quad (16)$$

In (14)–(16), the symbol $\hat{}$ represents fast-average which neglects the switching components of the PWM. By comparing (14)–(16) with the commanded voltages (8)–(10), it can be seen that the commanded voltage are achieved if the modulation index is set to

$$m = \frac{2\sqrt{2}v_s^*}{v_{\rm dc}}. \quad (17)$$

At this point, it would be important to point out the difference between modulation methods for cascaded H-bridge type of converters [12], [18]. In H-bridge based converters, the range of output voltage is twice that of converters where one dc voltage supplies all three phases (as in Fig. 1). In this case, the modulation index must be related to the commanded voltage magnitude by

$$m_H = \frac{\sqrt{2}v_s^*}{v_{\rm dc}}. \quad (18)$$

The modulation process described herein may be applied to H-bridge converters by substituting m_H for m in the equations that follow.

Since the third-harmonic term has been added to the commanded line-to-ground voltages, the modulation index has a range of [22]

$$0 \le m \le \frac{2}{\sqrt{3}}. \quad (19)$$

It is sometimes helpful to express the modulation index as a percentage of the maximum available voltage by defining

$$\bar{m} = \frac{\sqrt{3}}{2}m. \quad (20)$$

Duty cycles will now be defined by normalizing the commanded line-to-ground voltages to the dc voltage. This results in duty cycles of

$$d_a = \frac{1}{2}\left[1 + m\cos(\theta_c) - \frac{m}{6}\cos(3\theta_c)\right] \quad (21)$$

$$d_b = \frac{1}{2}\left[1 + m\cos\left(\theta_c - \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right] \quad (22)$$

$$d_c = \frac{1}{2}\left[1 + m\cos\left(\theta_c + \frac{2\pi}{3}\right) - \frac{m}{6}\cos(3\theta_c)\right]. \quad (23)$$

From the duty cycles, the switching state and switching times to be directly determined as described in the following section.

B. Timer Scheduling

Performing PWM switching from duty cycles in a multilevel converter is based on determining the nearest voltage levels (or the three nearest vectors in SVM) and the percentage of time spent at each level. This information may be determined by modifying the range on the duty cycles. Specifically, for phase x the modified duty cycle is

$$d_{xm} = (n-1)d_x. \quad (24)$$

The nearest voltage level is then directly found by integerizing the modified duty cycle as

$$l_x = \text{INT}(d_{xm}) \quad (25)$$

where the INT function returns the nearest integer that is less than or equal to its argument. The time spent in this level can be determined from

$$t_x = (d_{xm} - l_x)T_{\rm sw} \quad (26)$$

where $T_{\rm sw}$ is the switching period of the DSP. The remainder of the switching period is spent in the voltage level $l_x + 1$. As an example of how the switching may be accomplished, consider the switching state scheduling over one DSP period

$$s_x = \begin{cases} l_x + 1, & 0 \le t < t_x \\ l_x, & t_x \le t \le T_{\rm sw} \end{cases}. \quad (27)$$

Fig. 3(a) illustrates an example of the switching. Therein, the modified duty cycle for phase x is shown along with the switching rules according to (27). The vertical lines represent the start of a DSP clock cycle. At that time, the duty cycle is computed as indicated by the dots. The switching level and time are calculated according to (25) and (26) and the switching state is scheduled according to (27). Note that the discrete computing of d_{xm} will result in a nonideal zero-order-hold effect. This effect is typically negligible if the DSP switching period is small compared to the change in the duty cycle. It should be pointed out that, in practice, there will be a one-sample-delay effect since the DSP will require time to process the duty cycle. This means that a duty cycle computed during one switching period is not available to be scheduled until the start of the next clock cycle. This effect is also negligible if the DSP switching period is small. The switching shown in Fig. 3(a) is sometimes referred to as left-justified PWM since the pulses are aligned

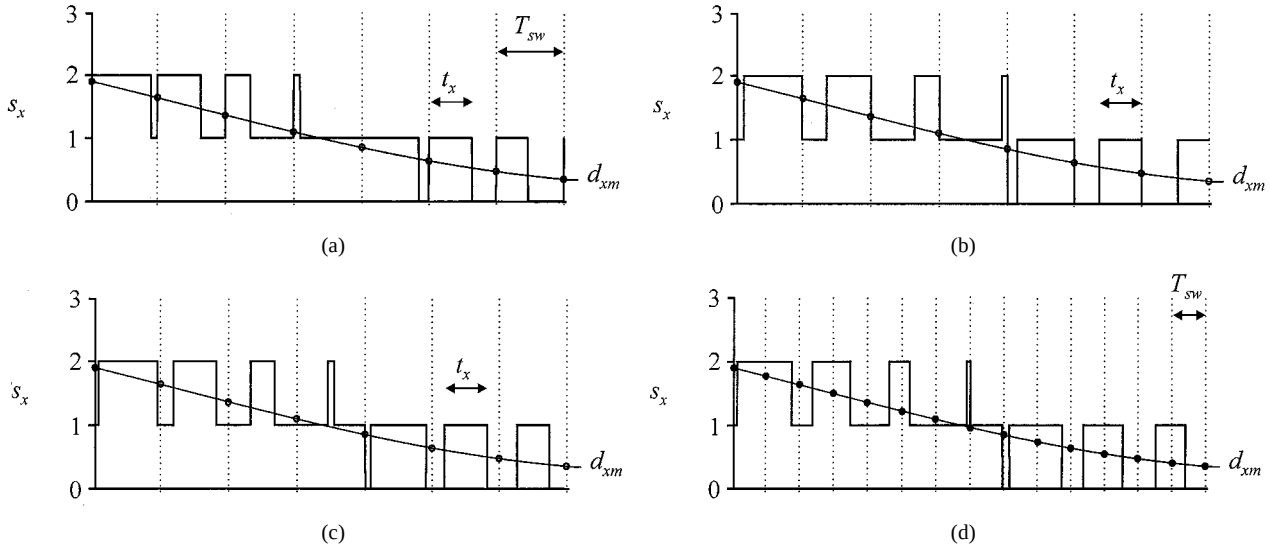

Fig. 3. Multilevel duty-cycle modulation technique. (a) Left-justified timer scheduling. (b) Right-justified timer scheduling. (c) Center-justified timer scheduling. (d) Alternate-justified timer scheduling.

with the left side of the DSP cycle. Right-justified PWM can also be scheduled by

$$s_x = \begin{cases} l_x, & 0 \le t < (T_{\rm sw} - t_x) \\ l_x + 1, & (T_{\rm sw} - t_x) \le t \le T_{\rm sw} \end{cases}. \tag{28}$$

Fig. 3(b) shows an example of right-justified PWM. For a more symmetrical waveform, center-justified PWM can be used. Using this method, the scheduling of the switching state is set according to

$$s_x = \begin{cases} l_x, & 0 \le t < \left(\dfrac{T_{\rm sw} - t_x}{2}\right) \\ l_x + 1, & \left(\dfrac{T_{\rm sw} - t_x}{2}\right) \le t < \left(\dfrac{T_{\rm sw} + t_x}{2}\right) \\ l_x, & \left(\dfrac{T_{\rm sw} + t_x}{2}\right) \le t \le T_{\rm sw}. \end{cases} \tag{29}$$

Fig. 3(c) demonstrates center-justified PWM. As can be seen, the DSP period has been set to twice that of the previous examples in order to keep the switching frequency constant. An even more symmetrical switching waveform can be achieved through alternate justification. This may be described by alternating between left and right justification. Fig. 3(d) shows an example of alternating justification.

C. Triangle Waveforms

The equivalence of the proposed method to sine-triangle modulating may be readily seen. Fig. 4 shows an example of the multilevel sine-triangle method [2]–[4]. Therein, three triangle waveforms are defined ($n - 1$ triangle waveforms in general) and the switching state rules are

$$s_x = \begin{cases} 0, & d_{xm} \le tr_1 \\ 1, & tr_1 < d_{xm} \le tr_2 \\ 2, & tr_2 < d_{xm} \le tr_3 \\ 3, & tr_3 < d_{xm}. \end{cases} \tag{30}$$

As can be seen from Fig. 4, the resulting switching state is the same as it would be with alternate justification if a zero-order hold is placed upon the modified duty cycle. Center-justified modulation may be achieved if the zero-order hold is extended for two switching cycles in Fig. 4. Left or right justification may be achieved if the triangle waveform is replaced with a sawtooth or reverse-sawtooth waveform, respectively.

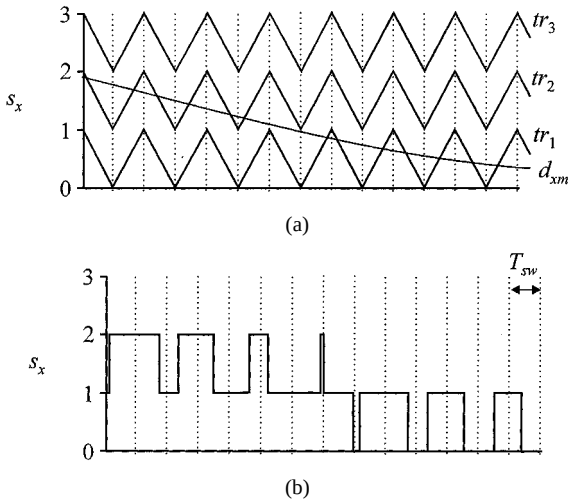

Fig. 4. Multilevel sine-triangle modulation. (a) Duty-cycle and triangle waveforms. (b) Resulting switching state.

D. Voltage Vectors

The voltage vectors of the proposed method will now be examined based on the previous definition of the overall switching state. Fig. 5 shows an example of the a-, b-, and c-phase switching states over one DSP switching period using the proposed method. For this example, the switching states start out as $s_a = 3$, $s_b = 2$, and $s_c = 1$. From (3), the overall switching state is $sw = 57$. On the vector plot of Fig. 2, this switching state is represented by v_{57}. Based on the times for each phase (t_a, t_b, and t_c), it can be seen that the c phase will have a transition first followed by the b phase, then the a phase. These three transitions uniquely define four windows in the DSP switching period indicated by I, II, III, and IV in Fig. 5.

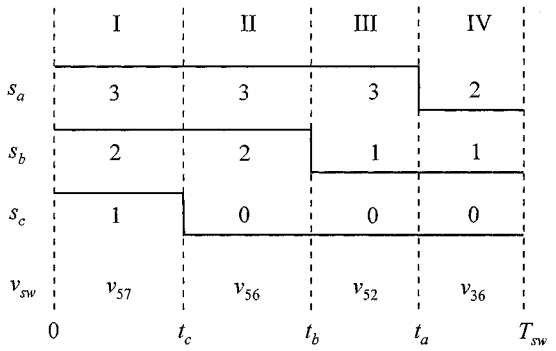

Fig. 5. Duty-cycle modulation voltage vectors.

Each window has a correspondingly unique switching state and voltage vector. In particular, for this example, the voltage vector sequence is $v_{57} \rightarrow v_{56} \rightarrow v_{52} \rightarrow v_{36}$. From the vector plot of Fig. 2, it can be seen that this results in a clockwise selection of the three-nearest voltage vectors (v_{57} and v_{36} being of redundant states). It should be noted that the nearest vectors and switching times are readily determined using the proposed method. The same result can be accomplished with SVM [5]–[8], but with awkward geometrical relationships. A reversal of the sequence in the voltage vectors can be accomplished by switching to right justification in the proposed method.

IV. Redundant State Selection

In multilevel power conversion, it is often necessary to utilize the redundant switching states for balancing of the voltages on input capacitor banks [11]. The idea is that if the capacitor voltages are nearly balanced, then the load voltage will be the same regardless of which redundant state is selected. For example, windows I and IV in Fig. 5 utilize switching states that produce the same voltage vector. In general, a redundant state may be found for a given switching state by incrementing or decrementing the states for all three phases since this results in changing the zero-sequence line-to-ground voltage, which does not affect the load voltages. Although the load voltages are the same regardless of the redundant switching state used, the resulting currents in the capacitors for a given topology are widely different. Therefore, the appropriate redundant switching state that results in improving the balance of the capacitor voltages may be selected when a choice arises.

As a matter of practical implementation, redundant states may be calculated offline and programmed into a programmable logic device (PLD) table [11]. Fig. 6 shows a block diagram of how this may be accomplished. Therein, the modulation is programmed in the DSP which output switching states, as described above, which are labeled s_a^*, s_b^*, and s_c^* to indicate desired switching states. These switching states along with the phase currents and the capacitor voltages are input to the PLD. An analog-to-digital conversion is performed on the phase currents and capacitor voltages in order to determine the current direction and the voltage imbalance [11]. This information along with the desired switching state forms the address of the redundant state selection (RSS) table. The table output is the switching states, which include capacitor voltage balancing information. It may be desirable to latch the analog inputs to

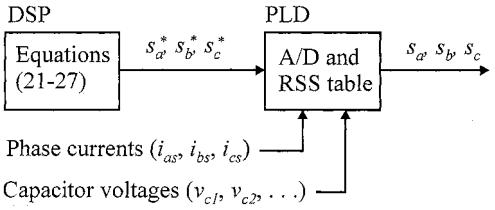

Fig. 6. Implementation of RSS using a PLD.

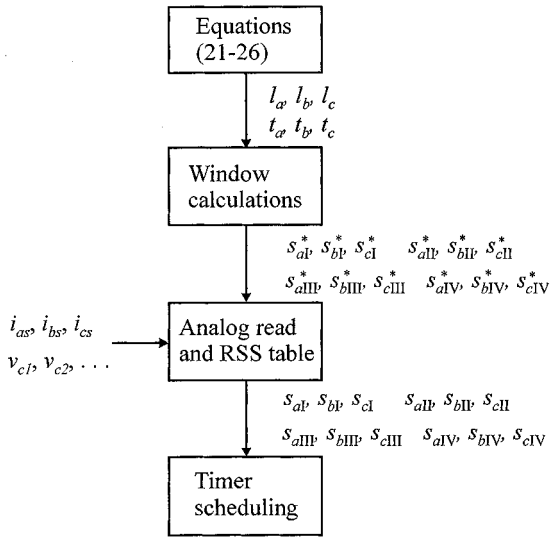

Fig. 7. Implementation of RSS using a DSP.

the PLD so that they align with the DSP switching period. This prevents changes in switching state during the DSP cycle due to changes in the analog inputs.

The RSS table may also be incorporated in the DSP. This is helpful for algorithms such as dead-time compensation where it is helpful to determine the final switching state within the processor. Fig. 7 shows a flowchart of the steps necessary to include the RSS table in the DSP. As can be seen, the desired switching states are computed for all four windows based on the level transitions of all three phases. Then, four RSS table lookups are performed in order to determine the redundant states for each window. The switching states along with the switching times may be scheduled by loading this information into a PLD.

V. Laboratory Results

A. Four-Level Rectifier/Inverter System

Fig. 8 shows a four-level back-to-back power conversion system which was used to validate the proposed modulation method. This system was constructed to mimic future naval ship propulsion systems, which include a synchronous generator, rectifier, and motor drive for propulsion. The details of the four-level rectifier and inverter will not be presented herein. The interested reader is referred to [17]. The four-level rectifier converts a 450 V 60 Hz source to a dc voltage, which is regulated to $v_{\rm dc}^* = 660$ V. The regulating control is a proportional plus integral (PI) control used to determine a commanded current magnitude based on the dc voltage error. Using the measured line voltages v_{ab} and v_{bc}, the commanded rectifier currents i_{ar}^* and i_{br}^* can be aligned with the source voltages so

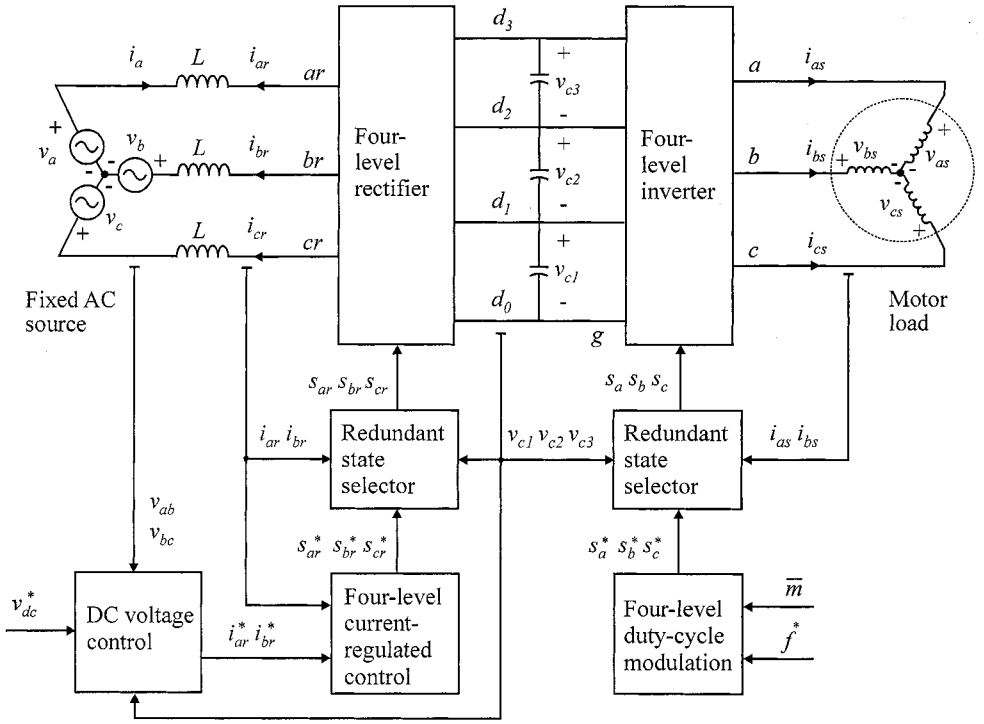

Fig. 8. Four-level rectifier/inverter system and associated control.

that unity power factor operation is ensured. These commanded currents are regulated by a hysteresis current control, the details of which are given in [9]. The resulting switching states are input to a four-level RSS table for capacitor voltage balancing. The reader is referred to [11] for the details of the RSS table. The inverter is controlled by a DSP using duty-cycle modulation as described herein with $\bar{m} = 0.9$ and a constant frequency of $f^* = 100$ Hz. The modulation electrical angle is then related to the commanded frequency by $\theta_c = 2\pi f^* t$. The DSP switching period for this study was $T_{\rm sw} = 200\ \mu$s and alternate-justification method was utilized. The redundant state selection for the inverter was identical to that of the rectifier. The motor load is an 18-kW induction motor, which is loaded by a synchronous generator.

Fig. 9 shows the four-level system performance. Therein, the motor phase voltage v_{as}, motor phase current i_{as}, source voltage v_a and source current i_a are shown. As can be seen, the motor voltage exhibits the typical four-level waveshape [5]. The phase current has exceptionally low harmonics due to the machine inductance. Unity power factor operation can be seen from the source voltage and current. Fig. 10 shows the capacitor voltages and the motor phase current during transient operation. In this study, the motor load is stepped from zero to rated. As can be seen, the rectifier control regulates the total dc voltage and the RSS switching ensures capacitor voltage balance.

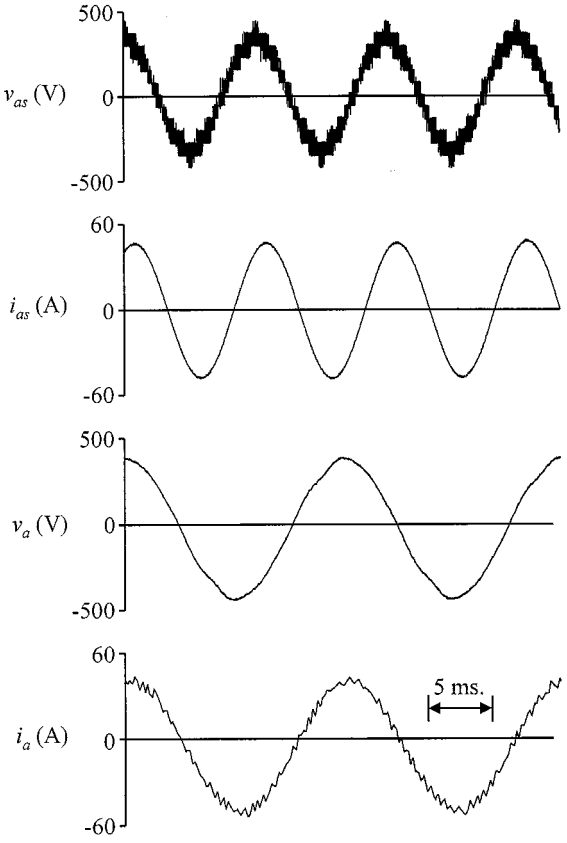

Fig. 9. Four-level system laboratory measurements.

B. 11-Level Cascaded Multilevel H-Bridge Inverter

As a demonstration of extension of the proposed modulation to other types of inverters, the method was also validated on an 11-level cascaded multilevel H-bridge inverter. Fig. 11 shows the specific topology for the a phase. As can be seen, the inverter is constructed of a five-level H-bridge cell in series with a three-level cell. Three phases were then wye connected and used to drive a 3.7-kW induction motor. The details of this inverter and capacitor balancing RSS table will not be included

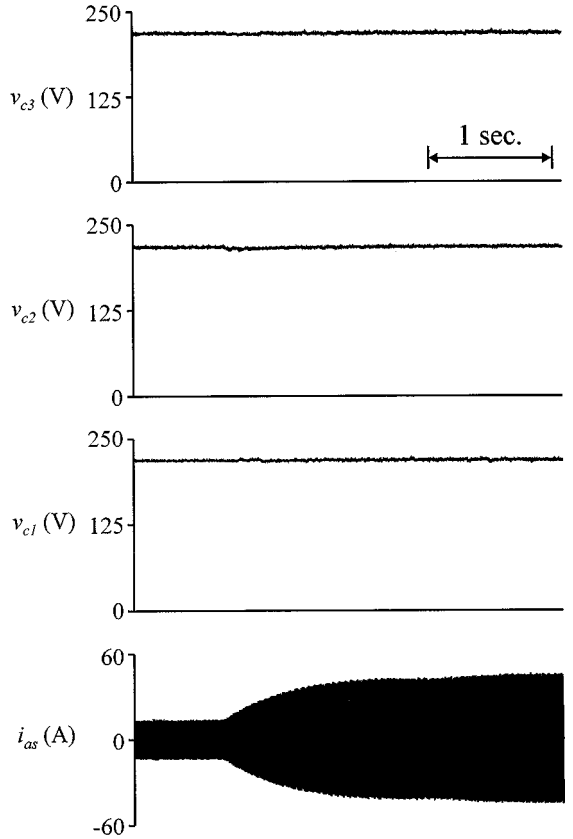

Fig. 10. Four-level system transient performance.

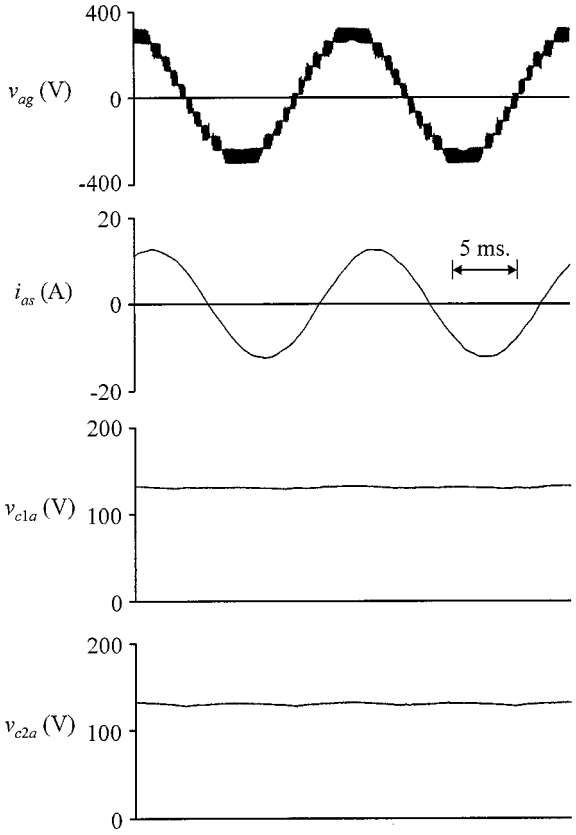

Fig. 12. 11-level inverter laboratory measurements.

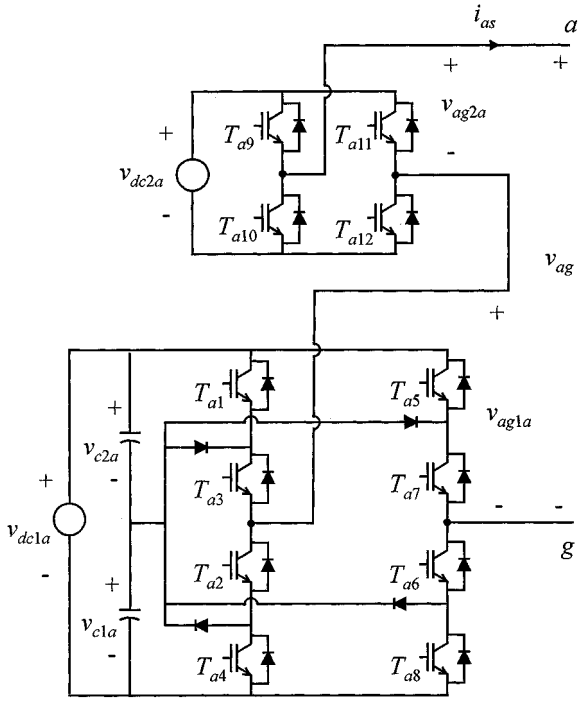

Fig. 11. 11-level cascaded inverter (a phase).

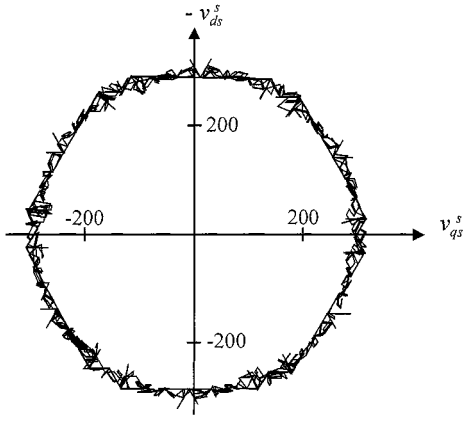

Fig. 13. 11-level utilized voltage vectors.

herein, but may be found in [18]. For this example, the modulation index and commanded frequency were set to $\bar{m} = 0.9$ and $f^* = 60$ Hz. The DSP switching period for this study was $T_{\rm sw} = 100$ μs and left justification was utilized. Fig. 12 shows the inverter line-to-line neutral v_{ag}, phase current i_{as}, and capacitor voltages v_{c1a} and v_{c2a}. The ac waveforms exhibit high power quality resulting form the high number of voltage levels. It can be seen that the capacitor voltages are effectively balanced through the RSS table. Fig. 13 shows the utilized voltage vectors for this study which were obtained by transforming the phase voltages to the synchronous reference frame [23]. As can be seen, the utilized vectors consist of the nearest available vectors which would be selected using SVM.

VI. Conclusion

A new multilevel modulation method was introduced. It was shown that the nearest voltage vector selection as well as the

PWM switching times can be directly determined from per-phase duty cycles. The method is discrete in nature and can be readily implemented on a DSP and is also expandable to any number of voltage levels. It was shown that the proposed scheme produces the same switching states at that of multilevel sine-triangle modulation and multilevel SVM. Inclusion of redundant state selection for capacitor voltage balancing is described. The method is implemented on a four-level back-to-back rectifier/inverter system, which was constructed to mimic naval ship propulsion systems. The method was also implemented on an 11-level cascaded H-bridge inverter.

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