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Multimode Silicon Nanowire Transistors

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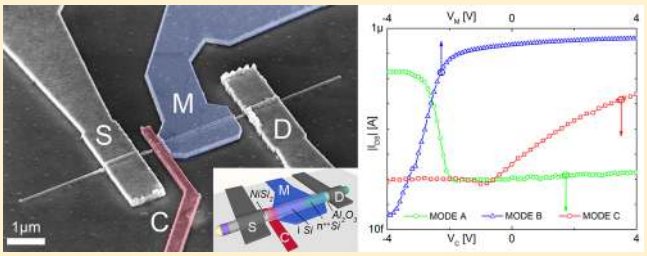
Supporting Information

ABSTRACT: The combined capabilities of both a nonplanar design and nonconventional carrier injection mechanisms are subject to recent scientific investigations to overcome the limitations of silicon metal oxide semiconductor field effect transistors. In this Letter, we present a multimode field effect transistors device using silicon nanowires that feature an axial n-type/intrinsic doping junction. A heterostructural device design is achieved by employing a self-aligned nickel-silicide source contact. The polymorph operation of the dual-gate device enabling the configuration of one p- and two n-type transistor modes is demonstrated. Not only the type but also the carrier injection mode can be altered by appropriate biasing of the two gate terminals or by inverting the drain bias. With a combined band-to-band and Schottky tunneling mechanism, in p-type mode a subthreshold swing as low as 143 mV/dec and an ON/OFF ratio of up to 10^4 is found. As the device operates in forward bias, a nonconventional tunneling transistor is realized, enabling an effective suppression of ambipolarity. Depending on the drain bias, two different n-type modes are distinguishable. The carrier injection is dominated by thermionic emission in forward bias with a maximum ON/OFF ratio of up to 10^7 whereas in reverse bias a Schottky tunneling mechanism dominates the carrier transport.



KEYWORDS: *Silicon nanowire, reconfigurable transistor, dual-gate, Schottky barrier tunneling, band-to-band tunneling, nickel silicide*

The continuous advance in information technology over the last decades is mainly attributed to the complementary metal oxide semiconductor (CMOS) technology and the excellent scalability of its key component: the metal oxide semiconductor field effect transistor (MOSFET). However, further miniaturization of conventional MOSFET structures faces insurmountable limitations with characteristic dimensions reaching the sub-10 nm regime. The main problem is 2-fold. First, the fundamental room-temperature limit of the subthreshold swing results in enhanced leakage currents, and second, short channel effects (SCEs), which further increase the leakage currents become more prominent for ultimately scaled devices. To overcome these limitations novel device architectures, materials, new physical concepts, or ways of logic operation must be exploited so that future devices continue to comply with Moore's law.

Nonplanar device architectures like trigated FinFETs have already been successfully introduced into recent large-scale integrated device fabrication.[1] Nanowires are promising candidates to succeed FinFET technology. Thelander et al.[2] denoted nanowire devices as an add-on to mainstream Si technology and according to Appenzeller et al.[3] they feature the right combination of excellent gate control, fast switching, high on-currents, and low off-currents. The superior electrostatic control of the channel conductivity can be closely related to the gate geometry and the high surface-to-volume ratio of nonplanar devices. Trigate-, Ω-shaped-, or even gate-all-around-structures that can be realized using nanowires furthermore lower the impact of SCEs.[4]

Besides the benefits induced by geometric properties of quasi 1D nanowire structures, alternative current transport mechanisms, which are also referred to as carrier injection mechanisms, have been investigated to complement CMOS technology. Recent publications describe devices based on impact ionization,[5,6] band-to-band tunneling,[7,8] or Schottky barrier tunneling.[9,10] Tunneling FETs (TFETs) and impact ionization FETs (IIFETs) are steep slope switching devices as their dynamic performance is not limited by thermionic emission. Hence, subthreshold swing (SS) values lower than the MOSFET room temperature limit of 60 mV/dec are achievable. IIFETs have the smallest SS values, but hot carrier injection degrades the reliability of such devices.[6] With TFETs, it is still challenging to realize high drive currents,[11] although adapted structures with improved on-currents that make use of a combined tunneling mechanism have been proposed recently.[12] In addition, conventional TFETs exhibit ambipolar conduction that prevents a complementary design. Le et al.

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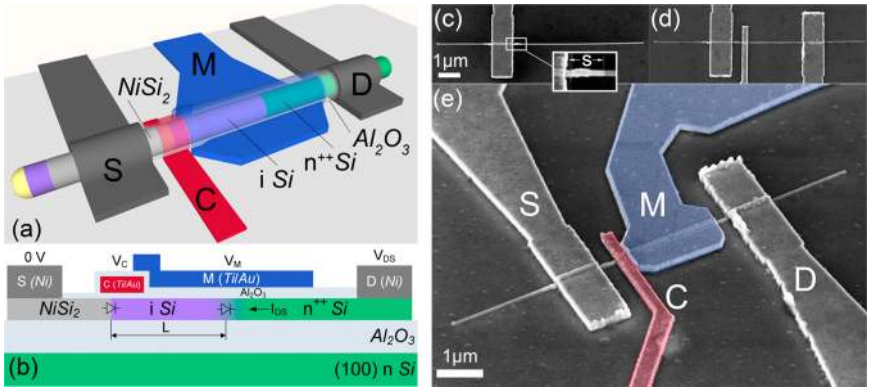

Figure 1. (a) Schematic illustration of the multimode nanowire heterostructure device. A $NiSi_2$ Schottky tunneling source (S) is formed at the intrinsic part of the nanowire whereas an ohmic drain (D) contact is formed at the highly n-doped region of the nanowire. The C-gate (C) is placed directly above the silicide-to-intrinsic Si junction. The M-gate (M) partly overlaps the C-gate, the intrinsic nanowire partition and about half of the n-type doped nanowire partition. The device is passivated with Al_2O_3, which is simultaneously used as gate oxide. (b) Schematic cross-section of the device along the nanowire. The effective channel length (L) is determined by the intrinsic section's length. (c–e) Scanning electron micrographs (SEMs) of the device during individual stages of the device integration. (c) Formation of the self-aligned $NiSi_2$ source contact in a 35 s rapid thermal annealing step at 510 °C in forming gas atmosphere. The inset magnifies the silicide region, and the silicide intrusion length (s) of this specific device equals 470 nm. (d) Fabrication of the ohmic drain contact and C-gate formation in the vicinity of the silicide-to-silicon junction. (e) Tilted view of the fully featured device with the C- and M-gate highlighted. The nanowire has a diameter of 67 nm, the source and drain contact separation length is 3.2 μm and the width of the C-gate is 280 nm.

circumvented ambipolarity by introducing a SiGe nanowire heterostructure[13] and Knoll et al. suggested asymmetric source and drain doping.[14] Schottky barrier tunneling FETs (SBTFETs) can be realized with metal or metal-like contact materials onto Si substrates.[15] Thereby contact properties are mainly determined by the semiconductor type and doping, the material used for the contacts, and the interface quality. Jhaveri et al.[10] suggested that the SS of an SBTFET, which employs nickel silicide as a tunneling source, is still limited to a minimum of 60 mV/dec at room temperature. However, the influence of the temperature on the SS is weak compared to conventional MOSFETs, which implies improvement of the SS at higher operational temperatures. On the basis of Schottky barrier tunneling and gated contact regions, reconfigurable nanowire transistors for a new type of logic operations have been recently introduced.[16,17]

The multimode device presented in this work is based on Si nanowires that feature an axial n-type/intrinsic (n^{++}/i) doping junction and a self-aligned, quasi-metallic $NiSi_2$ contact forming an atomically sharp Schottky junction,[18] which increases the electrostatic controllability of the contact region.[19] The Schottky barrier height of this material combination has been studied in previous works[20−22] to range from 0.63 to 0.79 eV. The polymorph functionality of the proposed device is based on a dual-gate structure, whereby the control-gate (C-gate) controls the carrier injection at the Schottky tunneling source and the modulation-gate (M-gate) modulates the bands in the intrinsic channel region. Figure 1a depicts a schematic illustration of the fully featured dual-gate device with the C-gate covering the silicide-to-silicon junction and the M-gate expanding partly over the C-gate, the intrinsic nanowire partition, and the n-type/intrinsic doping junction. Figure 1b shows the respective schematic cross-sectional view.

The vapor−liquid−solid (VLS) growth[23] as well as the in situ doping of the nanowires used for device implementation was accomplished in a low-pressure chemical vapor deposition system. The untapered nanowires[24] were grown in such a way that they feature a significant axial n^{++}/i doping profile with a sharp transition region close to the axial center.[25] The typical total growth length was 10 μm with nanowire diameters ranging from 58 to 120 nm. The fabrication of source and drain contact was accomplished subsequently in two separate steps. With this approach, first the self-aligned $NiSi_2$ Schottky tunneling source contact was formed in a rapid thermal annealing (RTA) step (Figure 1c) followed by the drain contact that remained unannealed (Figure 1d). This one-sided silicidation process emerged as markedly beneficial considering the ohmic properties of the drain contact.

For device performance optimization, particularly with respect to the on-currents, the nanowires were characterized to assess the general geometrical and electrical properties of the highly n-doped and intrinsic sections before and after the silicidation. The nanowires were contacted in multiterminal configurations with up to eight Ni pads. Four-terminal measurements conducted at the highly n-doped part allowed to calculate the resistivity and to estimate the impurity concentration by comparison with bulk Si values. The effective impurity concentration was calculated to about 1.66×10^{19} cm^{-3} with the average contact resistance being 12.52 kΩ. The nanowires were subsequently annealed for 15 s at 510 °C in forming gas atmosphere to intrude the contacts. It has been shown that at such conditions $NiSi_2$ develops as dominating interfacial nickel silicide stoichiometry.[26,27] Figure 2a depicts the results gained by averaging the silicide intrusion lengths (s) of 32 individual nanowires. The nanowires comprised different contact configurations; however, the averaging was performed from at least four intruded silicide segments. The average intrusion length decreased quite linearly with increasing nanowire diameter. Similar findings have been reported for the intrusion of Ni_2Si into Si nanowires that forms at lower temperatures.[28] Further investigations showed that the influence of the doping onto the silicidation process was negligible. In Figure 2b, the intrinsic and highly n-doped sections of three individual nanowires with different diameters are compared. Average values of s are in good agreement for both section types.

From $I-V$ characteristics measured at both, intrinsic (Figure 2c) and highly n-doped (Figure 2d) sections, before and after

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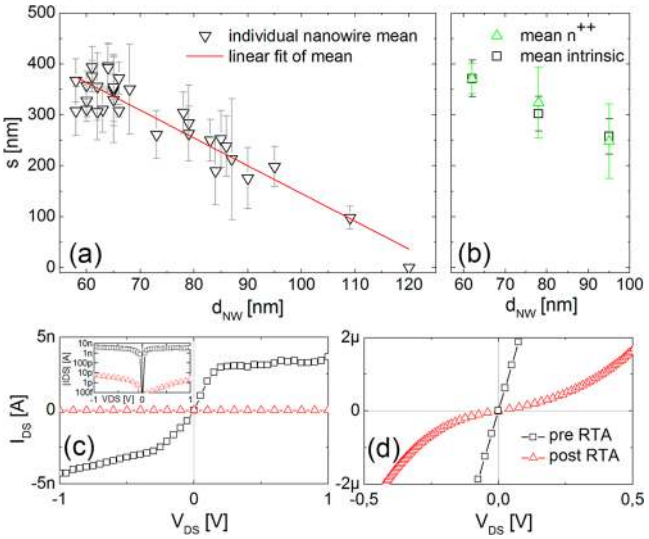

Figure 2. Properties of the silicidation process. The Ni contacts were annealed for 15 s at 510 °C in forming gas atmosphere. (a) Dependence of the average silicide intrusion length on the nanowire diameter. (b) Dependence of the average silicide intrusion length on the impurity concentration. The average values of both, intrinsic and highly n-doped part were extracted from the same individual nanowire for a total number of three nanowires with diameters of 62, 78, and 95 nm. Error bars of (a) and (b) indicate ±1 standard deviation. (c,d) Comparison of *I*–*V* curves before (black, squares) and after (red, up-triangle) the RTA process at zero back-gate voltage for intrinsic nanowire sections (c) and highly n-doped sections (d). The inset of (c) depicts the *I*–*V* curve of the intrinsic section in a semilogarithmic representation.

the silicidation, it was found that the silicidation significantly degraded the contact resistance. The resistivity of the nanowire segment is expected to remain unchanged; therefore, the increased total resistance is attributed to the contact resistance. A more than 10-fold increase of the total resistance can be noticed by comparing the two *I*–*V* curves, measured at the highly n-doped section of the same nanowire segment prior and after the silicidation process. The resistance extracted from the steepness of the *I*–*V* curve prior to the silicidation was 40.33 kΩ whereas the post-RTA resistance was found to be 577.98 kΩ. For that reason, a one-sided silicidation process was implemented in the final device design, which only considers the annealing of the intrinsic side of the nanowire. This basic nanowire structure was then passivated with a 10 nm layer of Al_2O_3 formed by atomic layer deposition. In two final steps, first the C-gate was structured followed by the M-gate. The two Ti/Au gate terminals were separated with 10 nm of Al_2O_3 resulting in a total gate oxide thickness of 20 nm in the channel region. Scanning electron micrographs (SEMs) after the formation of the C-gate and of the final device are shown in Figure 1d,e, respectively. A detailed description of the fabrication process can be found in the Supporting Information.

The transfer characteristics in Figure 3 demonstrate the multimode capability of a typical dual-gate nanowire device. The corresponding band schemes visualizing the on- and off-state as well as the respective terminal configurations for the three different modes (A–C) are shown aside.

The normally off p-type behavior of the device in mode A (Figure 3; green, circles) is a result of electrostatically modulated, combined band-to-band and Schottky barrier tunneling. In this mode, the nanowire device is biased in forward direction, that is, a negative drain-to-source voltage is applied, and the M-gate is set to −4 V. In this configuration, the barrier at the doping interface is thin so that band-to-band tunneling of electrons close to the n^{++}/i junction is enabled if holes are available in the channel region. Thus, by controlling the injection of holes from the source via Schottky barrier tunneling with the C-gate, the overall on-current is a result of the recombination current. The threshold voltage V_{TH}, derived by linear extrapolation at the maximum transconductance, was

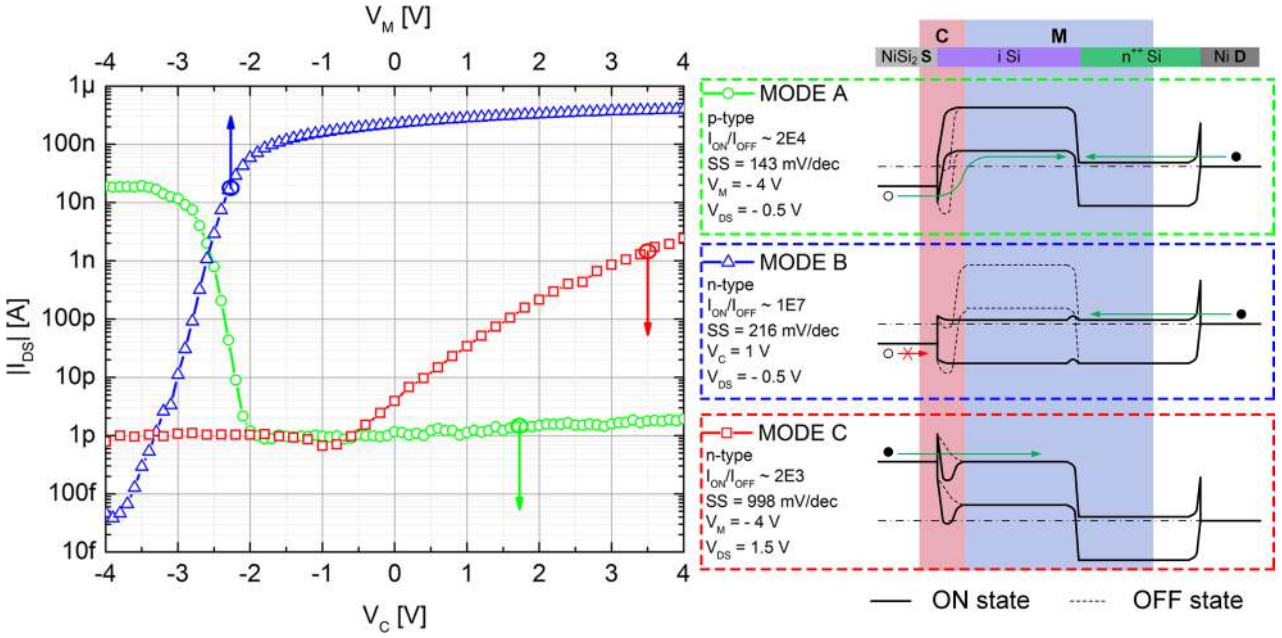

Figure 3. Transfer characteristics, corresponding band schemes, gate and drain terminal configurations of mode A–C. Mode A (green, circles) is dominated by combined band-to-band and Schottky barrier tunneling, mode B (blue, triangles) by thermionic emission, and mode C (red, squares) by combined Schottky barrier tunneling and thermionic emission.

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found to be −2.55 V. The maximum ON/OFF-ratio of 2×10^4 and the minimum SS of 143 mV/dec were extracted at V_{DS} = −0.5 V. The maximum on-current is 20 nA (which equals a current density of 0.57 kA/cm^2) while the off-current is about 1 pA. Figure 4a depicts the sensitivity of mode A onto the drain bias. Both, on- and off-currents increase with increasing drain bias due to enhanced thermionic emission of holes from the source over the barrier at the n^{++}/i doping junction. Figure 4b depicts the influence of the M-gate onto the C-gate transfer characteristics. Increasing on-currents with increasing V_M in the on-state of the device indicate a transition of the injection mechanism from combined tunneling to thermionic emission of electrons from the quasi-ohmic drain. The transition is further verified as the device cannot be switched off anymore by blocking the hole-injection via the C-gate if V_M reaches about −2 V.

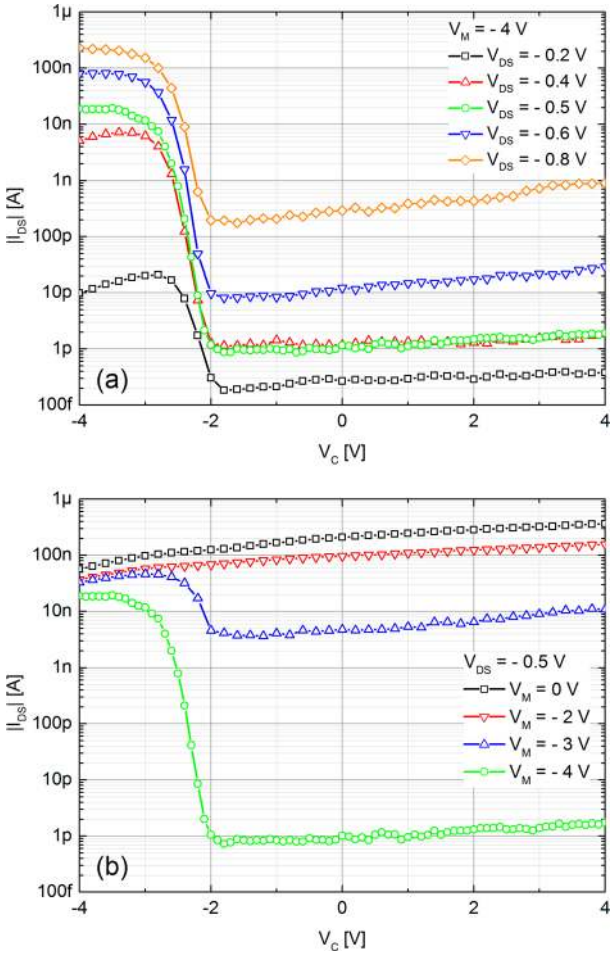

Figure 4. Transfer characteristics properties of mode A (green, circles). (a) Dependence on the drain bias at V_M = −4 V. (b) Influence of the M-gate voltage (V_M) at V_{DS} = −0.5 V. A transition of the injection mechanism from combined Schottky and interband tunneling to thermionic emission can be observed between V_M = −4 and V_M = −2 V.

By changing the gate configuration, i.e., by applying 1 V at the C-gate and by sweeping the M-gate, while preserving the forward drain bias (V_{DS} = −0.5 V), the device exhibits normally on n-type behavior. This mode is dominated by thermionic emission (mode B in Figure 3; blue, triangles). With V_C = 1 V the hole injection from the source is always blocked which prevents band-to-band tunneling. Hence, in contrast to mode A, the device is in off-state for sufficient negative V_M with the threshold voltage being V_{TH} = −2.45 V. At higher V_M the barrier at the n^{++}/i interface is low enough to enable thermionic emission of electrons from the drain. A noteworthy high on/off-ratio of up to 10^7 and a SS of 216 mV/dec are achieved at V_{DS} = −0.5 V. The maximum on-current is 0.4 µA (11.23 kA/cm^2) the off-current is less than 50 fA.

Finally, in mode C (Figure 3; red, squares) the device is operated as an n-type transistor. By preserving the same gate-configuration like in the p-type mode A, the operational mode is changed just by inverting the drain-bias. Thereby the injection mechanism in reverse bias is expected to be dominated by combined Schottky barrier tunneling and thermionic emission. At a drain voltage of 1.5 V, both the barrier height and width are controlled via the C-gate; the M-gate just slightly influences the transfer characteristics. The maximum on-current is 2.5 nA (71×10^{-3} kA/cm^2) and the off-current is about 1 pA. For this operational mode the SS of about 998 mV/dec and an ON/OFF ratio of about 2×10^3 appear to be rather moderate.

In conclusion, we have shown the independence of the average silicide intrusion length onto the impurity concentration and that the silicidation process degrades the contact resistance in both, intrinsic and highly n-doped sections. Nevertheless, the $NiSi_2$ tunneling source formation emerged as markedly beneficial, considering the superior electrostatic and geometric properties. On the basis of these results, the integration of a multimode transistor based on a Si nanowire heterostructure that features an n^{++}/i doping junction and a $NiSi_2$ Schottky tunneling source has successfully been demonstrated. The unique device dynamically configures the mode of operation by either changing the dual-gate configuration or just by inverting the drain bias, that is, the modulation of a single signal is sufficient to program the device as n- or p-type transistor. A total number of three modes has been identified that can be distinguished with reference to the dominating current transport mechanism. In all modes investigated, an effective suppression of ambipolar behavior is obtained.

■ ASSOCIATED CONTENT

Supporting Information

Detailed description of the experimental procedures. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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