

# Multi-objective Modulated Model Predictive Control for a Multilevel Solid State Transformer

Luca Tarisciotti\*, Pericle Zanchetta,  
Alan Watson, Pat Wheeler, Jon Clare

Department of Electrical and Electronic Engineering  
University of Nottingham  
Nottingham, UK

\* [luca.tarisciotti@nottingham.ac.uk](mailto:luca.tarisciotti@nottingham.ac.uk)

Stefano Bifaretti

Department of Electronic Engineering  
University of Rome Tor Vergata  
Rome, Italy

**Abstract**— Finite Control Set Model Predictive Control (FCS-MPC) offers many advantages over more traditional control techniques, such as the ability to avoid cascaded control loops, easy inclusion of constraint and fast transient response of the control system. This control scheme has been recently applied to several power conversion systems, such as two, three or more level converters, Matrix converters, etc. Unfortunately, because of the lack of presence of a modulation strategy, this approach produces spread spectrum harmonics which are difficult to filter effectively. This may result in a degraded power quality when compared to more traditional control schemes. Furthermore, high switching frequencies may be needed, considering the limited number of switching states in the converter. This paper presents a novel multi-objective Modulated predictive control strategy, which preserves the desired characteristics of FCS-MPC but produces superior waveform quality. The proposed method is validated by experimental tests on a seven level Cascaded H-Bridge Back-To-Back converter and compared to a classic MPC scheme.

## I. INTRODUCTION

Model Predictive Control (MPC) has been widely proposed as a promising solution for the control of power converters. In fact it presents several advantages, such as fast dynamic response, absence of a modulation scheme, the possibility of incorporating nested control loops in only one loop and flexibility to include other system requirements in the controller algorithm [1]–[4]. MPC considers a model of the system in order to predict its future behaviour over a time horizon. Based on this model, MPC solves an optimization problem where a sequence of future actuations is obtained by minimizing a cost function, which represents the desired behaviour of the system. The best performing converter state is then applied and all the calculations are repeated every sample period. Several approaches are possible to implement a Model Predictive Control on a modern power electronic converter, such as Continuous Control Set Model Predictive Control (CCS-MPC), which iteratively calculate the minimum value of the selected cost function [5], or Explicit MPC, which analytically solve the cost function minimization problem [6]–[8]. Both these approaches take advantage of a suitable modulation technique to apply the desired voltage demand to the converter. However, since power converters are

systems with a finite number of states, the MPC optimization problem can be simplified and reduced to the prediction of the behaviour of the system for each possible state [2]. The latter approach, called Finite Control Set Model Predictive Control (FCS-MPC), has been successfully applied for the current control in three-phase inverters [4], Cascaded H-Bridge Converters (CHBs) [9] and Matrix converters [10], as well as power control in an active front end rectifier [11], and torque and flux control of an induction machine [12], [13]. However, the lack of a modulator is, unfortunately, also one of the main drawbacks of FCS-MPC considering that the control can choose only from a limited amount of converter states. This usually results in a variable switching frequency, between zero and the sampling frequency, dependant from system parameters and load conditions. Moreover, FCS-MPC is forced to produce pulses with a width multiple of the sampling interval resulting in a degradation of the converter output voltage THD, especially when compared to a PWM technique which is able to produce pulses with a width much smaller than the sampling time. More advanced schemes which include modulation techniques inside the FCS-MPC algorithm have been proposed [14]–[17]. In [14] FCS-MPC current control is applied to a six-phase inverter feeding an Asymmetrical Dual Three-Phase Induction Machine while in [15] a Predictive Direct Power Control is applied to a three-phase voltage source converter. In [18] a Predictive Direct Torque Control (P-DTC) approach is described. In all these study cases, the duty cycles are calculated by solving an optimisation problem. This approach determines the optimal control action in order to track the desired reference with minimal error. Multi-objective control can become rather complex since a solution to a multidimensional optimisation problem must be found. In order to overcome these limitations, a novel approach, named Modulated Model Predictive Control (M<sup>2</sup>PC), has been recently proposed; it retains all the mentioned desired characteristics of MPC as multi-objective control strategy, but produces great improvements in power quality performance. M<sup>2</sup>PC has already been introduced for the current control of a 3-Phase, 2-Level Active rectifier in [19] and for the current control of a single phase, 7-Level Cascaded H-Bridge Back-To-Back converter in [9], [20], in comparison with Dead-Beat and Model Predictive Control. In order to extend the control in [9],

[20] for the case of multi-objective control, in this paper M<sup>2</sup>PC is applied and tested for the case of the AC current and DC-Link voltage control of a grid connected 7-Level, 3-Phase Cascaded H-Bridge Back-To-Back converter.

## II. CONVERTER DESCRIPTION

The 7-Level, 3-Phase Cascaded H-Bridge Back-To-Back converter schematic is described in Figure 1 where each bidirectional AC/DC/AC cell of the converter is composed of two H-bridge and a medium frequency isolated DC/DC converter.

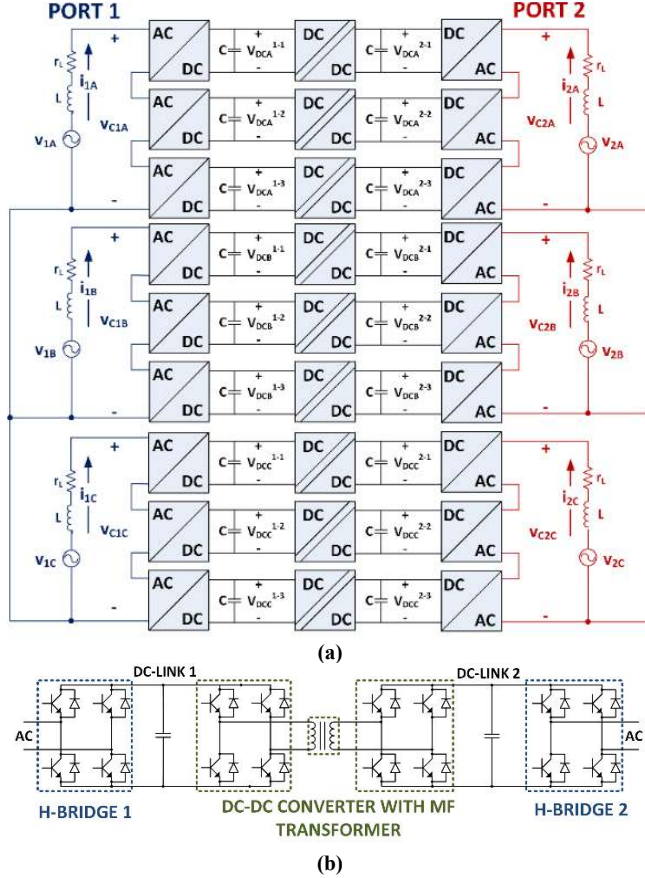


Figure 1. 3-Phase, 7-Level CHB Back-To-Back converter: (a) Overall structure, (b) Single AC/AC cell structure.

A series inductive input filter,  $L$ , with its inherent winding resistance  $r_L$ , is included to facilitate power flow from the grid and provide an acceptable attenuation of current harmonics. In a symmetrical converter, each cell is connected to a voltage source with  $V_{DC}=E$  and can produce three voltage levels, associated, respectively, to states  $-1$ ,  $0$  and  $1$ . Therefore, an  $n$ -cell cascaded converter can produce  $2n+1$  voltage levels on the AC side. Considering a 3-cell symmetrical converter, the output voltage on each phase is composed of seven different voltage levels, which can be produced by one or more combinations of H-Bridge states. Three indices are used to identify each HB, where  $p$  is the phase,  $h$  is the port connected to the selected HB and  $j$  defines which HB of the CHB is considered. As an example,  $s_A^{1-3}$  defines the state of the third

HB of the converter port 1, phase A. On the DC side the DC/DC converter has an independent control, described in [21], with the goal of achieving the same voltage on both side of the converter (or scaled by the transformer turns ratio), thus its dynamic is not considered in the model derivation. However, it has to be remembered that, in practical implementations, the active power reference variation rate must be limited in order to avoid excessive DC-Link voltage excursions. The switching model of the converter is obtained by approximating the DC/DC converter as a capacitor,  $C$ , and a resistance  $R_C$ , which represent the losses in the DC-Link circuit and DC/DC converter. It is important to highlight that  $R_C$  represents an unknown model parameter and for this reason, its effect cannot be taken into account in the control design. The model is described by the following system of equations, where the DC-Link voltage,  $V_{DCp}^j$ , and AC currents  $i_{hp}$  define the state of the system. The converter AC voltages,  $v_{chp}$ , and the DC-Link capacitor currents,  $I_{chp}$ , are also defined in (1).

$$\left\{ \begin{array}{l} \frac{di_{hp}}{dt} = \frac{1}{L}[v_{hp} - v_{chp}(t)] - \frac{r_L}{L}i_{hp} \\ \frac{dV_{DCp}^j}{dt} = \frac{1}{C}I_{chp} - \frac{1}{R_C C}V_{DCp}^j \\ V_{chp} = \sum_{j=1}^3 s_p^{h-j} V_{DCp}^j \\ I_{chp} = \sum_{h=1}^2 s_A^{h-j} i_{hp} \\ h = 1,2,3, \quad p = A, B, C, \quad j = 1,2,3 \end{array} \right. \quad (1)$$

For control design purposes an equivalent DC model for each phase is derived. The total DC-Link voltage on each phase,  $V_{DCp}$ , defined as the sum of the voltages on the DC-Link capacitors, is considered, under the assumption that the converter is symmetrical, in (2) where  $s_{hp}$  represents the sum of the H-Bridge states on port  $h$ , phase  $p$ .

$$s_{1p}i_{1p} + s_{hp}i_{2p} = C \frac{dV_{DCp}}{dt} - \frac{V_{DCp}}{R_C} \quad (2)$$

## III. MODULATED MODEL PREDICTIVE CONTROL

Modulated Model Predictive Control (M<sup>2</sup>PC) includes a suitable modulation scheme in the cost function minimization of the MPC algorithm. In this paper a modulation scheme particularly suitable for high power converter control is implemented in M<sup>2</sup>PC. At every sampling period, only one leg of a single HB is allowed to switch, obtaining a total switching frequency of the CHB that is half of the sampling frequency [22], [23]. This modulation approach equally distributes the commutations amongst the HB modules and, in the case of a 7-Level CHB converter, allows to obtain a device switching frequency equal to one sixth of the sampling frequency. This feature becomes rather important when high power

applications are considered. Moreover, the selected switching pattern helps to reduce the controller computational requirements. As a result, two converter states are selected by the controller. The first one is selected to be the voltage vector applied at the end of previous sampling interval, while the second one is selected between the two states adjacent to the first selected converter state, using a predictive cost function minimization algorithm. A combination of these two converter states is applied during the next sampling interval, where preference is given to the one associated with a lower cost function value. The control for this specific application is described in the following subsections. The overall M<sup>2</sup>PC scheme is shown in Figure 2, where the modulation scheme is integrated in the controller as described above.

#### A. Control references calculation

The aim of the proposed method is to control the AC current and the DC link voltages at the required references, and to obtain the desired active and reactive power flow through the converter, calculated using the following set of equations.

$$\begin{cases} i_{hp,k+n}^* = i_{hp,k+n}^{AC*} + i_{hp,k+n}^{DC*} \\ i_{hp,k+n}^{AC*} = \frac{(P_h^*/3) \sin(\theta_{hp} + nT_s - \varphi_{hp})}{\sqrt{2} \cos(\varphi_{hp}) V_{hp,rms}} \\ i_{hp,k+n}^{DC*} = \frac{P_{DCp,k+1} \sin(\theta_{hp} + nT_s - \varphi_{hp})}{\sqrt{2} \cos(\varphi_{hp}) V_{hp,rms}} \\ \varphi_{hp} = \text{atan}\left(\frac{P_h^*/3 + P_{DCp,k+1}}{Q^*/3}\right), n = 1,2 \end{cases} \quad (3)$$

The desired current references are calculated from (3) based on the active power reference,  $P_h^*$ , the reactive power reference,  $Q_h^*$ , the angle  $\theta_{hp}$  and RMS value  $V_{hp,RMS}$ , of the AC voltage, provided by a PLL [24]. Furthermore, the necessary amount of power required to regulate the DC-Link voltage at

the desired value,  $P_{DCh,k+1}$ , is considered in the current references calculation using the following equation.

$$P_{DCp,k+1} = P_{DCp,k} + \frac{1}{2}C[V_{DCp,k}^{*2} - V_{DCp,k}^2] \quad (4)$$

A single phase PLL is implemented on each phase, using the Second Order Generalized Integrator, described in [25], and the three phase PLL, described in [26]. It is important to note that equation (4) does not consider the losses in the DC circuit, modeled by  $R_c$ , and the steady state error is reduced using the DC-Link voltage control in the predictive algorithm. The DC-Link voltage reference calculation is limited by a ramp variation in order avoid interactions with the dynamics of the current control and undesired distortion on the grid current. A factor  $N$ , representing the DC-Link voltage reference horizon, is used for this purpose, as described by equation (5).

$$V_{DCp,k}^* = V_{DC}^* + \frac{V_{DC}^* - V_{DCh,k}}{N} \quad (5)$$

M<sup>2</sup>PC requires the prediction of the supply voltage,  $v_{hp}$ , that is obtained from previous periods as described in [1], assuming ideal supply operating conditions. Once the converter state and switching instants are calculated by M<sup>2</sup>PC, a combination of the HB states is applied to produce the desired converter state. The HB selected to switch is determined by a set of iterative rules with the aim of maintaining balanced DC-Link capacitors voltages, and distributing the commutations amongst the HBs whilst minimizing the overall switching frequency. It should be noted that the M<sup>2</sup>PC state selector follow the same rules of the modulator with active voltage balancing algorithm, described in [23].

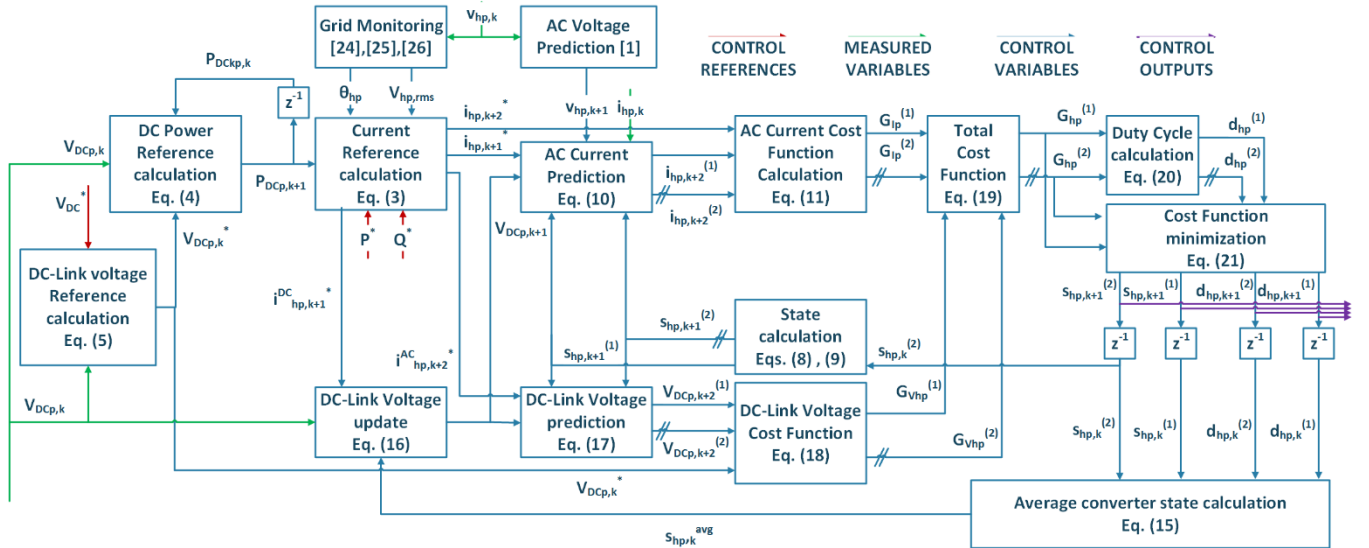


Figure 2. Overall M<sup>2</sup>PC block scheme for the control of port  $h$ , phase  $p$  of the proposed CHB back-to-back converter.

## B. Current control

The 2<sup>nd</sup> order derivative discretization of (6) is applied to the AC current equation in (1), to obtain the discrete time model in (7).

$$\left. \frac{di_{hp}}{dt} \right|_{t=t_k} = \frac{i_{hp,k+1} - i_{hp,k-1}}{2T_s} \quad (6)$$

$$v_{hp,k} - s_{hp,k+1}V_{DCp,k} = \frac{L}{2T_s} [i_{hp,k+1} - i_{hp,k-1}] - r_L i_{hp,k} \quad (7)$$

The AC system described by (4) represents an approximated discretization of the first equation in (1), which considers a constant dynamics of the system for two sampling intervals. This approximation is used in order to improve the control robustness with respect to noise on the measurements. At every sampling instant, two converter output vectors are selected by the control algorithm. The first vector  $s_{hp}^{(1)}$  is the same one applied at the end of the previous sampling interval as shown in (8).

$$s_{hp,k+1}^{(1)} = s_{hp,k}^{(2)} \quad (8)$$

The second vector  $s_{hp}^{(2)}$  is chosen between the two vectors adjacent to  $s_{hp}^{(1)}$  by the cost function minimization algorithm, as shown in (9).

$$s_{hp,k+1}^{(2)} = s_{hp,k+1}^{(1)} + s, \quad s = -1, 1 \quad (9)$$

By assuming that the control is operating correctly achieving an optimal current tracking, it is possible to approximate the term related with the inductor resistance  $r_L$  using the current reference instead of the current prediction at the instant  $t_k + T_s$ , incurring a negligible error. This approximation is used to reduce the controller computational effort. In fact, considering also that  $r_L$  is in the order of m $\Omega$  (inductive line filter) the error introduced by this approximation can be considered negligible in any operating condition. Using this approximation a two-step ahead current prediction is then obtained for both  $v_{Chp}^{(1)}$  and  $v_{Chp}^{(2)}$  as in (10) and used to calculate the relative cost function defined in (11).

$$i_{hp,k+2}^{(v)} = i_{hp,k} - \frac{2T_s r_L}{L} i_{hp,k+1}^* + \frac{2T_s}{L} [v_{hp,k+1} - s_{hp,k+1}^{(v)} V_{DCp,k+1}] \quad , \quad v = 1, 2 \quad (10)$$

$$G_{Ihp}^{(v)} = |i_{hp,k+2}^{(v)} - i_{hp,k+2}^*| \quad , \quad v = 1, 2 \quad (11)$$

The two-step ahead prediction has to be considered instead of the classical one-step ahead prediction in order to take into account the one sample step delay introduced by the digital implementation. It is important to highlight that this assumption does not represent an extension in the prediction horizon, but only one sampling interval delay compensation, always presents in practical systems.

## C. DC-Link voltage control

From (2) is possible to decouple the effects of the two AC sides of the converter on the DC model, as described in [27]. Integrating equation (2) between  $t_k$  and  $t_k + T_s$  the relations (9) and (10) are obtained.

$$C \int_{V_{DCp,k}}^{V_{DCp,k+1}} dV_{DCp} = \int_{t_k}^{t_k+T_s} s_{hp} [i_{hp} - i_{hp}^*] dt \quad (12)$$

$$V_{DCp,k+1} - V_{DCp,k} = \frac{1}{C} \int_{t_k}^{t_k+T_s} s_{hp} [i_{hp} - i_{hp}^*] dt \quad (13)$$

In order to solve the integral in (10), the average values of the time domain quantities during one sampling interval are considered instead of the instantaneous values resulting in the following approximation.

$$\begin{aligned} \int_{t_k}^{t_k+T_s} s_{hp} [i_{hp} - i_{hp}^*] dt &\cong \\ &\cong T_s s_{hp,k}^{avg} [i_{hp,k}^{avg} - i_{hp,k}^{*avg}] \end{aligned} \quad (14)$$

Assuming low DC-Link voltage variations during one sampling interval, its average value is considered equal to its instantaneous value at the instant  $t_k$ . For the same reason the average current produced in one sampling interval is considered equal to the current sampled at the end of the sampling interval. The average converter state,  $s_{hp}^{avg}$ , during a sampling interval is calculated, for M<sup>2</sup>PC, considering that two voltage vectors are applied during a sampling interval. Therefore, the converter voltage average value is equal to the expression in (13) at time  $t_k$ .

$$s_{hp,k}^{avg} = d_{hp,k}^{(1)} s_{hp,k}^{(1)} + d_{hp,k}^{(2)} s_{hp,k}^{(2)} \quad (15)$$

Under these approximations, the one-step ahead DC-Link voltage prediction is obtained in (14).

$$V_{DCp,k+1} = V_{DCp,k} + \frac{T_s}{C} s_{hp,k}^{avg} i_{hp,k+n}^{DC*} \quad (16)$$

By iterating (14), the two step ahead DC-Link voltage prediction is calculated, at the time instant  $t_k + 2T_s$ , for the two voltage vectors that must be generated during the next sampling interval.

$$\begin{aligned} V_{DCp,k+2}^{(v)} &= V_{DCp,k+1} + \\ &+ \frac{T_s}{C} s_{hp,k+1}^{(v)} [i_{hp,k+2}^{(v)} - i_{hp,k+2}^{AC*}] \quad , \quad v = 1, 2 \end{aligned} \quad (17)$$

The cost functions associated with  $v_{cIA}^{(1)}$  and  $v_{cIA}^{(2)}$  are then calculated also for the DC-Link voltage as follows.

$$G_{Vp}^{(v)} = |V_{DCp,k+2}^{(v)} - V_{DCp,k}^*| \quad , \quad v = 1, 2 \quad (18)$$

As already mentioned and discussed in subsection III.B for the current control, a two-step ahead prediction has to be here considered.

#### D. Total cost function

The total cost functions for each of the two selected output voltage vector,  $v_{Chp,k+1}^{(2)}$  and  $v_{Chp,k+1}^{(1)}$ , is chosen to be a weighted combination of the current and DC-Link voltage cost functions.

$$G_{hp}^{(v)} = w_I G_{Ihp}^{(v)} + w_V G_{Vp}^{(v)}, \quad v = 1, 2 \quad (19)$$

The two weighting factors,  $w_I$  and  $w_V$ , can be adjusted to achieve the desired the control performance [27]. Since the current cost function  $G_{Ihp}$  already includes the amount of current necessary to charge at the desired voltage the DC-Link capacitor, the importance of  $G_{Vp}$  lies in its ability to reduce the DC-Link voltage steady state error, related with the converter losses, which are not considered in  $G_{Ihp}$ . Therefore, the ratio  $w_V/w_I$  is typically set to the minimum value that ensure zero steady state error on the DC-Link voltage.

#### E. Duty cycles and overall cost function calculation

The switching times for the two selected vectors are calculated by solving the linear system of equations in (18). Once the value of  $K_{hp}$  is obtained from (18), the expressions for the switching times are obtained.

$$\begin{cases} d_{hp}^{(1)} = \frac{K_{hp}}{G_{hp}^{(1)}} \\ d_{hp}^{(2)} = \frac{K_{hp}}{G_{hp}^{(2)}} \\ d_{hp}^{(1)} + d_{hp}^{(2)} = 1 \end{cases} \rightarrow \begin{cases} d_{hp}^{(1)} = \frac{G_{hp}^{(2)}}{G_{hp}^{(1)} + G_{hp}^{(2)}} \\ d_{hp}^{(2)} = \frac{G_{hp}^{(1)}}{G_{hp}^{(1)} + G_{hp}^{(2)}} \end{cases} \quad (20)$$

Once the switching times are calculated the M<sup>2</sup>PC algorithm chooses the two converter states,  $s_{hp}^{(1)}$  and  $s_{hp}^{(2)}$ , applied respectively for a time  $d_{hp}^{(1)}$  and  $d_{hp}^{(2)}$ , if they minimize the following global cost function.

$$G_{hp} = d_{hp}^{(1)} G_{hp}^{(1)} + d_{hp}^{(2)} G_{hp}^{(2)} \quad (21)$$

This solution is proposed in alternative to an analytical duty cycle calculation. In fact the analytical determination of the duty cycles is highly dependent on the cost function chosen for the predictive control system while equation (18) represents a sub-optimal solution for the duty cycles calculations and it is only based on empirical considerations. In fact (18) is arbitrarily applicable to any combination of the most common cost functions, such as AC current, active and reactive power, DC-Link voltage for example, without requiring any analytical analysis. In fact, in this case it is not possible to calculate the optimal value of  $d_{hp}^{(1)}$  and  $d_{hp}^{(2)}$  that minimize the cost function as done in previous work. However, it is possible to demonstrate that the current error for FCS-MPC is higher compared to M<sup>2</sup>PC [9].

#### F. M<sup>2</sup>PC operative principle example

The operating principle of the M<sup>2</sup>PC is shown in Figure 2 for a generic sampling instant  $t_k$  where the current prediction process and the switching times calculation are highlighted. At the time  $t_k$  the cost function is calculated for both the selected vectors  $s_{hp}^{(1)}$  and  $s_{hp}^{(2)}$ . These vectors are applied at the time  $t_k + T_s$  for an interval that is inversely proportional to the value of the related cost functions. According to the example illustrated in Figure 3, at the time  $t_k$  the cost function associated with  $s_{hp}^{(2)}$  is lower than the one associated with  $s_{hp}^{(1)}$ ; therefore  $s_{hp}^{(2)}$  is applied for a longer time, with respect to  $s_{hp}^{(1)}$ , in the time interval  $t_k + T_s \dots t_k + 2T_s$ . Conversely, at the time  $t_k + T_s$ , the cost function associated with  $s_{hp}^{(1)}$  is lower than the one associated with  $s_{hp}^{(2)}$ ; therefore  $s_{hp}^{(1)}$  is applied for a longer time, with respect to  $s_{hp}^{(2)}$ , in the time interval  $t_k + 2T_s \dots t_k + 3T_s$ .

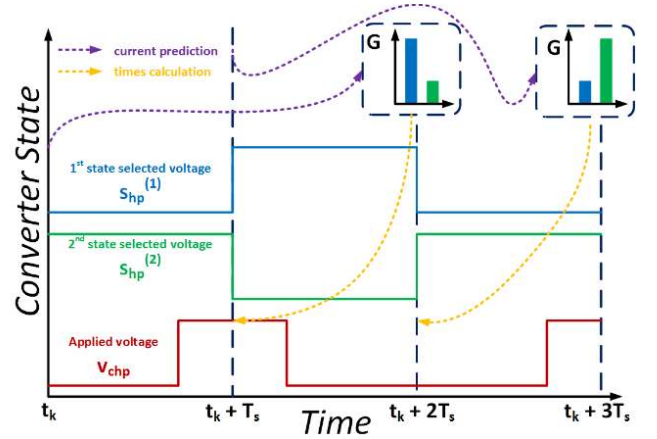


Figure 3. M<sup>2</sup>PC working principle example for port  $h$  phase  $p$ .

As a result, the applied voltage  $v_{chp}$  shows a pattern similar to the one obtained applying a modulation technique. Figure 2 also shows that the M<sup>2</sup>PC operation is equivalent to two predictive control systems operating in parallel, applying to the converter a combination of these two predictive current control outputs.

## IV. SIMULATION RESULTS

Simulation tests are carried out by means of Matlab/Simulink using the model of Figure 1 with parameters values reported in Table I.

TABLE I. SIMULATION AND EXPERIMENTAL PARAMETERS

Name	Description	Value	Unit
C	DC-Link capacitor	3100	[ $\mu$ F]
$r_L$	Inductor resistance	0.5	[ $\Omega$ ]
L	AC filter inductance	11	[mH]
$V_{peak}$	AC supply peak value	212	[V]
$V_{DC}$	Capacitor voltage	92	[V]
$f_{sw,DC/DC}$	DAB switching frequency	2500	[Hz]
$T_s$	Sample time	0.2	[ms]
N	DC-Link voltage reference horizon	100	/
$w_I$	Current control weighting factor	1	/
$w_V$	DC voltage control weighting factor	5 (FCS-MPC) 0.1 (M <sup>2</sup> PC)	/

Figure 4 shows the simulation tests results in several operational cases. Figure 4a shows a comparison of the AC current THD on port 1 obtained with M<sup>2</sup>PC at a sampling frequency of 5kHz and FCS-MPC at several values of sampling frequency. In the simulation two values of  $P_i^*$  are considered while  $Q_i^*$  is kept constant at 0VAR. Results show that the FCS-MPC switching frequency matches the M<sup>2</sup>PC one when a sampling frequency of 10kHz or 15kHz,

depending on the active power reference value, is used. However, in both cases the AC current THD produced using FCS-MPC exceeds the one obtained with M<sup>2</sup>PC. The converter voltages and AC currents on port 1 for the two selected values of active power reference are shown, respectively, in Figure 4c and Figure 4d for M<sup>2</sup>PC and Figure 4e and Figure 4f for FCS-MPC.

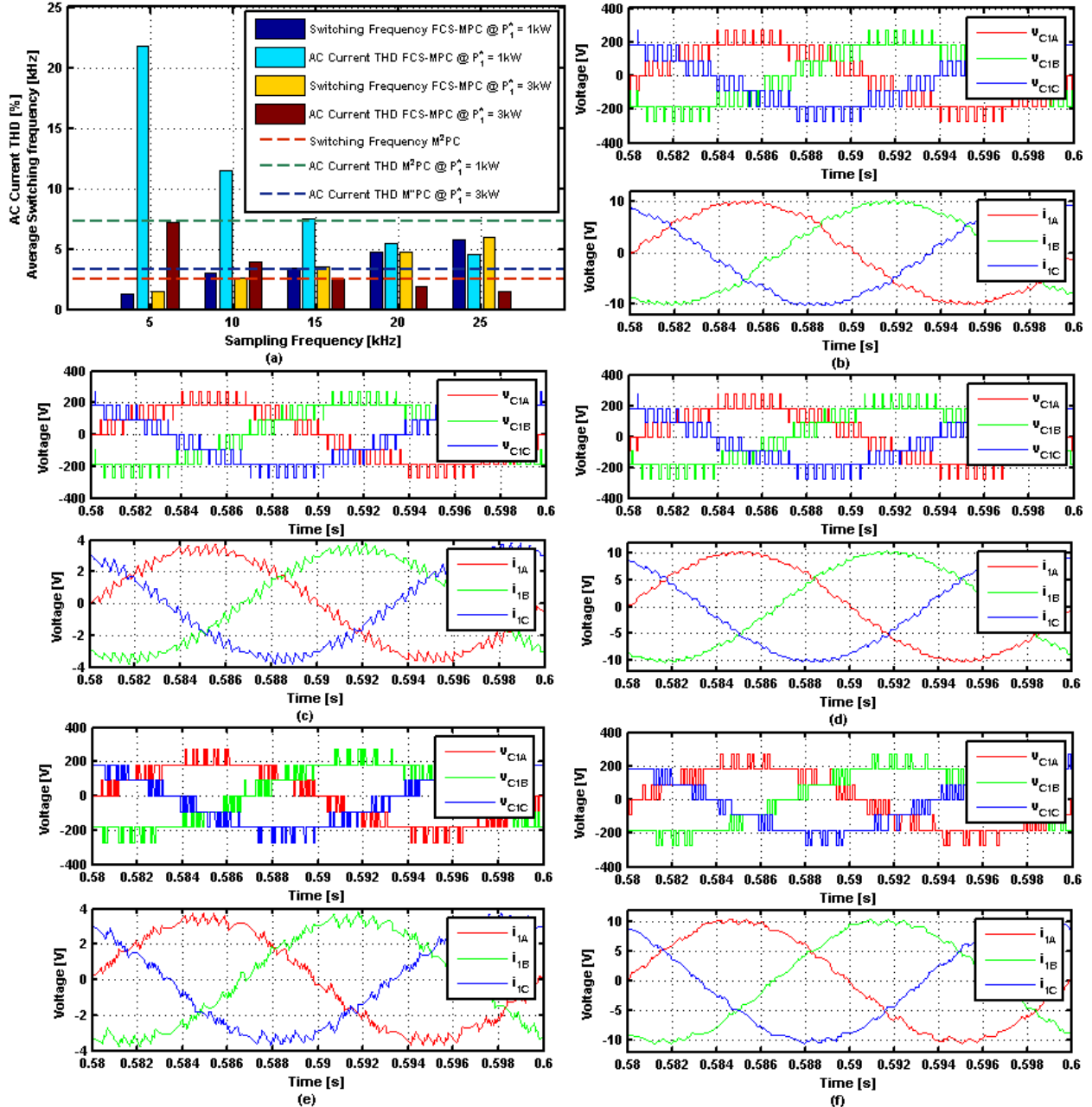


Figure 4. Simulation results: (a) Comparison of AC current THD and switching frequency at different power rating for MPC at different sampling frequencies and M<sup>2</sup>PC at a sampling frequency of 5kHz; (b) Converter voltage and AC currents for M<sup>2</sup>PC with a parameter variations of -30% ( $r_L=0.35\Omega$ ,  $L=0.77mH$ ,  $C=2300\mu F$ ) when an active power of 3kW flows through the converter; (c) Converter voltage and AC currents for M<sup>2</sup>PC for a sampling frequency of 5kHz when an active power of 1kW flows through the converter; (d) Converter voltage and AC currents for M<sup>2</sup>PC for a sampling frequency of 5kHz when an active power of 3kW flows through the converter; (e) Converter voltage and AC currents for MPC for a sampling frequency of 15kHz when an active power of 1kW flows through the converter; (f) Converter voltage and AC currents for M<sup>2</sup>PC for a sampling frequency of 10kHz when an active power of 3kW flows through the converter.

In figure 4b the robustness of M<sup>2</sup>PC to parameter mismatches is analyzed by showing the converter voltage and AC currents for an  $r_L$ ,  $L$  and  $C$  mismatch of -30% compared to the nominal values, when  $P_i^*$  is equal to 3kW and  $Q_i^*$  is equal to 0VAR. The results show that M<sup>2</sup>PC is able to operate under these extreme conditions, but increased AC current distortion are present, with respect to Figure 4d.

## V. EXPERIMENTAL RESULTS

Experimental testing has been carried out for the proposed M<sup>2</sup>PC on a 300kVA 3-Phase, 7-Level CHB Back-To-Back converter [28] shown in Figure 5, with the experimental parameters of Table II. This converter is able to operate at input AC voltage of 3.3kV controlling an AC current of approximately 65A at full power [28]. However, in order to test the control scheme, only low voltage tests are presented in this work, even if the converter device switching frequency is maintained at the nominal value (800Hz) when a sampling frequency of 5kHz is considered, to emulate high power switching conditions. This test condition represents a challenging scenario for the control system considering that when the proposed converter works at low power the device parasitic components and noise levels, typical of a high power converter, are still present. The control scheme for the converter is implemented on a Texas Instruments 6713 DSP interfaced to four custom FPGA boards. Experimental results are shown only for port 1 since the control on port 2 is identical with the only exception that the DC-Link voltage control is not required on port 2. In Figure 6 the steady state performances of M<sup>2</sup>PC are analyzed for phase A, port1 and compared the classic Model Predictive Control implementation proposed in [27] with the same cost function parameters. The converter voltage shows a fixed switching frequency waveform with a THD of approximately 24.5% while the current has a THD of approximately 4.5%, lower

than the AC current THD value produced with the standard control approach by FCS-MPC (6.3%). In fact, since an intrinsic modulation technique is implemented directly in the cost function minimization algorithm, the switching frequency is maintained constant and the harmonics are concentrated around multiples of the switching frequency.



Figure 5. 3-Phase, 7-Level CHB Back-To-Back converter.

However, the switching instants are calculated using an empirical method and some calculation errors, especially in practical systems, can occur. In Figure 7 an active power reference step from 0W to 3kW is considered. The finite delay introduced by the DC/DC converter has to be considered and, in order not to affect the DC-Link voltage control response, the active power reference variation has to be limited by using a ramp generator. The measured active power is around 3.8 kW with the additional 800W requested by the DC-Link voltage control in order to regulate the DC-Link voltages at the desired value and compensate the DC/DC converter losses. Looking at the DC-Link voltages, the converter takes around 0.7s to recover the DC-Link voltage tracking with a maximum error of about 10% of the nominal value.

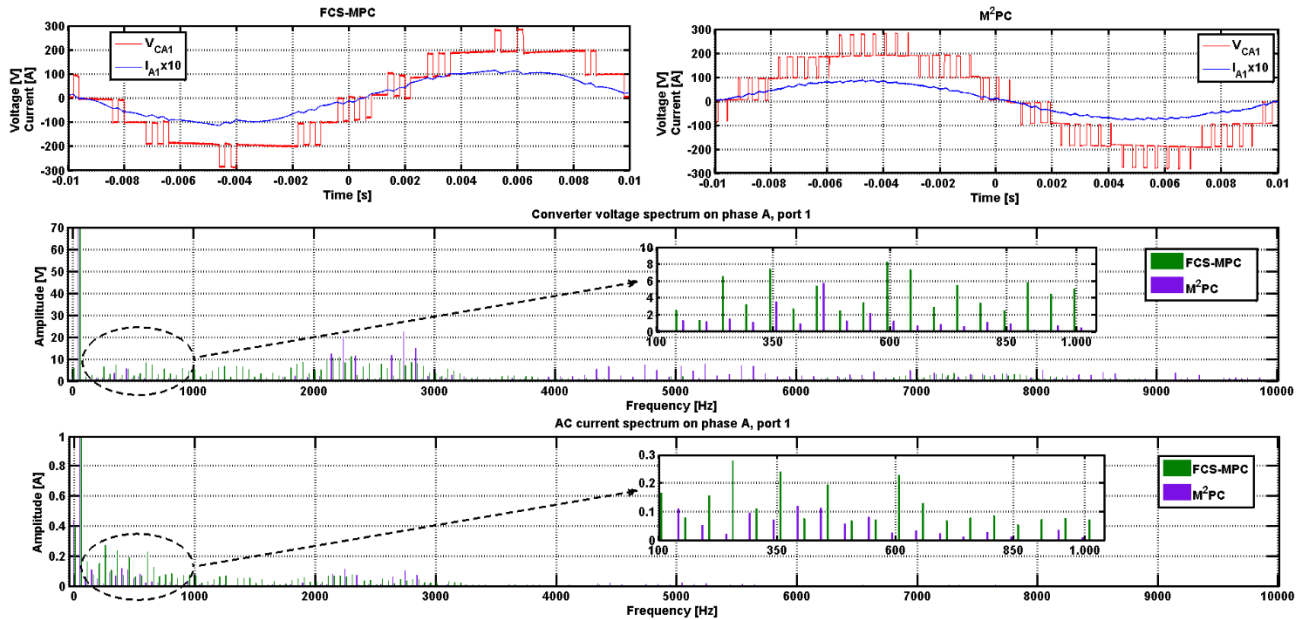


Figure 6. Experimental results for M<sup>2</sup>PC on the 3-Phase, 7-Level CHB Back-To-Back converter: steady state converter voltage and AC current on phase A, port 1.

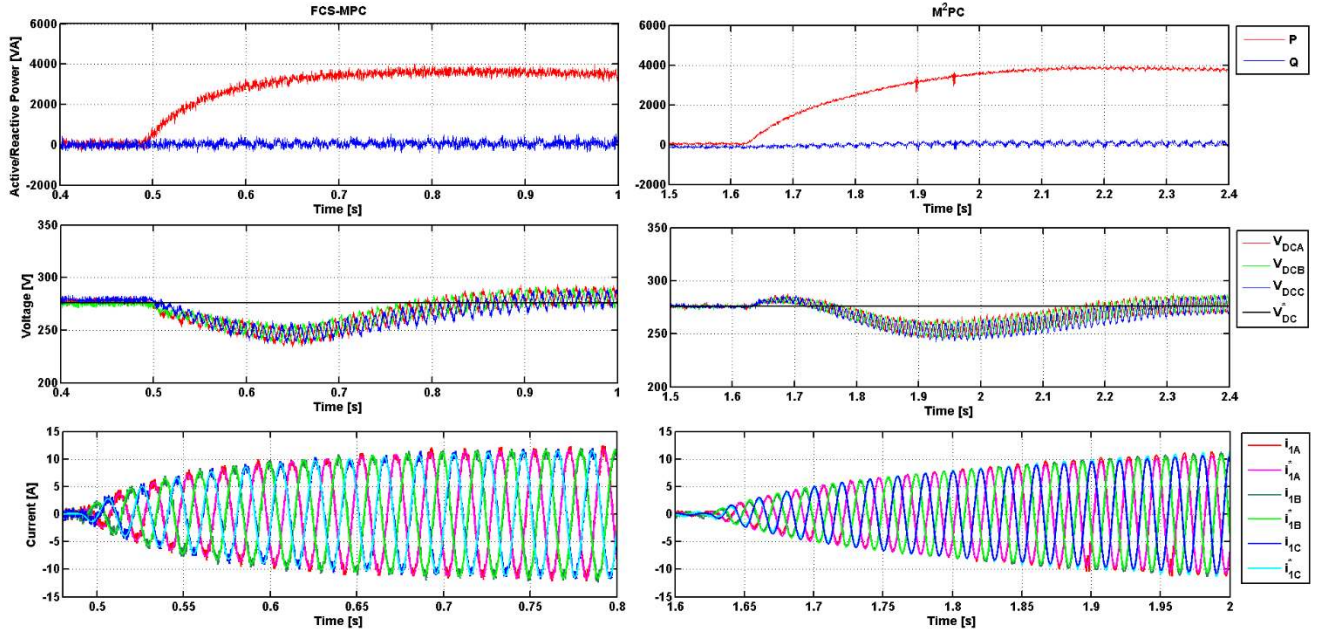


Figure 7. Experimental results for M<sup>2</sup>PC on the the 3-Phase, 7-Level CHB Back-To-Back converter: Active and Reactive power and DC-Link voltages on port 1 when an active power step from 0kW to 3kW is demanded to the SST converter at time 1.65s.

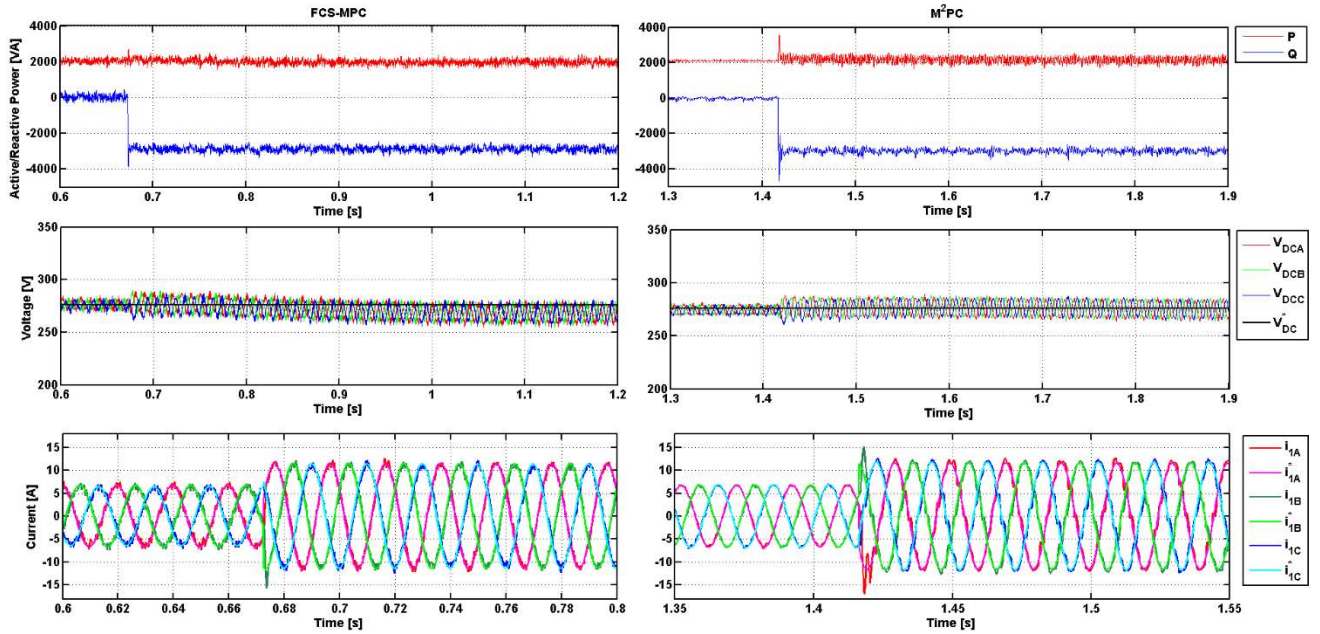


Figure 8. Experimental results for M<sup>2</sup>PC on the the 3-Phase, 7-Level CHB Back-To-Back converter: Active and Reactive power and DC-Link voltages on port 1 when an active power step from 0kW to 3kW is demanded to the SST converter at time 1.65s.

Compared with FCS-MPC, the M<sup>2</sup>PC DC-Link voltage controller manages to achieve similar dynamic performances. The only small difference in the two DC-Link voltage transient responses it is related with the different tuning of the controllers. Figure 8 considers a reactive power reference step from 0VAR to -3000VAR, while an active power of 2 kW is delivered to port 2. In this case, since the reactive power is not shared between the two sides of the converter, the dynamics of the DC-Link voltage control is not affected by the reactive power variation and there is no need to limit the reactive power reference variation. An oscillatory transient in the AC

current response is present using M<sup>2</sup>PC, which cannot be noticed using the classic MPC. This is related with the different operative point. In fact, the empirical switching time calculation generates more distortion when the generated converter voltage gets further from the ideal modulation index value of 0.8 times the DC-link voltage on each phase.

## VI. CONCLUSIONS

M<sup>2</sup>PC combines the main good features of MPC control, i.e. fast transient response, multi-objective control, include constraint and additional control target directly in the cost



function minimization algorithm. At the same time it has the further advantage of including a suitable modulation scheme inside the cost function minimization algorithm, in order to maintain a constant switching frequency equal to half of the sampling frequency. The switching times are calculated using an empirical solution based on the value of the cost functions for two adjacent states providing a sub-optimal approach to the minimization problem. This technique has already been introduced in previous works for a 7-Level CHB current control [9], [20], showing that M<sup>2</sup>PC performs similarly to a Dead-Beat current control with Space Vector Modulation operating at the same sampling frequency. The proposed technique is validated through experimental testing, showing a fast dynamic and a low current THD for a 2.5 kHz total converter switching frequency. Compared with previously published results, M<sup>2</sup>PC produces similar performances, in terms of current THD, to the Dead-Beat control proposed in [9], [27] whilst maintaining the fast DC-Link control response presented for MPC in [27]. M<sup>2</sup>PC introduces the ability to perform a multi-objective control; for example, by including the DC-Link voltage control in the cost function, it is possible to obtain a current and DC-Link voltage control without compromising the overall performance of the system.

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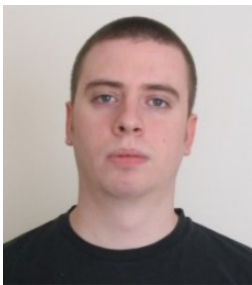


Luca Tarisciotti received the Master's degree in electronic engineering from The University of Rome "Tor Vergata" in 2009 and his Ph.D. degree in electrical and electronic engineering in the PEMC group, University of Nottingham in 2015. He is currently working as Research Fellow at the University of Nottingham, UK. His research interests include multilevel converters, advanced modulation schemes, and advanced power converter control.



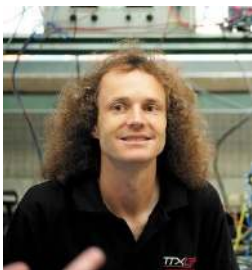
Professor Pericle Zanchetta received his degree in Electronic Engineering and his Ph.D. in Electrical Engineering from the Technical University of Bari (Italy) in 1993 and 1997 respectively. In 1998 he became Assistant Professor of Power Electronics at the same University and in 2001 he joined the PEMC research group at the University of Nottingham – UK, where he is now Professor in Control of Power Electronics systems. He is Vice-chair of the IAS Industrial Power Converters Committee (IPCC) and Associate

Editor of the IEEE Transactions on Industry Applications and IEEE Transactions on Industrial Informatics.



Alan Watson received his MEng (Hons) degree in Electronic Engineering from the University of Nottingham in 2004, before pursuing a PhD in Power Electronics, also at Nottingham. In 2008, he became a Research Fellow in the Power Electronics Machines and Control Group, working on the UNIFLEX project. Since 2008, he has worked on several projects in the area of high power electronics including high power resonant converters, high

voltage power supplies, and multilevel converters for grid connected applications such as HVDC and FACTS. In 2012 he was promoted to Senior Research Fellow before becoming a Lecturer in High Power Electronics in 2013. His research interests include the development and control of advanced high power conversion topologies for industrial applications, future energy networks, and VSC-HVDC.



Prof Pat Wheeler received his BEng [Hons] degree in 1990 from the University of Bristol, UK. He received his PhD degree in Electrical Engineering for his work on Matrix Converters from the University of Bristol, UK in 1994. In 1993 he moved to the University of Nottingham and worked as a research assistant in the Department of Electrical and Electronic Engineering. In 1996 he became a

Lecturer in the Power Electronics, Machines and Control Group at the University of Nottingham, UK. Since January 2008 he has been a Full Professor in the same research group. He has published over 250 academic publications in leading international conferences and journals.



Jon C. Clare (M'90–SM'04) was born in Bristol, U.K. He received the B.Sc. and Ph.D. degrees in electrical engineering from the University of Bristol, U.K. From 1984 to 1990, he was a Research Assistant and Lecturer at the University of Bristol involved in teaching and research in power electronic systems. Since 1990 he has been with the Power Electronics, Machines and Control Group at the University of Nottingham, U.K., and is currently Professor in Power

Electronics and Head of Research Group. His research interests are power electronic converters and modulation strategies, variable speed drive systems, and electromagnetic compatibility.



Stefano Bifaretti (M'07) received the Laurea degree and the PhD degree in Electronic Engineering from University of Rome "Tor Vergata", Italy, in 1999 and 2003. In 2004 he became Assistant Professor at Department of Electronic Engineering of the University of Rome "Tor Vergata" where he is currently a lecturer in Power Electronics. In 2007 he was with the PEMC research group at the University of Nottingham (UK),

collaborating on the UNIFLEX-PM European project. He has published over 70 papers in international journals and conferences. His research interests include power electronics converters, industrial drives and future electricity networks.