Multi-Phase Buck Converters with Extended Duty Cycle

Yungtaek Jang, Milan M. Jovanović, and Yuri Panov

Power Electronics Laboratory
Delta Products Corporation
P.O. Box 12173, 5101 Davis Drive
Research Triangle Park, NC 27709

***Abstract* — A family of multi-phase, pulse-width-modulated (PWM) step-down converters that exhibit high input-to-output voltage conversion ratios is introduced. The proposed converters operate with larger duty cycles and lower voltage stresses on the switches than their conventional converter counterparts making them suitable for applications in high-frequency, non-isolated point-of-load converters employed in powering today's microprocessors.**

I. INTRODUCTION

Today, multi-phase, interleaved, synchronous-rectifier buck converters are extensively used as point-of-load regulators for modern high-performance microprocessors that require very low output voltages and fast dynamic responses [1], [2]. These modular or embedded point-of-load converters, which are known as voltage regulators (VRs), have the output voltage in the 0.8 – 1.3-V range and need to provide very high currents, very often in excess of 100 A, to highly dynamic microprocessor loads that exhibit current slew rates as high as 400-500 A/μs. In the majority of applications VRs are powered from the 12-V output of an ac-dc power supply (*i.e.*, silver box).

Due to a very low output voltage, the duty cycle of the 12-V input VRs is very narrow, *i.e.*, it is only around 10 %. Moreover, with anticipated future reductions of the microprocessor supply voltage, the duty cycle will be reduced even further. Generally, a small duty cycle has a detrimental effect on the VR efficiency and load transient response [2], [3]. In addition, a very small duty cycle limits the maximum attainable switching frequency because the conduction time of the high-side switch cannot be controlled when it becomes shorter than the driver rise/fall time.

One method to overcome the performance limitations of a short duty cycle is to employ a two-stage approach [4]. In this approach, the 12-V input voltage is stepped down to an optimal level by a pre-regulator stage before it is applied to a multi-phase interleaved buck converter output stage. While it has been demonstrated that this approach can improve the overall performance of the 12-V VR, it has not gained acceptance in industry due to an increased number of components and, more importantly, an increased cost.

Another approach to deal with a small duty cycle of the 12-V VRs is to develop single-stage multi-phase buck-derived topologies with extended duty cycles. So far, a number of these topologies have been discussed in the literature. The proposed topologies employ either transformers or coupled inductors to achieve a duty-cycle extension, *i.e.*, to increase the step-down voltage conversion ratio of the buck converter. The transformer-based topologies, for example, include the phase-shifted full-bridge converter [3], the push-pull forward converter [5], the push-pull converter [6], and the half-bridge converter [7]. The coupled-inductor implementations reported in [8]-[10] are based on the tapped-inductor buck converter. Generally, the performance of all these implementations is adversely affected by leakage inductances of their magnetic components, limiting their switching-frequency range and performance.

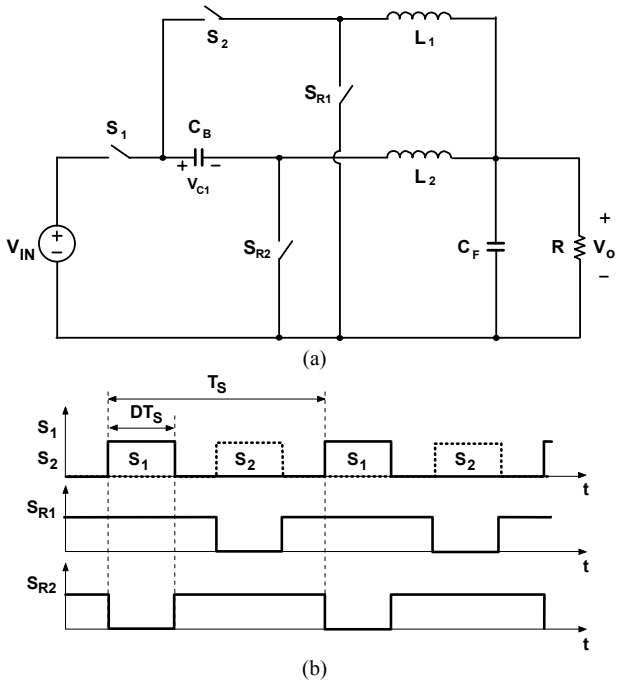

Fig. 1. Two-inductor, two-switch PWM buck converter: (a) circuit diagram; (b) switch timing diagrams.

0-7803-9547-6/06/$20.00 ©2006 IEEE.

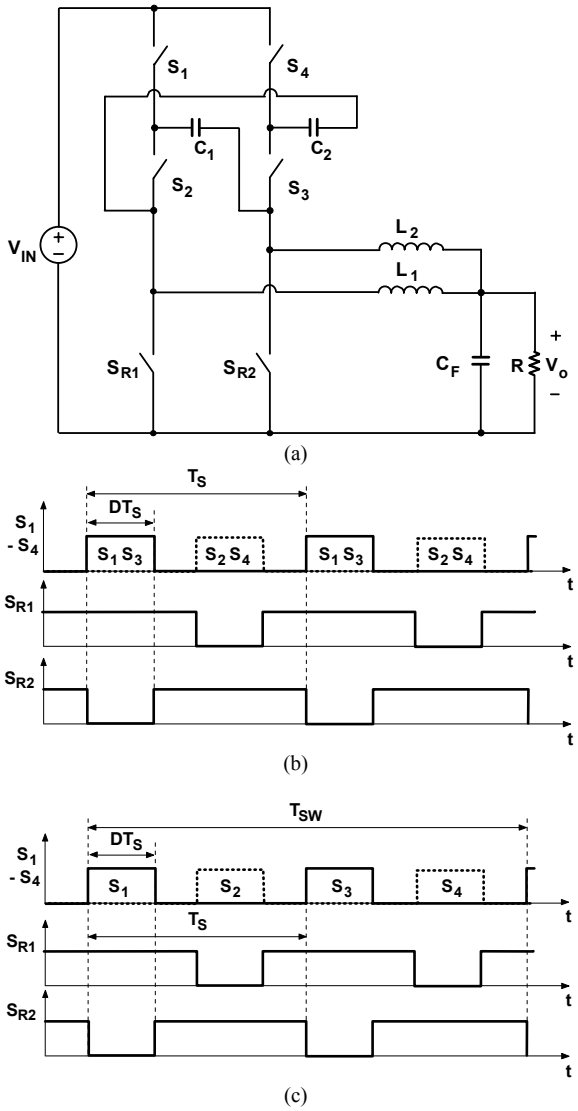

Fig. 2. Two-inductor, four-switch PWM buck converter: (a) circuit diagram; (b) switch timing diagrams for two-phase interleaved control; (c) switch timing diagrams for four-phase interleaved control.

In this paper, a family of multi-phase PWM converters that provide extended duty cycle without the use of magnetic components is introduced. The proposed multi-phase step-down converters operate with larger duty cycles and lower voltage stresses on the switches than their conventional buck converter counterparts. Since these converters do not use magnetic components to extend the duty cycle, they have the potential of operating at a high switching frequency without a degradation of performance.

II. Multi-Phase PWM Buck Converters with Extended Duty Cycle

Figures 1(a) and 1(b) show the circuit diagram and switch timing waveforms, respectively, of the two-inductor, two-switch buck converter with extended duty cycle. The circuit in Fig. 1(a) exhibits the same voltage-conversion ratio (voltage gain) as the conventional single, or multi-phase buck converter, but with a duty cycle that is twice as large as that of the conventional buck converter.

The implementation of the two-inductor, four-switch PWM buck converter is shown in Fig. 2(a). Generally, this converter can be controlled either by two-phase or four-phase interleaved control. The timing diagrams of the switches for the two-phase interleaved control are shown in Fig. 2(b), whereas the timing diagrams for the four-phase interleaved control with counter clockwise sequence S_1-S_2-S_3-S_4 are shown in Fig. 2(c).

Since the operation and detailed analysis of the two-inductor, two-switch buck converter in Fig. 1(a) was presented in [11] and [12], in this paper the analysis and operation of the two-inductor, four-switch buck converter in Fig. 2(a) is given.

A. Principle of Operation

To facilitate the explanation of the circuit operation, Fig. 3 shows a simplified circuit diagram of the circuit in Fig. 2(a). In the simplified circuit, it is assumed that filter capacitor C_F and capacitors C_1 and C_2 are large enough so that the voltage ripple across them are small compared to their dc voltages. Synchronous rectifiers S_{R1} and S_{R2} are modeled as diode rectifiers D_1 and D_2, respectively. In this analysis it is also assumed that all semiconductor components are ideal, *i.e.*, they represent zero impedances in the on state and infinite impedances in the off state. Finally, it is assumed that the conducting periods (*i.e.*, DT_S) of switches S_1, S_2, S_3, and S_4 are equal.

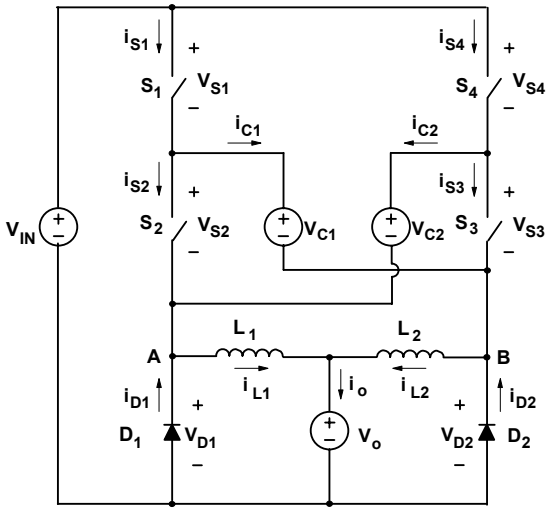

Fig. 3. Simplified circuit diagram of two-inductor, four-switch buck converter in Fig. 2 showing reference directions of currents and voltages.

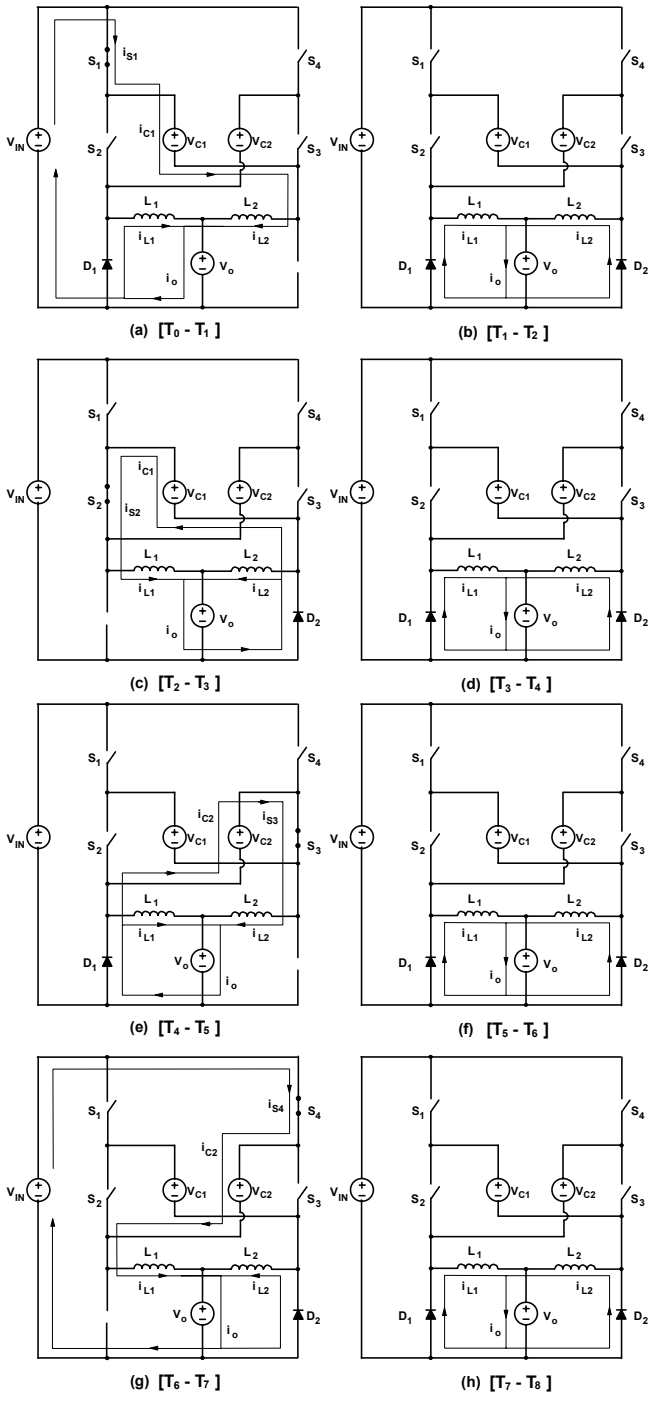

Fig. 4. Topological stages of two-inductor, four-switch buck converter with four-phase interleaving control.

To further facilitate the analysis of operation, Fig. 4 shows the topological stages of the circuit in Fig. 3 during a switching cycle, whereas Fig. 5 shows its key waveforms for four-phase interleaved operation. The reference directions of currents and voltages plotted in Fig. 5 are shown in Fig. 3.

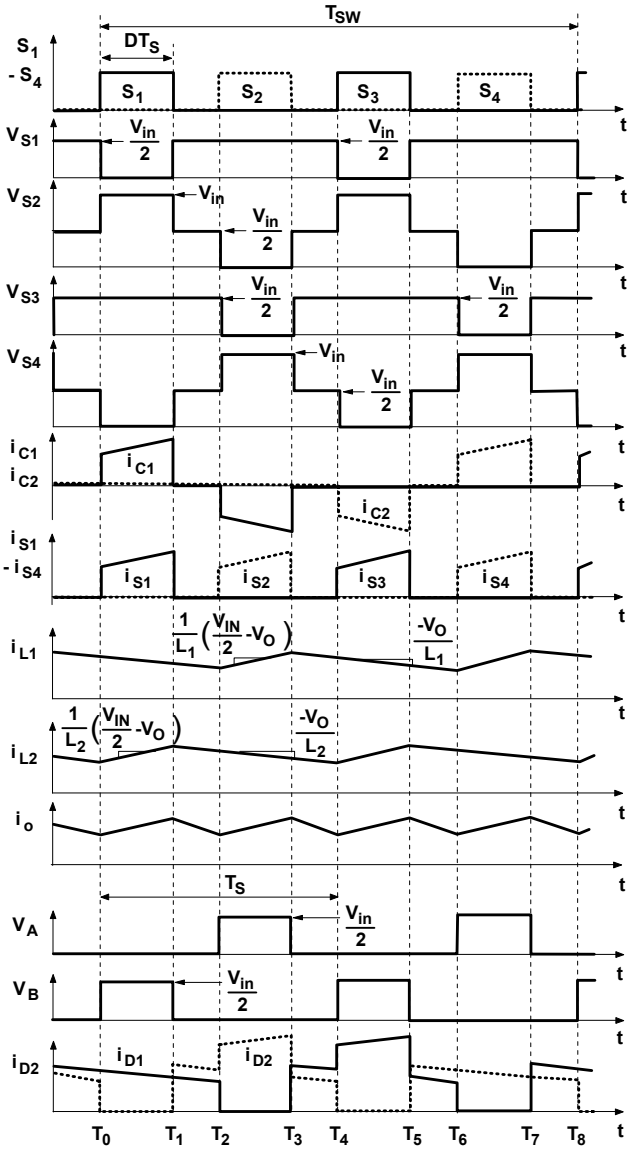

Fig. 5. Key waveforms of two-inductor, four-switch buck converter with four-phase interleaving control.

It should be noted that in steady state, the voltage across capacitor C_1 is equal to the average voltage across switch S_2 because the average voltages across inductors L_1 and L_2 are zero. From the waveform of voltage V_{S2} shown in Fig. 5, the average voltage across switch S_2 can be easily derived as

$$< V_{S2} >= V_{C1} = DV_{IN} + (1-2D)V_{C1} . \quad (1)$$

Solving Eq. (1) for V_{C1}, it follows that

$$V_{C1} = V_{IN}/2 . \quad (2)$$

Similarly, it can be derived that voltage V_{C2} across capacitor C_2, which is equal to the average voltage across switch S_3, is

$$V_{C2} = V_{IN}/2 . \quad (3)$$

As shown in Fig. 4(a), during time interval $[T_0 - T_1]$ when switch S_1 is on, capacitor C_1 is being charged by the input current flowing through switch S_1, capacitor C_1, and inductor L_2 into output V_O. At the same time, the energy stored in inductor L_2 is being increased because current i_{L2} increases at the rate

$$\frac{di_{L2}}{dt} = \frac{V_{IN} - V_{C1} - V_O}{L_2} = \frac{\frac{V_{IN}}{2} - V_O}{L_2}. \quad (4)$$

During time interval $[T_0 - T_1]$, the energy stored in inductor L_1 is being discharged into the output by current i_{L1} flowing through diode D_1 into output V_O. During this time interval inductor current i_{L1} decreases at the rate

$$\frac{di_{L1}}{dt} = \frac{-V_O}{L_1}. \quad (5)$$

When at $t=T_1$, switch S_1 is turned off, inductor current i_{L2} is diverted from switch S_1 to rectifier D_2, as shown in Fig. 4(b), and the energy stored in inductor L_2 starts to discharge into output V_O. During time interval $[T_1 - T_2]$, current i_{L2} decreases at the rate

$$\frac{di_{L2}}{dt} = \frac{-V_O}{L_2}, \quad (6)$$

while inductor current i_{L1} continues to decrease at the rate given in Eq. (5).

When at $t=T_2$, switch S_2 is turned on, the circuit enters the topological stage shown in Fig. 4(c). During this topological stage, *i.e.*, during time interval $[T_2 - T_3]$, capacitor C_1 is being discharged by inductor current i_{L1} flowing in the loop consisting of switch S_2, inductor L_1, output V_O, diode D_2, and capacitor C_1. In fact, during this topological stage, capacitor C_1 serves as the input energy source to the buck converter with inductor L_1. As the result of a positive voltage across inductor L_1, inductor current i_{L1} during time interval $[T_2 - T_3]$ increases as

$$\frac{di_{L1}}{dt} = \frac{V_{C1} - V_O}{L_1} = \frac{\frac{V_{IN}}{2} - V_O}{L_1}. \quad (7)$$

In the same time interval, current i_{L2} in inductor L_2 continues to flow through diode D_2 into the output, as shown in Fig. 4(c), and is decreasing at the rate given in Eq. (6).

When at $t=T_3$, switch S_2 is turned off, the circuit enters the topological stage shown in Fig. 4(d), which is identical to the topological stage in Fig. 4(b). During this stage both switches are off and both inductors discharge their energy into the load. For equal values of inductances of inductors L_1 and L_2, currents i_{L1} and i_{L2} decrease at the same rates that are given by Eqs. (5) and (6).

After switch S_3 is turned on at $t=T_4$, the circuit enters the topological stage shown in Fig. 4(e) that lasts until switch S_3 is turned off at $t=T_5$. During this topological stage, capacitor C_2 is being discharged by inductor current i_{L2} flowing in the loop consisting of switch S_3, inductor L_2, output V_O, diode D_1, and capacitor C_2, *i.e.*, during this topological stage, capacitor C_2 serves as the input energy source to the buck converter with inductor L_2. Because of a positive voltage across inductor L_2, inductor current i_{L2} during time interval $[T_4 - T_5]$ increases at the rate

$$\frac{di_{L2}}{dt} = \frac{V_{C2} - V_O}{L_2} = \frac{\frac{V_{IN}}{2} - V_O}{L_2}, \quad (8)$$

During the same time interval, current i_{L1} in inductor L_1 continues to flow through diode D_1 into the output, as shown in Fig. 4(e), and decreases at the rate given in Eq. (6).

When at $t=T_5$, switch S_3 is turned off, inductor current i_{L2} is diverted from switch S_3 to rectifier D_2, as shown in Fig. 4(f), and the energy stored in inductor L_2 starts to discharge into voltage source V_O at the rate given in Eq. (6) while inductor current i_{L1} continues to decrease at the rate given in Eq. (5).

When at $t=T_6$, switch S_4 is turned on, the input current starts flowing through switch S_4, capacitor C_2, and inductor L_1 into output voltage source V_O, while the current in inductor L_2 continues to flow through diode D_2 into output V_O, as shown in Fig. 4(g). Namely, during the duration of this topological stage, capacitor C_2 is being charged and at the same time the energy stored in inductor L_1 is being increased because current i_{L1} increases at the rate

$$\frac{di_{L1}}{dt} = \frac{V_{IN} - V_{C2} - V_O}{L_1} = \frac{\frac{V_{IN}}{2} - V_O}{L_1}. \quad (9)$$

When at $t=T_7$, switch S_4 is turned off, the circuit enters the topological stage shown in Fig. 4(h). During this stage both switches are off and both inductor currents i_{L1} and i_{L2} decrease with rates given by Eqs. (5) and (6), respectively.

The circuit enters a new switching cycle at $t=T_8$, when switch S_1 is turned on again.

Voltage conversion ratio $M=V_O/V_{IN}$ of the analyzed converter can be calculated from the volt-second balance of the output inductors. However, it should be noticed that in the converter in Fig. 2(a), the ripple frequency of output filter inductors L_1 and L_2 is twice the switching frequency of the individual switches S_1-S_4. With the notation used in Fig. 5, the volt-second balance equation for inductor L_2 is

$$\left(\frac{V_{IN}}{2} - V_O\right) DT_S = V_O(T_S - DT_S) \quad (10)$$

so that

$$M = \frac{V_O}{V_{IN}} = \frac{D}{2}. \quad (11)$$

As can be seen from Eq. (11), for the same duty cycle, the output voltage of the converter in Fig. 2(a) is one half of the output voltage of the conventional buck converter. This high step-down conversion ratio makes the converter suitable for applications with a high difference between the input and output voltage.

It should be noted that Eq. (11), which defines the voltage-gain dependence on duty cycle of the converter in Fig. 2(a) with four-phase interleaving control sequence S_1-S_2-S_3-S_4, is only valid for duty cycles equal or less than 50%, *i.e.*, for $D \le 0.5$. Namely, if the duty cycle is greater than 0.5, the conduction periods of switches S_2 and S_3 overlap causing a short across capacitors C_1 and C_2.

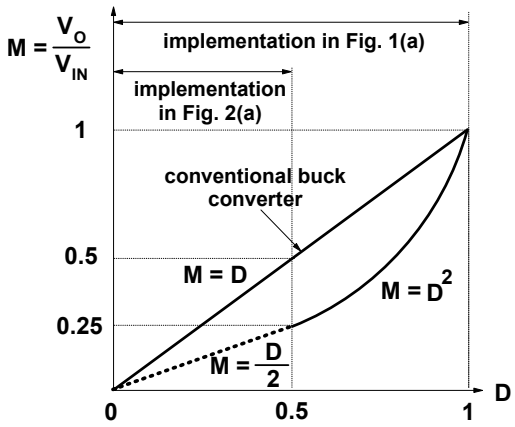

Fig. 6. Dependence of voltage-conversion ratio M on duty cycle of converters in Figs. 1(a) and 1(b) along with that of conventional buck converter.

Generally, the restricted duty-cycle range of the four-phase interleaved converter in Fig. 2(a) does not have any effect on the performance of the converter in VRM applications with a 12-V input where the duty cycle never exceeds 50% even during no-load-to-full-load transitions. Furthermore, in applications that require operation with a duty cycle larger than 50%, the implementation in Fig. 1(a) can be employed because this implementation offers a full-range duty cycle operation. For duty cycles $D \le 0.5$, voltage-conversion ratio M of the circuit in Fig. 1(a) is identical to that in Fig. 2(a), whereas for D>0.5, voltage conversion ratio M of the circuit in Fig. 1(a) is

$$M = \frac{V_O}{V_{IN}} = D^2, \qquad (10)$$

as shown in Fig. 6 along with the corresponding dependence of the conventional buck converter.

B. Design Considerations

As can be seen from the voltage waveforms of all switches in Fig. 5, the drain voltage variation of each switch is only one half of input voltage V_{IN} at the turn-on and turn-off instants, unlike the conventional buck converter, whose open switches block the full input voltage V_{IN}. Because the turn-on and turn-off switching losses due to the overlapping of the switch current and voltage waveforms are approximately proportional to the voltage across the switch and since the capacitive discharge turn-on loss is proportional to the square of the voltage across the switch prior to the turn-on, the switching losses of the proposed converter are very much reduced compared to those of the conventional buck converter. As a result, the proposed converter is expected to show better efficiency compared to its conventional multi-phase counterpart at high frequencies where the switching loss is dominant.

In addition, because the maximum voltage stress on switches S_1, S_3, S_{R1}, and S_{R2} is only $V_{IN}/2$, as shown in Fig. 5, the converter can employ semiconductor switches with a lower voltage rating, which usually have lower on-resistances with respect to their higher voltage rated counterparts, resulting in a reduction of conduction loss. However, it should be noted that in the converter in Fig. 2(a), each switch carries one half of the load current, *i.e.*, $I_O/2$ compared to $I_O/4$ that is carried by each switch in a four-phase conventional buck converter. Nevertheless, this difference in the switch currents does not significantly affect the performance of the converter. Namely, to have the same number of semiconductor switches as in the conventional four-phase buck converter, each synchronous rectifier S_{R1} and S_{R2} in the converter in Fig. 2(a) should be implemented with two switches in parallel so that each synchronous rectifier switch carries current $I_O/4$. In addition, for high step-down ratios, *e.g.*, M<0.2, the conduction time of high-side switches S_1-S_4 is much shorter than that of synchronous rectifiers S_{R1} and S_{R2} so that the increase of conduction loss of switches S_1-S_4 due to their increased current is not very significant. To further minimize conduction losses, the capacitors C_1 and C_2 should be implemented by using low-ESR ceramic capacitors.

One very desirable feature of the proposed converter is the inherent and accurate current sharing between inductor currents i_{L1} and i_{L2} due to the fact that charging portions of the inductor currents flow through capacitors C_1 and C_2. Namely, if the charging portions of the currents become unbalanced, the voltage across capacitors C_1 and C_2 starts to deviate from the $V_{IN}/2$ value in the direction that balances the inductor currents. Because of this inherent current sharing, the interleaved controller for the converter in Fig. 2(a) does not need a current sharing loop, which makes the controller simpler compared to that of the conventional multi-phase buck converter.

C. Concept Generalization

The concept in Figs. 1(a) and 2(a) can be extended to any number of inductors and phases. In fact, the extension of the converter in Fig. 1(a) to the three-inductor, three-switch topology is given in [11] and [12]. The approach can be extended to n-inductor implementation as shown in Fig. 7.

Similarly, Fig. 8 shows the extension of the circuit in Fig. 2(a) to the three-inductor, six-switch step-down topology. This circuit can be operated either by three-phase or six-phase interleaved control. For a three-phase interleaved operation, the switching instances of pairs of switches that are switched simultaneously S_1-S_5, S_2-S_6, and S_3-S_4 are interleaved, *i.e.*, phase shifted by 120 degrees. For a six-phase operation, the switching instances of individual switches S_1, S_4, S_2 S_5, S_3, and S_6 of the proposed converter are interleaved, *i.e.*, phase shifted by 60 degrees.

The extension of the converter in Fig. 2(a) to the 2n-switch, n-inductor, step-down PWM converter is shown in Fig. 9. This circuit can be operated either with n-phase or 2n-phase interleaved control. The voltage gain of the converter

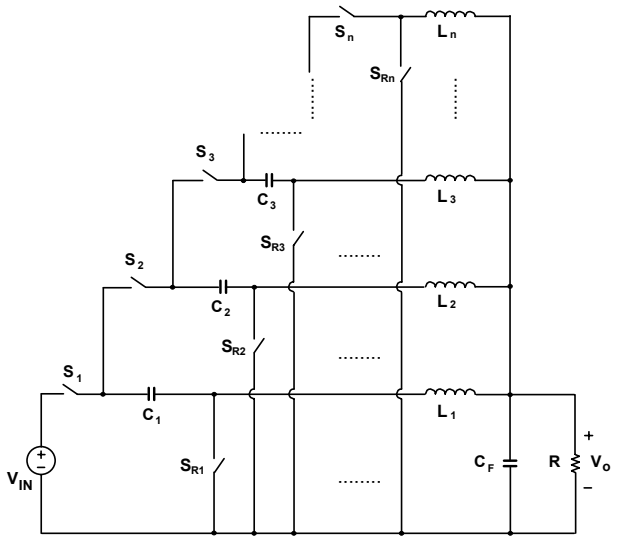

Fig. 7. Implementation of n-switch, n-inductor, step-down PWM converter.

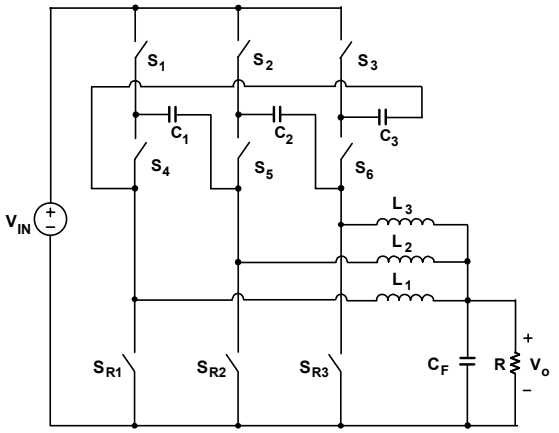

Fig. 8. Three-inductor, six-switch, step-down PWM converter.

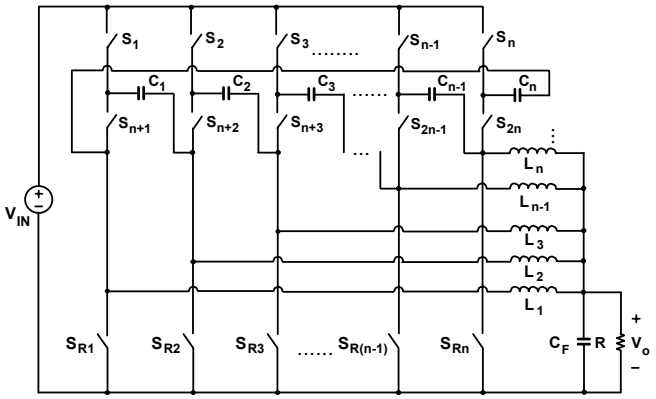

Fig. 9. Implementation of 2n-switch, n-inductor, step-down PWM converter.

shown in Fig. 9 is the same as that of the converter shown in Fig. 2(a).

Finally, it should be noted that the described concept of generating a family of multi-phase buck converters with high step-down gain can also be employed to derive a family of boost converters with increased step-up gain [11]. The gain of this family is identical to the gain of the boost converters introduced in [13].

III. Experimental Results

The operation and the performance of the proposed converters with extended duty cycle was verified on a two-phase, two-inductor converter in Fig. 1(a). The experimental 400-kHz prototype was designed for a 12-V input and a 1.25-V nominal output delivering a maximum current of 75 A. Each high-side switch (*i.e.*, S_1 and S_2) was implemented with a 20-V IRF6601 device, whereas each synchronous rectifier switch (*i.e.*, S_{R1} and S_{R2}) was implemented with two 20-V IRF6609 devices in parallel. Five 10-µF/16-V ceramic capacitors connected in parallel were used for blocking capacitor C_1, each with 5-mΩ ESR, resulting in a 1-mΩ total ESR. Inductors L_1 and L_2 were implemented with an inductance of 0.43-µH and winding resistance of 0.7-mΩ. In

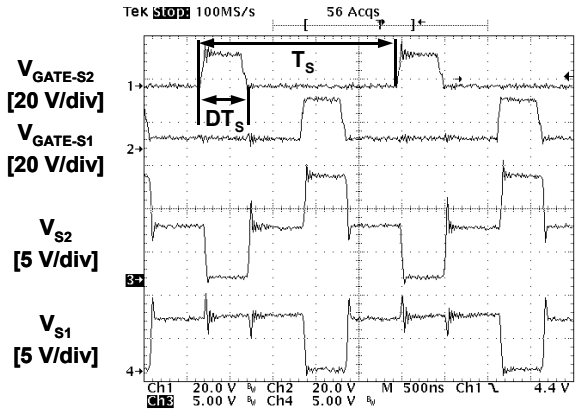

Fig. 10. Measured key waveforms of experimental prototype. From top to bottom: gate voltage $V_{GATE-S2}$ of S_2; gate voltage $V_{GATE-S1}$ of S_1; drain-source voltage V_{S2} of S_2; drain-source voltage V_{S1} of S_1. Time scale 500 ns/div.

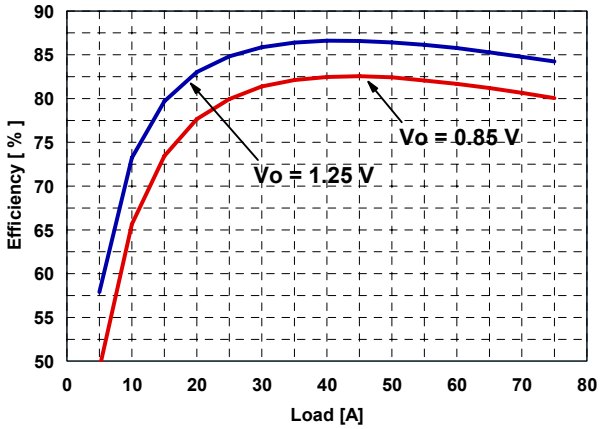

Fig. 11. Measured efficiencies of experimental prototype as functions of load current for V_O=1.25 V and V_O=0.85 V.

the absence of a dedicated multi-phase buck controller without a current-sharing loop, the general-purpose half-bridge voltage-mode controller ISL6740 from Intersil was employed. A pair of Intersil's ISL6613CB mosfet drivers was used to drive the switches.

The waveforms of gate voltages $V_{GATE-S1}$ and $V_{GATE-S2}$ of high-side switches S_1 and S_2 and their corresponding drain-to-source voltages V_{S1} and V_{S2}, measured at output voltage V_O=1.25 V and load current I_O=50 A, are shown in Fig. 10. As can be seen from the figure, the experimental converter operates with a duty cycle of 22%, which is twice as large as the duty cycle of the conventional buck converter with the same step-down ratio. Furthermore, by inspecting the drain-to-source voltage waveforms V_{S1} and V_{S2}, it can be seen that the experimental circuit exhibits lower voltage stress on switches S_1 and S_2 compared to its conventional counterpart. The peak voltage on switch S_1, including the parasitic ringing, is around 8 V, whereas the peak voltage on switch S_2 is around 13 V. Excluding the parasitic ringing voltage, the maximum voltage across switch S_1 is around 6 V, whereas the maximum voltage across switch S_2 is 12 V, *i.e.*, the maximum voltages of switches S_1 and S_2 are $V_{IN}/2$ and V_{IN}, respectively.

The measured efficiencies of the experimental converter for V_O=1.25 V and V_O=0.85 V as functions of the load current are shown in Fig. 11. The full-load efficiency of the experimental prototype is 84.2 % at V_O=1.25 V and 80.1 % at V_O= 0.85 V.

The measured full-load efficiencies are similar to those of the conventional two-phase buck converter built with the same components, which also has been confirmed in [12]. The full load efficiency of the proposed converter could be further improved by optimizing the high side switches. Generally, because high-side switches in the circuits of the proposed family exhibit larger conduction losses and reduced switching losses compared to those of their conventional counterparts, the optimized high-side switches should make a trade-off between the on-resistance and terminal capacitances in the direction of a reduced on-resistance. With optimized switches, the proposed converters have potential to show better performance than their conventional counterparts, especially as the switching frequency is pushed into the megahertz range.

IV. Summary

A family of multi-phase PWM step-down converters that feature a high voltage conversion ratio is introduced. The proposed multi-phase converters of the proposed family operate with larger duty cycles and lower voltage stresses on the switches than their conventional buck-converter counterparts. As a result, the proposed multi-phase converters are suitable for employment in high-frequency dc/dc applications with very high step-down ratios such as, for example, in VR applications.

References

[1] X. Zhou, X. Zhang, J. Liu, P. Wong, J. Chen, H. Wu, L. Amoroso, F. C. Lee, and D. Chen, "Investigation of Candidate VRM Topologies for Future Microprocessors", *IEEE Applied Power Electronics Conference Proc.*, Feb. 15-19, 1998, pp. 145-150.

[2] Y. Panov and M. Jovanović, "Design Considerations for 12-V/1.5-V, 50-A Voltage Regulator Modules", *IEEE Applied Power Electronics Conference Proc.*, Feb. 6-10, 2000, pp. 39-46.

[3] J. Wei and F. C. Lee, "A Novel Soft-Switched, High-Frequency, High-Efficiency, High-Current, 12-V Voltage Regulator – The Phase-Shift Buck Converter", *IEEE Applied Power Electronics Conference Proc.*, Feb. 9-13, 2003, pp. 724-730.

[4] Y. Ren, M. Xu, K Yao, Y. Meng, and F. C. Lee, "Two-stage approach for 12 VR", *IEEE Applied Power Electronics Conference Proc.*, Feb. 22-26, 2004, pp. 1306-1312.

[5] X. Zhou, B. Yang, L. Amoroso, F. C. Lee, and P-L. Wong, "A Novel High-Input-Voltage, High Efficiency and Fast Transient Response Voltage Regulator Module – Push-Pull Forward Converter", *IEEE Applied Power Electronics Conference Proc.*, Mar. 14-18, 1999, pp. 279-283.

[6] J. Guo, "Double-Ended Transformer-Based Multiphase Converters", *IEEE International Telecom. Energy Conference Proc.*, Oct. 19-23, 2003, pp. 104-109.

[7] Z. Yang, S. Ye, and Y. Liu, "A Novel Non-Isolated Half-Bridge Dc-Dc Converter", *IEEE Applied Power Electronics Conference Proc.*, Mar. 6-10, 2005, pp. 301-307.

[8] J. Wei, P. Xu, H. Wu, F. C. Lee, K. Yao, and M. Ye, "Comparison of Three Topology Candidates for 12-V VRM", *IEEE Applied Power Electronics Conference Proc.*, Mar. 4-8, 2001, pp. 245-251.

[9] P. Xu, J. Wei, K. Yao, Y. Meng, and F. C. Lee, "Investigation of Candidate Topologies for 12-V VRM", *IEEE Applied Power Electronics Conference Proc.*, Mar. 10-14, 2002, pp. 686-692.

[10] K. Yao, F. C. Lee, Y. Meng, and J. Wei, "Tapped-Inductor Buck Converters With A Lossless Clamp Circuit for 12-V VRM", *IEEE Applied Power Electronics Conference Proc.*, Mar. 10-14, 2002, pp. 693-698.

[11] Y. Jang and M. Jovanović, "Non-Isolated Power Conversion System Having Multiple Switching Power Converters", U.S. Patent Application 10/972,632, Oct. 26, 2004. Available at http://www.uspto.gov/patft/ after Apr. 27, 2006.

[12] K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "Analysis of Double Step-Down Two-Phase Buck Converter for VRM", *IEEE International Telecom. Energy Conference Proc.*, Sep. 18-22, 2005, pp. 497-502.

[13] L.C. Franco, L.L. Pfitscher, and R. Gules, "A New High Static Gain Non-Isolated Dc-Dc Converter," *IEEE Power Electronics Specialists Conf. (PESC) Proc.*, Jun. 15-19, 2003, pp. 1367-1372.