Multi-port Hybrid HVDC Circuit Breaker

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***Abstract*—This paper proposes a new n-port hybrid dc circuit breaker for offshore multi-terminal HVDC grid application. The n-port dc circuit breaker can substitute $n-1$ hybrid dc circuit breakers at a dc bus with $n-1$ adjacent dc transmission lines. The system level behavior of the proposed multi-port hybrid dc circuit breaker is similar to other hybrid dc circuit breakers. The operation principles of the proposed multi-port dc circuit breaker are introduced, analyzed and compared to the existing solution in this work. The components ratings are compared to the existing solution and the functionality of proposed device is verified by simulation.**

***Index Terms*—dc Circuit Breaker, Multi-terminal dc Grid, Fault Protection, Multi-port Device.**

I. Introduction

AS a consequence of the development of large offshore wind farms at large distances from the coast, there is an increasing need for formation of multi-terminal HVDC (MT-HVDC) grids. The voltage source converter (VSC) is identified as the key technology for realization of the MT-HVDC grid [1]. The MT-HVDC grid can connect different geographical areas with redundant transmission paths to benefit from the diversity of renewable energy resources while enhancing the supply reliability [2]. Although MT-HVDC grid potentially offers substantial benefits, its protection against short circuit fault is considered to be one of the main challenges, by academia and industry. One major issue relates to dc fault current interruption. The dc fault current interruption is especially difficult due to the lack of natural current zero crossing [3].

Several dc circuit breaker (DCCB) topologies have been introduced in the literature. The DCCBs can be categorized in three types including electromechanical (MCBs), pure solid-state (SSCBs) and hybrid dc circuit breakers [3], [4]. Traditional MCBs have a long operating time, in the order of 30-50 ms. Although recent developments have reduced the operating time significantly, with operating times in the range of 8-10 ms [5], it may not be still enough for the protection of MT-HVDC grid. The SSCBs can interrupt fault currents near instantaneously, and much faster than the MCBs [6]–[9]. However, compared to the MCBs, such breakers have high on-state losses as well as high capital costs [3], [4]. The combination of SSCB and MCB results in HCB configurations. The main current path in an HCB consists of a load commutation switch (LCS), which is composed of few semiconductor switches together with a mechanical switch [4]. When it is required to interrupt the flowing current, the current should be commutated into the parallel branch(s) by use of the LCS unit [10], [11]. The HCBs have lower on-state losses compared to SSCBs and have an operating time in the order of few milliseconds [10]–[12]. Since, the HCB introduced in [10] has been investigated extensively in the literature [13]–[17], it will be referred as typical HCB in this paper.

Although the typical HCB brings about many advantages in terms of current interruption time and power losses, it requires hundreds of semiconductor switches in its main breaker (MB) branch to tolerate the system voltage [18], hence its implementation cost is expected to be high. The number of required semiconductor switches for protection of a dc bus with two adjacent transmission lines would be comparable to that of a modular multilevel converter (MMC) station [18]. The economic complexity of HCBs can be much serious when their application in the future offshore MT-HVDC grids is considered. Such an MT-HVDC grid will be composed of large wind farms located in different geographical areas connected through several sub-marine HVDC cables. Hence, a considerable number of HCBs might be required to have a fully selective protected MT-HVDC grid [2], [19].

The reduction in the realization cost of HCBs has been a research subject in recent years. A thyristor based current limiting circuit [20] and a superconducting fault current limiter in series connection with HCB [21] can reduce the size of HCB surge arresters. An H-bridge realization of HCB can almost reduce the number of semiconductor switches in the main breaker branch by half while maintaining bidirectional interruption capability of HCB [22]. The topologies of unidirectional HCBs with reduced number of semiconductor switches are investigated in [23]. A novel current injection HCB with unidirectional main breaker unit has been proposed in [24].

The application of novel multi-port devices can be technically and economically attractive. For instance, a multi-port LCL based dc hub is proposed in [25]. This dc hub can interconnect several dc transmission lines in an MT-HVDC grid and control the power flow among them. Furthermore, the application of a multi-port dc/dc converter based on half-bridge topology in dc grid is investigated in [26]. Both mentioned proposals focus on the power flow control among different transmission lines while they can limit the propagation of dc fault in the MT-HVDC grid. However, their power losses can be a drawback for their application. This paper proposes a novel multi-port dc current interrupter device benefiting from the HCB core concept [12] for offshore MT-HVDC applications. The proposed DCCB has n ports and can interrupt the current at each of its ports independent of the other ports and irrespective of the current direction. Therefore, it is called multi-port hybrid dc circuit breaker (Mp-HCB). The Mp-HCB requires fewer switches in the MB and also in the load commutation switch (LCS)

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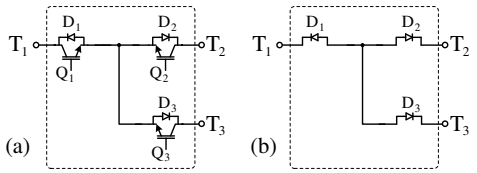

Fig. 1. Basic block of Mp-HCB, (a) ON (close) state, (b) OFF (open) state

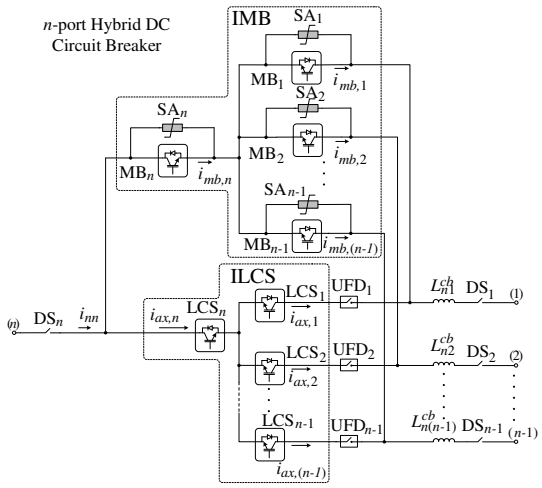

Fig. 2. n-port hybrid dc circuit breaker topology

compared to the HCB. Furthermore, the size of surge arresters for energy absorption can be significantly decreased.

The topology of proposed Mp-HCB is presented in section II and analyzed in section III. A comparison between the HCB and the Mp-HCB has been carried out in section V. The functionality of Mp-HCB is examined through a simulation study using a three-terminal grid model in section IV.

II. Multi-port Hybrid dc Circuit Breaker

A. Basic Representation

The basic representation for a 3-port switch consists of three IGBTs with antiparallel diodes is shown in Fig. 1(a). Although several states exist for the 3-port switch based on the states of IGBTs, only a couple of them are utilized for developing the proposed Mp-HCB. The first state of 3-port switch is the ON (close) state. In this state all the IGBTs are turned on and the 3-port switch has no impact on the current flow between the terminals (T_1-T_3). The second state of 3-port switch is the OFF (open) state and can be achieved by turning off all the IGBTs. As shown in Fig. 1(b), due to the arrangement of D_1-D_3, all the terminals are disconnected from each other in the open state. The 3-port switch concept can be generalized to an n-port switch.

B. Mp-HCB topology

The topology of proposed Mp-HCB with n ports is depicted in Fig. 2. The Mp-HCB is composed of an integrated main breaker (IMB), an integrated load commutation switch (ILSC), ultra-fast disconnectors (UFD_i), current limiting inductors (L_{ni}^{cb}), surge arresters (SA_i) and disconnectors (DS_i). Port n is assumed to be connected to a dc bus and ports 1 to $n-1$ are assumed to be connected to $n-1$ adjacent transmission lines. Fig. 3(a) shows an n-terminal dc system protected by the

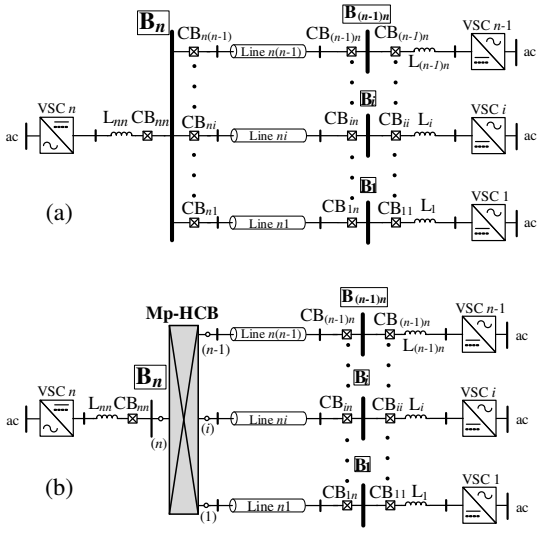

Fig. 3. Multi-terminal dc grid protected by: (a) hybrid dc circuit breakers, (b) multi-port hybrid dc circuit breaker

HCBs. As shown in the figure, the HCBs are placed at ends of all transmission lines to achieve full protection selectivity. Although the number of DCCBs might be reduced based on the grid requirements, a fully protected grid is considered in this study [27]. Fig. 3(b) depicts similar system when $n-1$ HCBs at dc bus n (B_n) are replaced by an n-port Mp-HCB. The SAs, UFDs and DSs are similar to the typical ones used in the HCBs [12]. The Mp-HCB has two new integrated modules:

1) Integrated main breaker unit (IMB): As shown in Fig. 2, the IMB unit consists of n MB subunits. The MB subunits consist of series connected IGBTs. Contrary to the MB unit of typical HCB, the MB subunits of Mp-HCB are not bidirectional switches. The unidirectional MB subunits are integrated together to form a multidirectional IMB unit. Similar to the n-port switch basic representation, the IMB has two states (ON and OFF) depending on the states of MB subunits.

2) Integrated load commutation switch (ILCS): The ILCS consists of n LCS subunits. The ILCS is in the ON state when all the LCS subunits are closed and is in the OFF state when the LCS subunits are opened. The LCS subunit can be realized by one IGBT or series connection of few IGBTs similar to the LCS of typical HCB due to the reduced voltage requirements [12].

C. Operation principles

The Mp-HCB operation principles can be separated into three modes: normal conduction, current interruption and reclosing.

1) Normal conduction mode: In the normal conduction mode, the ILCS together with UFD_1-UFD_{n-1} and DS_1-DS_n are closed whereas the IMB is in the open state. The equivalent circuit of Mp-HCB in this mode is similar to Fig. 4(a). Therefore, the power flow can be maintained between the dc bus and the adjacent lines irrespective of its direction.

2) Fault current interruption mode: The Mp-HCB can receive n independent trip commands. Upon receiving a trip command from a line or the bus protection relay, the corresponding port(s) of Mp-HCB must interrupt(s) its(their) current(s).

a) Fault on adjacent transmission line i (Port i): Line i is connected to port i of the Mp-HCB where $i=1,2,...,n-1$. Hence, to clear a permanent fault on line i, port i of the Mp-HCB should trip. It is assumed that the fault incepts at $t=0$ s

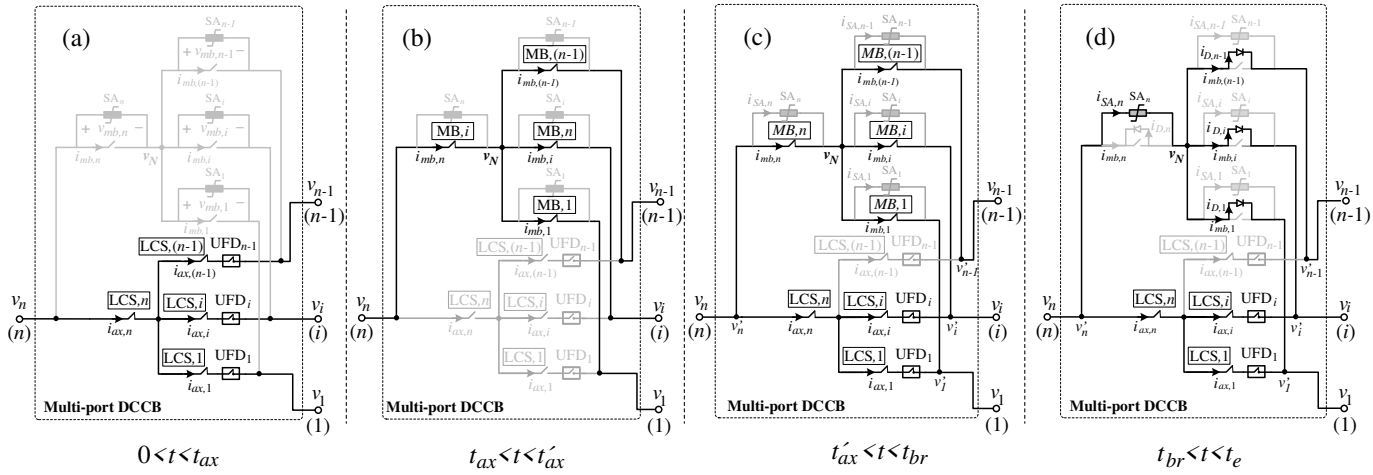

Fig. 4. Operation stages of multi-port hybrid dc circuit breaker

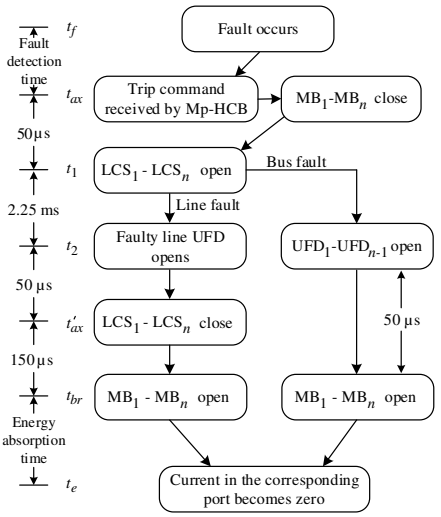

Fig. 5. Line and bus faults isolation process

and the trip command for port i is received at time $t=t_{ax}$. Fig. 4(a) depicts the equivalent circuit of Mp-HCB for $0<t\leq t_{ax}$. The fault current flows through the ILCS during this time period. Upon receiving the trip command, the IMB is closed and then the ILCS is opened in order to commutate the currents into the IMB. Due to the fast turn-on and turn-off of IGBTs, the current commutation time is expected to be in the range of few tens of micro-seconds [16]. The rate of rise of current would slightly be reduced after current commutation is done due to the larger number of IGBTs in the IMB and its higher stray inductance compared to the ILCS. However, the variation is negligible and has no remarkable impact on the fault current. In order to ease the explanation of Mp-HCB operation, the current commutation is assumed to be done instantaneously. After completion of the current commutation at t_{ax}, UFD$_i$ should be opened. During UFD$_i$ operation delay, the fault current flows through the MB subunits. Fig. 4(b) shows the equivalent circuit for this stage. UFD$_i$ operation is assumed to be accomplished at time t'_{ax} and thereafter the ILCS should be closed. This stage of the Mp-HCB operation is depicted in Fig. 4(c). When the ILCS is closed in this stage, some of the MB subunits share their current with some of the LCS subunits. This stage is named as current sharing stage. Although the ILCS is closed, the current cannot flow through LCS$_i$ into the port i due to the open state of UFD$_i$. Nevertheless, the fault current can still flow into the faulty line via MB$_i$. Considering a fast fault current interruption strategy, after closing the ILCS, the IMB unit should be opened to interrupt the fault current. After opening the IMB at $t=t_{br}$, the currents of healthy lines can flow though the corresponding LCS subunits whereas the fault current is commutated into the surge arresters in the IMB unit as shown in Fig. 4(d). Finally, the released energy is absorbed in SA$_1$-SA$_n$ by $t=t_e$. Note that due to the presence of antiparallel diodes of MB$_i$ the current cannot be redirected into SA$_i$. To provide electrical isolation DS$_i$ can be opened. Fig. 5 illustrates the line fault isolation process and related timings.

b) Fault at dc bus (port n): Upon detection of a permanent dc bus fault, all adjacent lines must be isolated from the dc bus. Therefore, after receiving dc bus fault trip command the IMB should be closed and the ILCS should be opened in order to commutate the current into the IMB (at $t=t_{ax}$). Following the current commutation completion, UFD$_1$-UFD$_{n-1}$ can be opened. Finally, the IMB should be opened (at $t=t_{br}$) and the currents will be redirected into the SAs. The electrical isolation can be provided by opening DS$_n$. The sequential bus fault interruption process is shown in Fig. 5.

c) Recloser mode: The reclosing mode might be required before completely opening of the Mp-HCB. The Mp-HCB can be reclosed by reclosing the IMB after opening the UFD$_i$. The equivalent circuits of reclosing mode are equal to Fig. 4(c) and (d). Finally, in case of a non-permanent fault, the UFD$_i$ can again be closed and the Mp-HCB shifts to its normal conduction state by closing the ILCS and opening the IMB.

III. Analysis

The internal operation of Mp-HCB is analyzed through the simplified model of dc system depicted in Fig. 3. The analyzed network is an n-terminal grid where dc buses B$_1$-B$_{n-1}$ are connected through $n-1$ transmission lines to dc bus B$_n$. It is clear that the Mp-HCB operation does not depend on the grid topology. In a fully selective protection scheme HCBs are attached between the dc lines and the dc bus and also at dc side of the converter station [2], [27]. This protection

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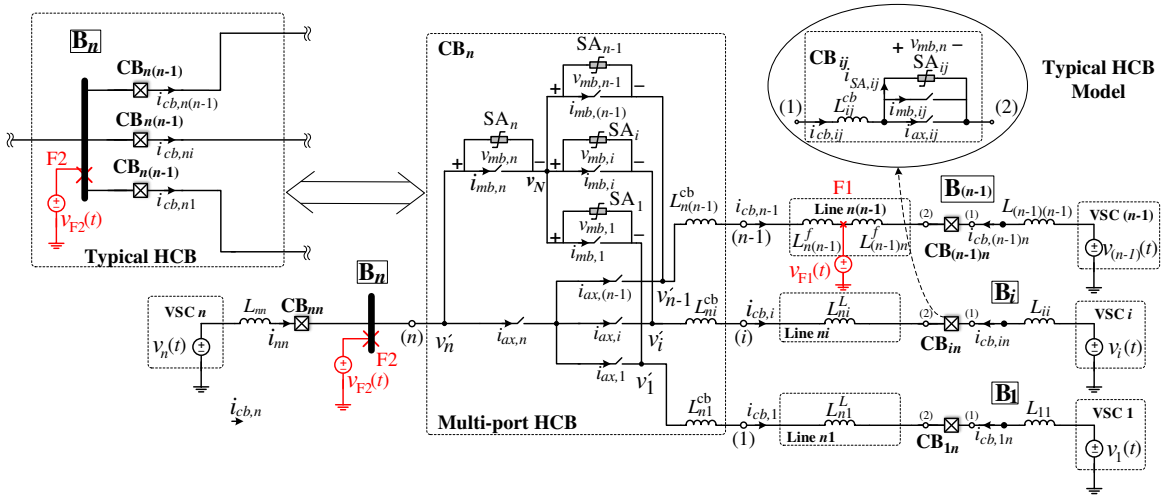

Fig. 6. Equivalent circuit of test system in presence of Mp-HCB

scheme will be referred as the typical scheme in this paper. In order to compare the proposed approach with the typical scheme, similar analysis has been carried out for the system based on the typical HCBs. The schematic of typical HCB [10] and its internal currents and voltages are shown in Fig. 6. To perform the analysis, the following aspects are considered:

- Simple (RL-equivalent) model of the transmission line is used in order to clarify the internal operation of the Mp-HCB and avoid variation in rate of rise of fault current.
- Detailed models of HCB [16] and Mp-HCB are used and the current limiting inductor is considered as a part of DCCB.
- The permanent dc fault and prompt fault interruption strategy are considered [27].
- Voltage at dc buses are assumed to be constant during the DCCB operation time [28].
- Short circuit fault is modeled by a voltage source, whose value is equal to the system steady-state voltage value in normal condition and it changes to 0 V when a fault happens.

A. Transmission line fault F_1 and Mp-HCB

The equivalent circuit is depicted in Fig. 6. A low impedance ($R_{fault} \approx 0\ \Omega$) pole-to-ground fault occurs on line $n-1$ at point F_1 at $t=0$ s. The voltage at fault location (v_{F1}) becomes zero after fault occurs. The following equations can be given considering the initial conditions and assumptions:

$$\begin{aligned} &v_{F1}(0)=V_{dc},\\ &v_{F1}(0^+)=0,\\ &v_j(t)=V_{dc};\quad 0<t\le t_{br},\quad j=1,...,n,\\ &i_{cb,j}(0)=I_{pre,j};\quad j=1,...,n. \end{aligned} \tag{1}$$

In (1) $v_{F1}(t)$, $v_j(t)$ and $I_{pre,j}$ represent the voltage at fault location, dc bus B_j voltage and pre-fault current in port j of the Mp-HCB. t_{br} represents the current interruption instant. The current at port j can be given as follows for $j=1,...,n-2,n$:

$$i_{cb,j}(t)=\begin{cases} i_{ax,j}(t), & 0<t\le t_{ax}\\ i_{mb,j}(t), & t_{ax}<t\le t'_{ax}\\ i_{mb,j}(t)+i_{ax,j}(t), & t'_{ax}<t\le t_{br}\\ i_{SA,j}(t)+i_{ax,j}(t), & t_{br}<t\le t_e \end{cases}, \tag{2}$$

and for $j=n-1$:

$$i_{cb,j}(t)=\begin{cases} i_{ax,j}(t), & 0<t\le t_{ax}\\ i_{mb,j}(t), & t_{ax}<t\le t'_{ax}\\ i_{mb,j}(t), & t'_{ax}<t\le t_{br}\\ i_{mb,j}(t), & t_{br}<t\le t_e \end{cases}, \tag{3}$$

We replace the sum of line jn inductance (L^L_{jn}), faulty line corresponding port current limiting inductor value (L^{cb}_{nj}), the remote end HCB limiting inductor (L^{cb}_{jn}) and the remote dc bus filter inductor (L_{jj}) by L'_{nj}:

$$\begin{aligned} &L'_{nj}=L^{cb}_{nj}+L^L_{jn}+L^{cb}_{jn}+L_{jj}\quad for\quad j=1,...,n,\\ &L'_{nn}=L_{nn}+L^{cb}_{nn}. \end{aligned} \tag{4}$$

Therefore, the rate of rise of current at port $n-1$, which is equal to that of the fault current for $t=0^+$ when the transmission line resistance is neglected can be given as follows:

$$\frac{\mathrm{d}i_{cb,n-1}(0^+)}{\mathrm{d}t}=\frac{V_{dc}\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)}{1+\left(L^{cb}_{n(n-1)}+L^f_{n(n-1)}\right)\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)} \tag{5}$$

where $L^f_{n(n-1)}$ represents the inductance between port $n-1$ and the fault location. The current derivative at the other ports of Mp-HCB for $i=1,...,n-2,n$ can be given as:

$$\frac{\mathrm{d}i_{cb,i}(0^+)}{\mathrm{d}t}=\frac{-V_{dc}}{L'_{ni}\left(1+\left(L^{cb}_{n(n-1)}+L^f_{n(n-1)}\right)\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)\right)} \tag{6}$$

The current in MB and LCS subunits can be obtained using (2), (3), (5) and (6). The maximum current at interruption instant sets the current requirements of the subunits.

1) Main breaker (MB) subunits: The IMB is in ON state when $t_{ax}<t<t_{br}$. Therefore, the current in MB subunits can be evaluated considering two time periods as follows:

a) $t_{ax}<t<t'_{ax}$: (2) and (3) illustrate that the current in MB subunits is equal to the current in the corresponding port for $t_{ax}<t<t'_{ax}$. Assuming instantaneous current commutation at $t=t_{ax}$ and using (5) and (6), the current in MB subunits for $i=1,...,n-2,n$ can be given as:

$$i_{mb,i}(t)=I_{pre,i}+\frac{sgn(i-n+1)V_{dc}t}{L'_{nn}\left[1+\left(L^{cb}_{n(n-1)}+L^f_{n(n-1)}\right)\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)\right]} \tag{7}$$

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and for $i=n-1$:

$$i_{mb,i}(t)=I_{pre,i}+\frac{V_{dc}\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)t}{1+\left(L^{cb}_{n(n-1)}+L^{f}_{n(n-1)}\right)\left(\frac{1}{L'_{nn}}+\sum_{j=1}^{n-2}\frac{1}{L'_{nj}}\right)} \quad (8)$$

b) $t'_{ax} < t < t_{br}$: In addition to the MB subunits, LCS_1-LCS_{n-2} and LCS_n conduct when $t'_{ax}<t<t_{br}$. LCS_{n-1} cannot conduct the current since DS_{n-1} is in open position. Fig. 4(c) shows the equivalent circuit of the Mp-HCB for this time period. The MBs have several IGBTs in series whereas the LCSs have only few IGBTs. The on-state voltage drop on an MB can be hundred times larger than the on-state voltage drop of LCS. Hence, the voltage drop on LCSs can be neglected against that of MB subunits. Therefore, the following equation can be given considering Fig. 4(c):

$$v'_1\approx v'_2\approx ...\approx v'_{n-2}\approx v'_n, \quad t'_{ax}<t\leq t_{br} \quad (9)$$

v'_1 - v'_n are illustrated in Fig. 4(c). Based on (9), MB_1, MB_2, ..., MB_{n-2} and MB_n can be considered as parallel branches during the mentioned time period and their currents will be almost equal. Therefore, the current in the mentioned MB subunits can be given by:

$$i_{mb,j}(t)=\frac{i_{mb,n-1}(t)}{n-1}, j=1,2,...,n-2,n \quad (10)$$

The current in MB_{n-1} is equal to the current in its corresponding port and holds the same equation as (8).

2) Load commutation switch (LCS) subunits: As was explained, the ILCS conducts the current in two periods of time. In the first stage (when $0<t<t_{ax}$), the current in LCS_j holds the same equations as (7) and (8) and its maximum happens at $t=t_{ax}$. Considering (2) and Fig. 4(c), the current in the LCS subunits for $t'_{ax}<t<t_{br}$ can be given as follows:

$$i_{ax,j}(t)=i_{cb,j}(t)-i_{mb,j}(t), \quad j=1,2,...,n-2,n \quad (11)$$

The second maximum of current in the LCS subunits occurs at time t_{br}, which can be obtained by evaluating (11) at $t=t_{br}$.

3) Surge arresters (SA): Surge arresters possess a non-linear $V-I$ characteristic. Only for comparison purposes, ideal SAs are considered by assuming their voltage to be constant until their current falls to zero for both proposed and typical schemes. It is assumed that the SA current reaches its maximum instantaneously at $t=t_{br}$ and then decreases linearly and reaches zero at $t=t_e$. Neglecting the practical mismatch between $V-I$ characteristics of surge arresters, the current can be given as:

$$|i_{SA,j}|=\left|\frac{i_{mb,n-1}}{n-1}\right|, \quad j=1,2,...,n-2,n \quad (12)$$

The current and hence the energy in SA_{n-1} are zero due to the conduction of antiparallel diodes of MB_{n-1}. Considering (9) it can be assumed that SA_1, SA_2, ?, SA_{n-2} and SA_n operate in parallel connection. The overvoltage protection voltage of each surge arrester is assumed to be equal to V_{ovp}. The maximum total absorbed energy in all the surge arresters holds:

$$E_{SA,T}=\int_{t_{br}}^{t_e}V_{ovp}\cdot i_{cb,n-1}(t)dt \quad (13)$$

The maximum absorbed energy in SA_j can be given as:

$$E_{SA,j}=\frac{V_{ovp}I^{cb,n-1}_{max}(t_e-t_{br})}{2(n-1)}; \quad j=1,...,n-2,n, \quad (14)$$

B. dc bus fault F_2 and Mp-HCB

As shown in Fig. 6, a low impedance pole-to-ground fault ($R_{fault}\approx 0\ \Omega$) occurs at dc bus n at $t=0$ s. The initial conditions and study assumptions are similar to (1) and also similar approach to subsection III-A is used for analysis. The current at port j for various time periods can be given by:

$$i_{cb,j}(t)=\begin{cases} i_{ax,j}(t), & 0<t\leq t_{ax} \\ i_{mb,j}(t), & t_{ax}<t\leq t_{br} \\ i_{SA,j}(t), & t_{br}<t\leq t_e \end{cases} \quad (15)$$

Using similar approach to section III-A. the rate of rise of current at ports of Mp-HCB can be given as follows:

$$\frac{\mathrm{d}i_{cb,n}(0^+)}{\mathrm{d}t}=V_{dc}\sum_{j=1}^{n-1}\frac{1}{L'_{nj}}; \quad i=n,$$
$$\left|\frac{\mathrm{d}i_{cb,i}(0^+)}{\mathrm{d}t}\right|=\frac{V_{dc}}{L'_{ni}}; \quad i=1,2,...,n-1. \quad (16)$$

1) Main breaker (MB) subunits: The currents of MB subunits during $t_{ax}<t\leq t_{br}$ can be given as:

$$i_{mb,i}(t)=\begin{cases} I_{pre,i}-\frac{V_{dc}}{L'_{nj}}t; & i=1,2,...,n-1 \\ I_{pre,i}-V_{dc}\sum\limits_{j=1}^{n-1}\frac{1}{L'_{nj}}t; & i=n \end{cases} \quad (17)$$

The maximum current in MB_j ($I^{mb,j}_{max}$) is reached at $t=t_{br}$.

2) Load commutation switch (LCS) subunits: Despite the line fault scenario, the current in LCS subunits has one maximum at $t=t_{ax}$ and can be given as:

$$I^{ax,i}_{max}(t)=\begin{cases} I_{pre,i}-\frac{V_{dc}}{L'_{nj}}t_{ax}; & i=1,2,...,n-1 \\ I_{pre,i}-V_{dc}\sum\limits_{j=1}^{n-1}\frac{1}{L'_{nj}}t_{ax}; & i=n \end{cases} \quad (18)$$

3) Surge arresters (SA): The SA current can be given as:

$$|i_{SA,j}|=\left|\frac{i_{mb,n}}{n-1}\right|, \quad j=1,2,...,n-2,n-1 \quad (19)$$

Depending on the length of adjacent lines, the absorbed energy in the surge arresters of the Mp-HCB and also the energy absorption time ($t_{e,j}-t_{br}$) can be different for each surge arrester. Due to conduction of antiparallel diode D_n, the current in SA_n remains zero and consequently the absorbed energy in SA_n is also zero. The absorbed energy in SA_j can be given by:

$$E_{SA,j}=\frac{V_{ovp}I^{mb,j}_{max}(t_{e,j}-t_{br})}{2}, \quad j=1,2,...,n-1 \quad (20)$$

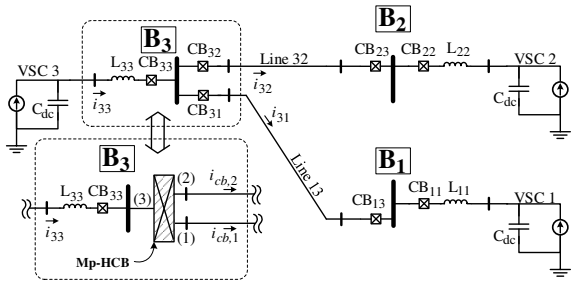

Fig. 7. Mp-HCB and HCBs in the thee-terminal test grid

C. Transmission line fault and HCB

As shown in Fig. 6, the Mp-HCB can be replaced by $n-1$ HCBs at B_n. A detailed schematic of the HCB is illustrated in the figure. Similar fault analysis to subsections III-A and III-B have been carried out. It is assumed that only the MB unit of corresponding HCB of the faulty line is activated. For sake of brevity, only the most relevant equations are included.

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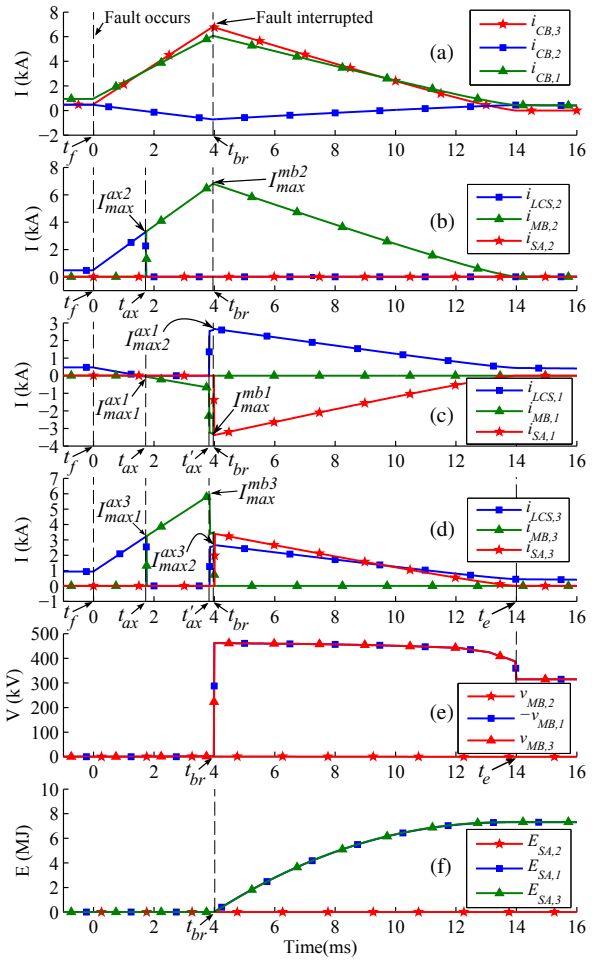

Fig. 8. Mp-HCB during line fault at line 32 of three-terminal grid

1) Load commutation switch (LCS) subunits: The LCS current in $CB_{n(n-1)}$ reaches its maximum at $t=t_{ax}$ whereas the current in LCS unit of CB_{ni} reaches its maximum at $t = t_{br}$. The maximum current in LCS unit of CB_{ni} for $n=1,2,...,n-2,n$ can be given by:

$$I_{max}^{ax,i}=I_{pre,i}+\frac{sgn(i-n+1)V_{dc}t_{br}}{1+\left(L_{n(n-1)}^{cb}+L_{n(n-1)}^{f}\right)\left(\frac{1}{L_{nn}^{l}}+\sum_{j=1}^{n-2}\frac{1}{L_{nj}^{l}}\right)} \quad (21)$$

and for $i=n-1$:

$$I_{max}^{ax,i}=I_{pre,i}-\frac{V_{dc}\left(\frac{1}{L_{nn}^{l}}+\sum_{j=1}^{n-2}\frac{1}{L_{nj}^{l}}\right)t_{ax}}{1+\left(L_{n(n-1)}^{cb}+L_{n(n-1)}^{f}\right)\left(\frac{1}{L_{nn}^{l}}+\sum_{j=1}^{n-2}\frac{1}{L_{nj}^{l}}\right)} \quad (22)$$

2) Main breaker (MB) subunits: The current in MB unit of $CB_{n(n-1)}$ for $t_{ax}<t\le t_{br}$ can be given as:

$$i_{mb,n-1}(t)=I_{pre,n-1}-\frac{V_{dc}\left(\frac{1}{L_{nn}^{l}}+\sum_{j=1}^{n-2}\frac{1}{L_{nj}^{l}}\right)t}{1+\left(L_{n(n-1)}^{cb}+L_{n(n-1)}^{f}\right)\left(\frac{1}{L_{nn}^{l}}+\sum_{j=1}^{n-2}\frac{1}{L_{nj}^{l}}\right)} \quad (23)$$

3) Surge arresters (SA): The current in surge arresters of all the HCBs are zero except the faulty line HCB ($SA_{n(n-1)}$). The absorbed energy in the surge arrester can be given by:

$$E_{SA,n(n-1)}=\frac{V_{ovp}I_{max}^{mb,n(n-1)}\left(t_{e,n(n-1)}-t_{br}\right)}{2} \quad (24)$$

D. dc bus fault and HCB

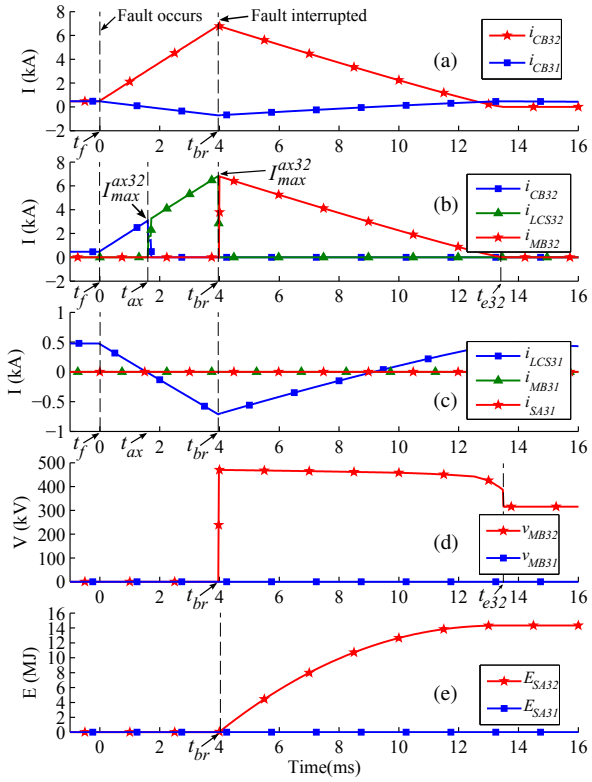

Fig. 9. HCBs during line fault at line 32 of three-terminal grid

1) Load commutation switch (LCS) subunits: During the bus fault, all the adjacent HCBs of the faulty dc bus are activated. The maximum current in the LCS unit of all the adjacent HCBs ($I_{max}^{ax,ni}$) can be given as:

$$I_{max}^{ax,ni}=I_{pre,ni}-\frac{V_{dc}}{L_{ni}^{l}}t_{ax};\quad i=1,2,...,n-1 \quad (25)$$

2) Main breaker (MB) subunits: The current in MB units for $0<t\le t_{br}$ can be given as:

$$i_{mb,ni}(t)=I_{pre,ni}-\frac{V_{dc}}{L_{ni}^{l}}t;\quad i=1,2,...,n-1 \quad (26)$$

3) Surge arresters (SA): The absorbed energy in SA_{nj} can be given by (27).

$$E_{SA,nj}=\frac{V_{ovp}I_{max}^{mb,nj}\left(t_{e,nj}-t_{br}\right)}{2},\quad j=1,2,...,n-1 \quad (27)$$

IV. Simulation Results

The three-terminal grid model is shown in Fig. 7. Two HCBs (CB_{31} and CB_{32}) at bus 3 are replaced by a 3-port Mp-HCB. The parameters of test system are illustrated in Table IV. The simulation studies are carried out in an electromagnetic transient type software namely PSCAD. The timings of internal operation stages of the Mp-HCB is implemented based on Fig. 5. The overvoltage protection voltage of surge arresters and the inductance of current limiting inductors are set to 460 kV and 50 mH, respectively. The transmission lines are protected by overcurrent protection scheme. The line fault trip command is sent to the corresponding DCCBs when the line current exceeds 2.8 kA. The dc buses of grid are protected by differential protection scheme. In this scheme, when the sum of incoming and outgoing currents at a dc bus becomes non-zero, the dc bus trip signal is activated. The dc bus fault measurement and identification delay is also considered and set to 1 ms.

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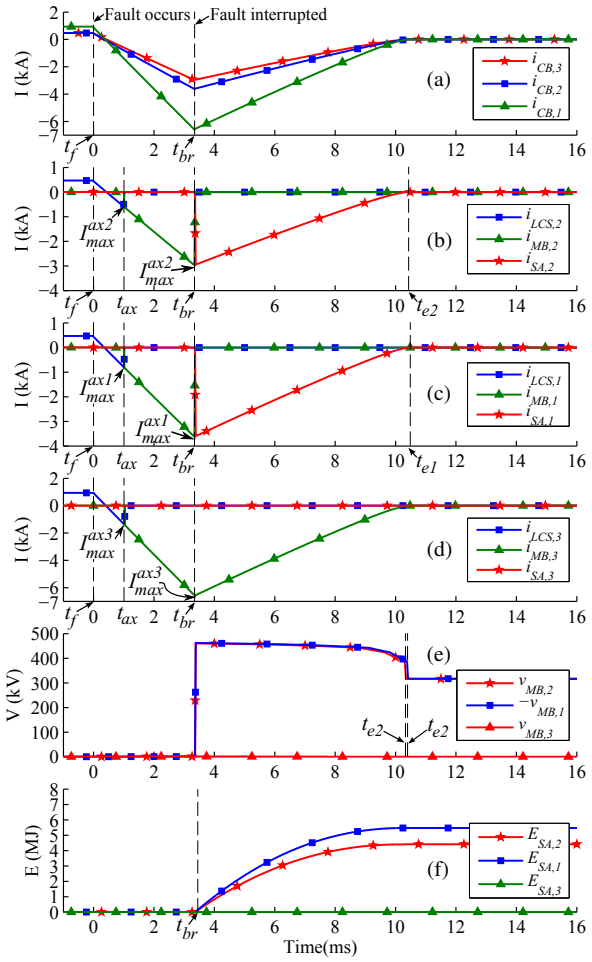

Fig. 10. Mp-HCB during bus fault at bus 3 of three-terminal grid

A. Transmission line Fault

A low impedance pole-to-ground fault (100 mΩ) is placed at the middle of line 32 at time 0 s. In HCB based protection, CB_{32} and CB_{23} and in case of Mp-HCB based protection, CB_{32} and port 2 of Mp-HCB should trip. Fig. 8 and 9 show the waveforms for Mp-HCB and HCBs, respectively. The important numerical values obtained from simulation and analysis are also illustrated in Table I. Comparing Fig. 8(a) and Fig. 9(a) confirms that the behavior of typical and proposed DCCBs from grid point of view are similar. Slight difference (25 A) in the interrupted currents of HCB and Mp-HCB is observed due to the additional time, which is considered in the modeling of current sharing stage in Mp-HCB. Fig. 8(b)-(d) depict the current in the subunits of Mp-HCB. As can be seen in Fig. 9(b) and (c), CB_{31} has no internal operation whereas the fault current is commutated into the MB unit in CB_{32}. Fig. 8(b) and Fig. 9(b) show that the trip command is received by the corresponding DCCBs at $t_{ax} = 1.7$ ms and then the current is commutated into the corresponding (I)MB unit. Table I illustrates that the simulation results are in agreement with the analysis in section III. As can be seen in Fig. 8(f) and Fig. 9(e), the absorbed energy in the surge arrester of HCB is almost equal to twice the absorbed energy in each surge arrester of Mp-HCB.

B. dc bus Fault

A low impedance pole-to-ground fault (100 mΩ) is placed at bus B_3. The differential protection relay activates the trip

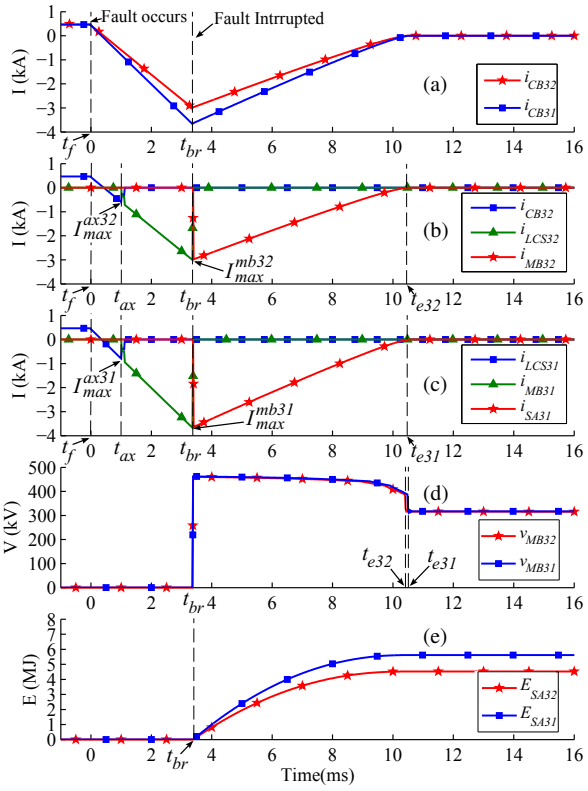

Fig. 11. HCB during bus fault at bus 3 of three-terminal grid

signal at almost $t = 1$ ms. In HCB based protection CB_{33}, CB_{31} and CB_{32} and in Mp-HCB based protection CB_{33} and all the ports of Mp-HCB should trip. Fig. 10 and 11 depicts the waveforms of Mp-HCB and HCBs, respectively. It can be seen in Fig. 10(b)-(d) that the fault current is commutated into MB subunit for all ports. In contrary with MB_1 and MB_2, the current in MB_3 does not redirected to the surge arrester due to explained reason in section III. The most relevant numerical values obtained from analysis and simulation are illustrated in Table II. The obtained approximated values from analysis are close to the values obtained from simulation of simplified model. The maximum current in MB_{31} and MB_1 and also in MB_{32} and MB_2 are equal. Moreover, the maximum current in LCS_{31} and LCS_1 and also in LCS_{32} and LCS_2 are equal. The current in MB_3 of Mp-HCB reaches 6.62 kA, which is higher than the currents of other subunits. However, this does not necessarily mean that the antiparallel diodes of MB_3 should be rated for higher current than the antiparallel diodes of MB_1 and MB_2. In fact, MB_1 and MB_2 may be required to carry higher currents during a line fault and should be rated for that. Fig. 10(e) and 11(d) illustrate that equal amount of energy absorbed in SA_1 and SA_{31} and also in SA_2 and SA_{32}.

C. Power flow

The currents flowing from the dc bus and the transmission lines in presence of the Mp-HCB are depicted in Fig. 12. Fig. 12(a) and (b) depict the currents for dc bus B_3 and line 32 fault scenarios, respectively. Moreover, Fig. 13 illustrates the currents flowing from the dc bus and the transmission lines in presence of the HCBs. Fig. 13(a) and (b) depict the currents for dc bus B_3 and line 32 fault scenarios, respectively. In all scenarios, the fault happens at time $t = 0$ s. The behavior

TABLE I
MP-HCB AND HCB PARAMETERS DURING LINE FAULT

Parameters	Mp-HCB		HCB	
Mp-HCB (HCB)	Analysis	Simulation	Analysis	Simulation
$I_{max1}^{ax,2}(I_{max}^{ax,2})[kA]$	3.198	3.190	3.198	3.190
$I_{max}^{mb,2}(I_{max}^{mb,2})[kA]$	6.84	6.83	6.82	6.81
$E_{SA,2}(E_{SA,32})[MJ]$	0	10^{-7}	14.844	14.340
$E_{SA,1}(E_{SA,31})[MJ]$	7.422	7.315	0	0
$E_{SA,3}[MJ]$	7.422	7.333	-	-

TABLE II
MP-HCB AND HCB PARAMETERS DURING BUS FAULT

Parameters	Mp-HCB		HCB	
Mp-HCB (HCB)	Analysis	Simulation	Analysis	Simulation
$I_{max}^{ax,1}(I_{max}^{ax,31})$ [kA]	-0.76	-0.78	-0.76	-0.78
$I_{max}^{ax,2}(I_{max}^{ax,32})$ [kA]	-0.56	-0.54	-0.56	-0.54
$I_{max}^{ax,3}$ (-) [kA]	-1.32	-1.35	-	-
$I_{max}^{mb,1}(I_{max}^{mb,31})$ [kA]	-3.64	-3.62	-3.64	-3.62
$I_{max}^{mb,2}(I_{max}^{mb,32})$ [kA]	-2.97	-2.96	-2.97	-2.96
$I_{max}^{mb,3}$ (-) [kA]	-6.62	-6.59	-	-
$E_{SA,1}(E_{SA,31})$ [MJ]	5.661	5.478	5.661	5.472
$E_{SA,2}(E_{SA,32})$ [MJ]	4.492	4.415	4.492	4.411
$E_{SA,3}(-)$ [MJ]	0	2×10^{-6}	-	-

of Mp-HCB has been found out to be similar to the typical scheme during normal operation and fault condition from the grid point of view. Fig. 12 shows that the Mp-HCB can clear a single line fault without tripping all its ports.

V. COMPARISON

The proposed Mp-HCB is compared to the typical HCB in this section. As seen in Fig. 3(a), to protect a dc bus with $n-1$ adjacent lines and one converter station with an asymmetric monopole HVDC configuration, n HCBs are required. The number of HCBs can be doubled in symmetric monopole and bipole configurations. Although the comparison study is done for asymmetric monopole configuration, it is valid for other mentioned configurations. As shown in Fig. 3(b), the HCBs can be replaced by an n-port Mp-HCB. The converter station HCB (CB_{nn}) will not be removed. Therefore, the requirements of CB_{nn} in both cases are equal and will not be compared and included in calculations. Table III compares different aspects of both the proposed and typical devices assuming $t'_{ax} \approx t_{br}$.

A. Load commutation switches

The maximum current in the LCS unit of HCB_{nj} is equal to the first maximum current in LCS_j in Mp-HCB for line fault scenario. Depending on the grid topology, the second maximum current in the LCS subunits of Mp-HCB might be greater as compared to the typical HCB. During the dc bus fault condition the current in LCS_1-LCS_{n-1} of Mp-HCB are equal to the current in LCS units of HCB_{n1}-$HCB_{n(n-1)}$. The current in LCS_n is equal to sum of currents in LCS_1-LCS_{n-1} of Mp-HCB and therefore is higher than the currents in other subunits. Note that the current in LCS_n flows through the antiparallel diode D_n during the bus fault. However, considering the most severe power flow scenario in the normal condition, the current flowing through LCS_n can be equal to the sum of currents flowing though LCS_1-LCS_{n-1} and hence LCS_n may require additional parallel branches. In the worst case, the number of parallel branches in LCS_n can be equal to the number of adjacent transmission lines if similar

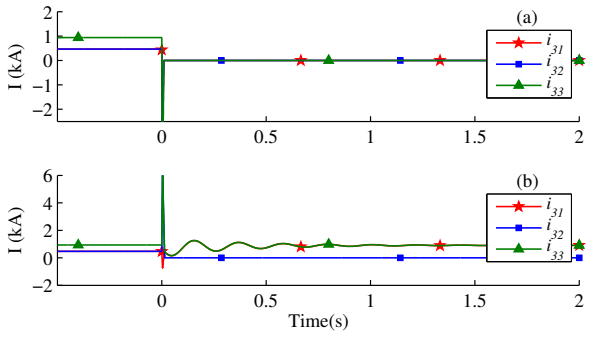

Fig. 12. Transmission lines and dc bus currents in Mp-HCB based scheme during fault at a) dc bus B_3, b) line 32

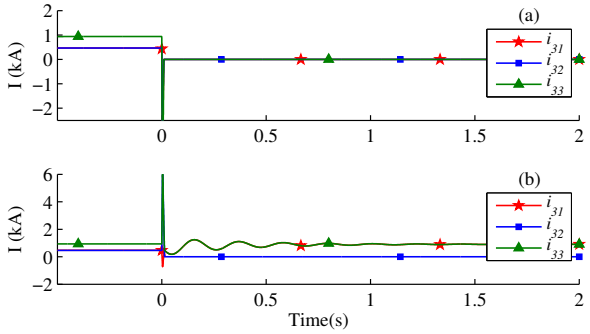

Fig. 13. Transmission lines and dc bus currents in HCB based scheme during fault at a) dc bus B_3, b) line 32

IGBTs are used for realization of all LCS subunits. Hence, the current rating of the IGBTs are equal. Fig. 14(a) shows the total number of required IGBTs for LCS units of HCB and Mp-HCB for protecting a dc bus with $n-1$ adjacent lines. The figure is plotted using Table III and assuming V_{ovp}=460 kV and V_{CES}=4.5 kV. V_{CES} represents the collector-emitter voltage of IGBTs. It can be seen that in the worst case, the number of required IGBTs in the LCS subunits of Mp-HCB based protection and the HCB based protection are identical.

B. Main breaker units

During the line fault the current in corresponding MB (sub)units of the Mp-HCB and HCB are equal. Similar to the previous subsection, the antiparallel diodes of subunit n of IMB in Mp-HCB may need to be able to carry higher current as compared to the other (sub)units depending on the fault identification time and the grid topology. The number of IGBTs are compared in Table III. Fig. 14(b) depicts the total number of IGBTs in MB (sub)units versus the number of adjacent lines. Fig. 14(b) shows that the Mp-HCB requires significantly fewer IGBTs, especially when the number of adjacent lines increases.

C. Surge arresters

1) Overvoltage protection level: The overvoltage protection voltage for the surge arrester of the HCB would lie in range of $1.4V_{dc}-1.5V_{dc}$ [12], [18]. The overvoltage protection level of the surge arresters of Mp-HCB are also assumed to lie in the same range.

2) Discharge current: (12) illustrates that the maximum discharge current in the surge arresters of the Mp-HCB in line fault scenario is smaller than the value of fault current

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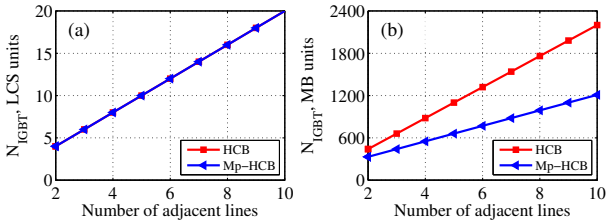

Fig. 14. Number of IGBTs versus the number of adjacent lines (a) MB (b) LCS

TABLE III
MP-HCB AND HCB PARAMETERS COMPARISON

dc bus protection requirement with $n-1$ adjacent line			
Parameter	**Asymmetric Monopole**	**Symmetric Monopole**	**Bipole**
Mp-HCB	1	2	2
HCB	$n-1$	$2(n-1)$	$2(n-1)$
Internal parameters comparison (For dc bus with $n-1$ adjacent line)			
Parameter	**HCB**	**Mp-HCB**	
Number of UFDs	$n-1$	$n-1$	
Number of limiting ind.	$n-1$	$n-1$	
Number of surge arresters	$n-1$	n	
Surge arresters energy	E	$\frac{E}{n}$	
Surge arresters voltage	V_{ovp}	V_{ovp}	
Number of IGBTs in LCS	$2(n-1)$	$2(n-1)$	
Number of IGBTs in MB	$\frac{2(n-1)V_{ovp}}{V_{CES}}$	$\frac{nV_{ovp}}{V_{CES}}$	

at the interruption instance by a factor of $n-1$. However, the maximum discharge current in the surge arrester in typical HCB is almost equal to the interrupted current.

3) Energy:

a) Transmission line Fault: In HCB based protection and during the line fault, only the faulty line DCCB interrupts the current and its surge arrester absorbs the energy. When using the Mp-HCB the faulted line corresponding surge arrester does not absorb the energy and the energy absorption is shared between $n-1$ surge arresters. Using (14) and (24) the ratio of absorbed energy in both DCCBs can be given as:

$$\frac{E_{SA}^{Mp-HCB}}{E_{SA}^{HCB}} = \frac{1}{n-1}, \tag{28}$$

where E_{SA}^{Mp-HCB} and E_{SA}^{HCB} represents the absorbed energy in a single surge arrester of Mp-HCB and the HCB, respectively. (28) implies that the energy rating of surge arresters in Mp-HCB is at least 50% smaller than that of HCB.

b) dc bus Fault: Equal amount of energy is absorbed in the surge arresters of both devices in dc bus fault interruption.

D. Ultra-fast disconnector

The Mp-HCB requires $n-1$ UFDs, which is equal to the number of UFDs in HCB based scheme.

E. Current limiting inductors

The number of current limiting inductors and their inductance in both schemes are identical.

F. Multiple fault handling

The average failure rate for all types of submarine power cables are 0.1114 faults/100 km/year [29] and it has been reducing since most new cables being buried to a depth of at least 0.5 m and have better route design. Considering that the future MT-HVDC grid is expected to connect large wind farms and the cables will not be buried physically close together, the probability of faults in different cables are independent. Therefore, using the fault occurrence probability in a single cable the multiple fault probability can be obtained by multiplication of single fault probabilities. For instance, the average failure rate for 2 cables at the same time for all types of submarine power cables can be obtained as 0.0124 faults/100 km/year. This means the average time for having faults on two cables simultaneously in 100 km is almost 80 years. This time range is even longer than the lifetime of the offshore systems. Therefore, due to the proposed application for Mp-HCB, the multiple fault occurrence has not been considered in design of Mp-HCB. However, in case that the proposed Mp-HCB is needed to be designed for systems with considerable multiple faults occurrence probability, the MB subunits may be required to be rated for higher currents depending on the number of ports (adjacent lines). The worst case happens when the system has two adjacent lines (3-port Mp-HCB). In this case, when two faults simultaneously happen, MB_n is required to carry sum of the fault currents. However, when the system has larger number of adjacent lines, when two faults happen, MB_n will carry only a portion of sum of fault currents as other healthy MB subunits will also carry some portion of sum of the fault currents. For instance, assume a system with 5 adjacent lines (6-port Mp-HCB). If two faults happen on adjacent lines connected to ports 1 and 2, the sum of fault currents will be shared between MB_3, MB_4, MB_5 and MB_6. Therefore, an increase in the rating of MB subunits is expected. Note that the requirement for increase in the ratings of MB subunits will be decreased as the number of adjacent lines are increased. Moreover, when Mp-HCB is interrupting a fault current ($t_{ax} < t < t_{br}$), if it receives another trip command (due to another fault occurrence), it should restart the interruption process from $t = t_{ax}$ and open the required DS before opening MB units. This can lead to a delay in current interruption and consequently higher magnitude of fault current as it will be growing during the mentioned delay time, which can reach to 2.25 ms in the worst case.

VI. CONCLUSION

In this paper, a novel multi-port dc circuit breaker has been proposed and analyzed. Each port of Mp-HCB interrupts the current, independent of the other ports. The proposed device has a similar time performance compared to the HCB. The analysis implies that the proposed Mp-HCB requires fewer IGBTs compared to the typical HCB. For a dc bus with two adjacent transmission lines, Mp-HCB needs 25% fewer IGBTs in its MB unit as compared to the HCB. As the number of adjacent lines increases the percentage of saved IGBTs approaches 50%. Moreover, the proposed device requires smaller size surge arresters due to the less discharge current and energy absorption in its surge arresters as compared to the HCB. The results from this study confirms that the energy ratings of the surge arresters can be reduced by almost 50%. Considering the improvements by applying the proposed device, its implementation cost is expected to be remarkably lower than the cost of typical HCBs. Although the Mp-HCB is proposed for cable based offshore MT-HVDC grid applications, it can also be designed for over-head line based MT-HVDC grid applications by considering the possibility of multiple

faults occurrence. In this case, depending on the number of Mp-HCB ports, the MB and LCS subunits may be required to be rated for larger currents. The future work will concern with the cost-benefit and reliability studies of the proposed device.

APPENDIX

TABLE IV
THREE-TERMINAL HVDC SYSTEM PARAMETERS

Converter terminal parameters			
Parameter	**VSC 1**	**VSC 2**	**VSC 3**
Rated power [MVA]	300	150	150
dc bus capacitor [μF]	1000	1000	1000
dc bus voltage [kV]	320	320	320
Bus filter reactor [mH]	10	10	10
Cable parameters			
Parameter	**Line 32**	**Line 13**	
Length [km]	200	150	
Resistance [Ω/km]	0.001	0.001	
Inductance [mH/km]	2	2	

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