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INVITED REVIEW

N-polar GaN epitaxy and high electron mobility transistors

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Abstract

This paper reviews the progress of N-polar $(000\bar{1})$ GaN high frequency electronics that aims at addressing the device scaling challenges faced by GaN high electron mobility transistors (HEMTs) for radio-frequency and mixed-signal applications. Device quality (Al, In, Ga)N materials for N-polar heterostructures are developed using molecular beam epitaxy and metalorganic chemical vapor deposition. The principles of polarization engineering for designing N-polar HEMT structures will be outlined. The performance, scaling behavior and challenges of microwave power devices as well as highly-scaled depletion- and enhancement-mode devices employing advanced technologies including self-aligned processes, $n+$ (In,Ga)N ohmic contact regrowth and high aspect ratio T-gates will be discussed. Recent research results on integrating N-polar GaN with Si for prospective novel applications will also be summarized.

(Some figures may appear in colour only in the online journal)

1. Introduction

The combination of high electron velocity, large breakdown field and high 2-D electron gas (2DEG) density of the III-nitride material system has enabled devices possessing wide bandwidth and high breakdown voltage simultaneously [1]. GaN high electron mobility transistors (HEMTs) have demonstrated high frequency power amplification from the S-band to the W-band with high power-added efficiencies (PAE) and significantly higher output power densities than currently available from amplifiers based on other material systems such as GaAs or InP [2–8]. The highest reported RF power densities of GaN HEMTs to date are 41.4 W mm^{-1} at 4 GHz [4], 30.6 W mm^{-1} at 8 GHz [2], 13.7 W mm^{-1} at 30 GHz [5] and 10.5 W mm^{-1} at 40 GHz [3]. W-band power amplifier monolithic millimeter-wave integrated circuits (MMICs) have delivered 1.7 W of output power at 91 GHz [8]. The high drain current density (I_{DS}) and high-speed performance of GaN HEMTs also render these devices suitable for integrated digital or control functions. Monolithic integration of highly-scaled enhancement- and depletion-mode (E/D) GaN HEMTs with an unprecedented combination of high-frequency and high-breakdown characteristics offer the feasibility of high-density GaN-based mixed-signal circuits [9–15].

For both radio-frequency (RF) and mixed-signal applications, the unity short-circuit current-gain cutoff

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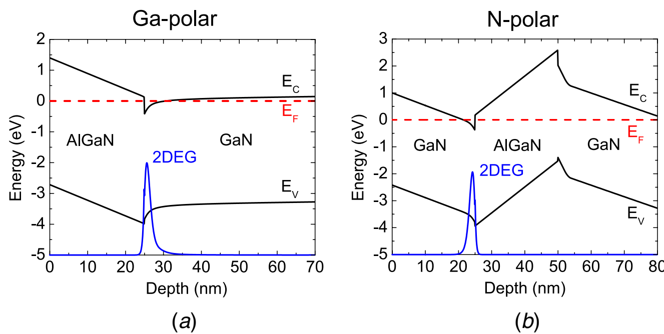


Figure 1. Equilibrium band diagrams of generic Ga-polar (0 0 0 1) (left) and N-polar (000 $\bar{1}$) (right) heterostructures.

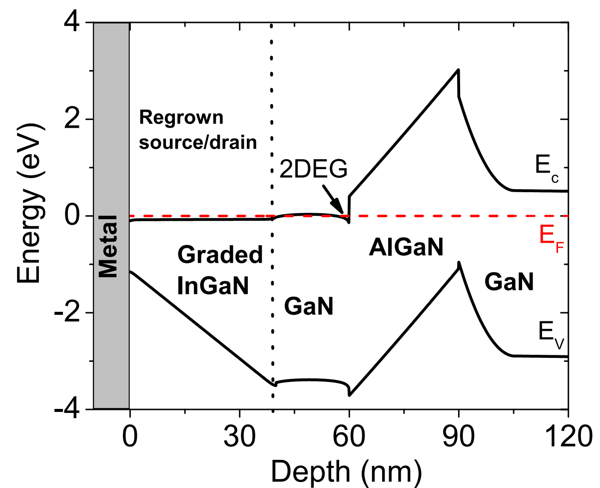


Figure 2. An equilibrium band diagram along the access region of an N-polar HEMT structure with a regrown graded-InGaN contact layer. Reprinted with permission from [57]. Copyright 2010, American Institute of Physics.

frequency (f_T) and maximum oscillation frequency ($f_{\max}$) of a transistor are key high frequency figures of merit. Devices with high gain are desirable for reducing circuit size and complexity that will lead to higher efficiency. Improvements in f_T and $f_{\max}$ of GaN HEMTs have been achieved primarily through the scaling of device dimensions. There have been numerous reports of GaN HEMTs with record f_T and $f_{\max}$ values achieved through novel technologies and heterostructures including AlGaN or InGaN back-barriers to reduce short-channel effects, regrown $n+$ ohmic contacts to minimize contact resistances, thin Al(In)N charge-inducing barriers with strong polarizations for high transconductance (g_m) and low access resistances, and gate recesses to enhance gate control [16–50]. To more effectively address these scaling challenges of GaN transistors for millimeter- and sub-millimeter-wave frequencies, a disruptive device technology based on the N-polar (000 $\bar{1}$) orientation of GaN has been intensively studied in recent years. This paper reviews the research in high frequency N-polar GaN HEMTs and the epitaxial processes that have enabled these technologies.

2. Design principles and polarization engineering of N-polar GaN HEMTs

Due to the absence of inversion symmetry in wurtzite III-nitride materials, the polarization of N-polar crystals is opposite to that of the Ga-polar (0 0 0 1) crystals. Therefore, the polarization-induced electric fields in N-polar heterostructures are opposite to those of the Ga-polar counterpart, inducing a 2DEG above instead of below the wide-bandgap barrier layer (figure 1). N-polar GaN HEMTs, with a generic structure consisting of GaN-channel/Al(Ga)N-barrier/GaN-buffer, are envisioned to offer device scaling advantages over the existing Ga-polar technology in the following areas:

(i) *Strong back-barrier:* N-polar heterostructures possess an inherent wide-bandgap Al(Ga)N back-barrier for electron confinement to reduce short-channel effects [51]. As a negative gate bias is applied to turn off the device, the 2DEG charge is depleted and the wavefunction is delocalized away from the gate in a Ga-polar device but is confined by the back-barrier and localized at the GaN/Al(Ga)N heterointerface in an N-polar structure. This improved electron confinement in an N-polar HEMT results in better off-state pinch-off characteristics as well as reduced on-state output conductance. Simulation studies performed by Park *et al* [52] and Guerra *et al* [53] supported these predictions.

(ii) *Low-resistivity Ohmic contact*: The 2DEG in N-polar HEMTs can be contacted through the channel layer that has a narrower bandgap and lower surface barrier to electrons, rather than through the wide-bandgap Al(Ga)N barrier that acts as a bottleneck to obtaining a low contact resistance in Ga-polar HEMTs [54, 55]. This results in the possibility for a lower contact resistance in the N-polar structure using selective-area ohmic regrowth. Taking advantage of the surface electron accumulation in InN [56] to achieve a metal-InN contact resistance as low as 5 Ω-μm, and eliminating the large conduction band offset between GaN and InN using a compositionally graded $In_xGa_{1-x}N$ layer (figure 2), the ohmic contact resistance of ~25 Ω-μm (0.025 Ω-mm) between the metal and the 2DEG thus obtained has remained the lowest in GaN HEMTs [57].

(iii) *Improved scalability:* Maintaining a high aspect ratio while scaling to short gate lengths requires a proportionate scaling of the gate–channel separation. By forming the 2DEG between the gate metal and the GaN/Al(Ga)N heterointerface, the quantum displacement of the 2DEG in an N-polar HEMT reduces the effective gate–channel distance. This effect is opposite to that in Ga-polar HEMTs where the effective gate–channel capacitance is reduced by the quantum capacitance [58]. Such enhancement of the gate–source capacitance over the geometric capacitance in N-polar HEMTs and consequently a higher transconductance compared to Ga-polar structures with the same physical gate–channel thickness is expected to be of significant benefit to scaling when the wavefunction displacement is of comparable magnitude to the physical gate–channel spacing.

Associated with scaled gate–channel distances is enhanced 2DEG charge depletion under the gate due to

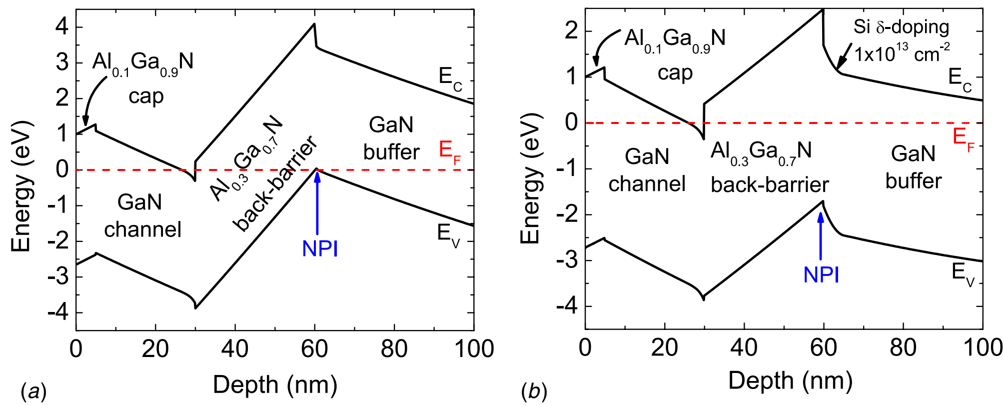


Figure 3. Equilibrium band diagrams of (*a*) an undoped and (*b*) a Si δ-doped N-polar GaN HEMT. The negatively polarized interface (NPI), where an interfacial hole trap of interest is located, is indicated in each structure. Copyright 2012 IEEE. Reprinted, with permission, from [62].

surface pinning [59]. Since the aspect ratio in Ga-polar HEMTs is determined by the barrier thickness, a tradeoff exists between the barrier thickness and the charge density under the gate. In N-polar HEMTs, on the other hand, the aspect ratio and the charge density under the gate can be independently controlled such that the enhanced charge depletion due to scaled channel thicknesses can be compensated by increasing the polarization or thickness of the charge-inducing back-barrier. InAlN back-barriers lattice-matched to GaN overcome the constraint in barrier thickness due to strain relaxation while simultaneously offering strong polarization [60].

The formation of a 2DEG in an N-polar heterostructure is possible without intentional n-type doping [55, 61, 62], suggesting the presence of a high density of unintentional donors in the system that cannot be accounted for by surface states (since positive surface donors cannot compensate the positive polarization charge on an N-polar surface) or unintentional bulk donors (due to their low densities for well-optimized growths) [63]. For a nominally undoped N-polar GaN/Al$_x$Ga$_{1-x}$N/GaN heterostructure with $x = 0.3$, where the equilibrium Fermi level (E_F) is in close proximity to the valence band (E_V) at the negatively polarized AlGaN-barrier/GaN-buffer interface, a hole trap state (E_T) is measured by deep level transient spectroscopy (DLTS) to be at 60 meV from the E_V at the negatively polarized Al$_x$Ga$_{1-x}$N/GaN interface (figure 3) [64]. The hole trap state is considered donor-like due to its charge compensating effect at the negative interface in the sense that it is positive when empty and neutral when occupied. The trap screens the net fixed polarization charge at the negative interface when ionized without a hole gas forming and transfers electrons to the 2DEG channel [51, 65].

The role of the hole trap state as a native source of electrons in N-polar heterostructures results in two undesirable device characteristics. During large-signal high-frequency operation, modulating the charge occupancy of the hole traps located under the gate by V_{GS} leads to large-signal dc-RF dispersion [51]. Under dc operation at a given fixed gate potential, ionization of the hole traps located on the drain side of the gate by increasing V_{DS} beyond the saturation voltage ($V_{DS,sat}$) causes dc output conductance albeit without apparent output resistance degradation under RF conditions (figure 4) [62]. The dc-RF dispersion and dc output conductance in N-polar GaN HEMTs can be eliminated by grading the AlGaN-back-barrier/GaN buffer interface, where ionized Si donors are used to maintain an equilibrium E_F above mid-gap throughout the grade by compensating the negative

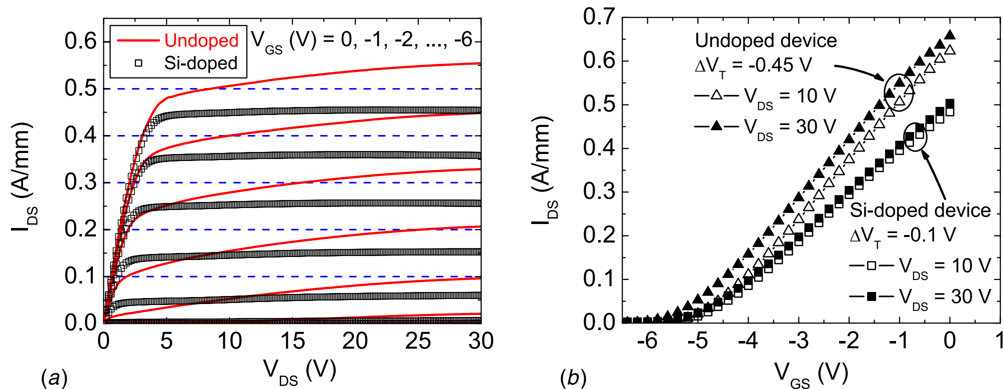


Figure 4. (*a*) DC output characteristics of the undoped (red line) and Si-doped (black square) N-polar GaN HEMTs depicted in figure 3 showing a higher output resistance with Si doping. (*b*) Transfer characteristics of the undoped and Si-doped N-polar GaN HEMTs showing a much smaller V_T shift with Si doping. Copyright 2012 IEEE. Reprinted, with permission, from [62].

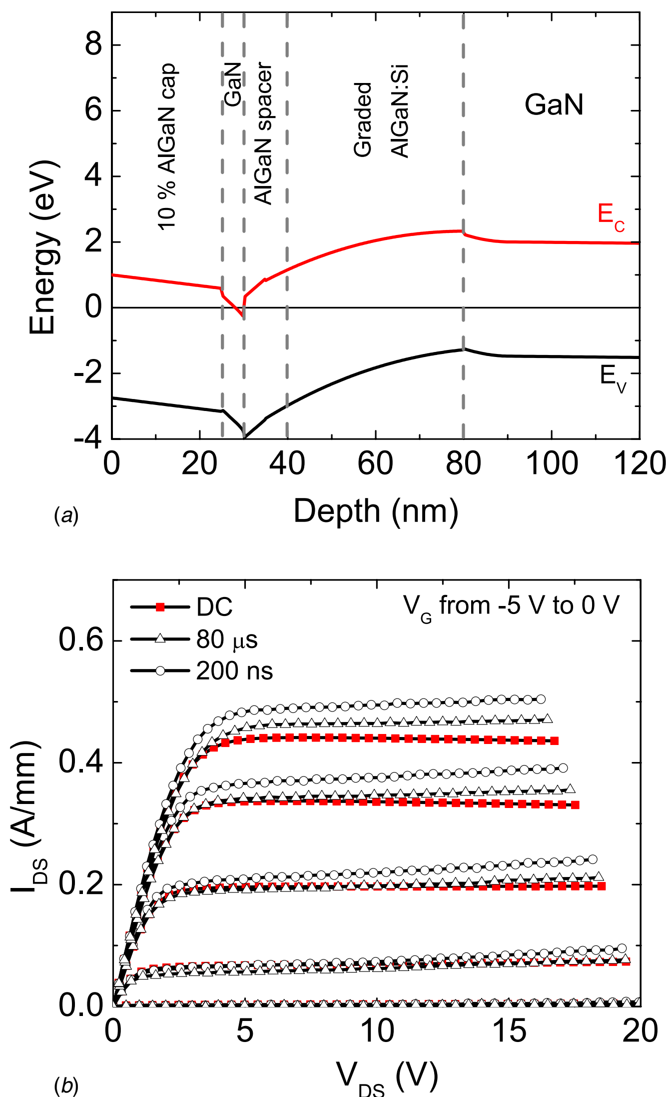


Figure 5. (*a*) An equilibrium band diagram of an N-polar HEMT with a graded-AlGaN back-barrier. (*b*) Pulsed and dc *I*–*V* characteristics of the device depicted in (*a*) with no dc-RF dispersion observed under pulsed conditions. Reprinted with permission from [51]. Copyright 2007, American Institute of Physics.

space charge (ρ) induced by the gradient in polarization ($\overline{P}$) according to the relationship $\rho = -\nabla \cdot \overline{P}$ [51] (figure 5). Alternatively, Si δ-doping can be inserted at or below the negatively polarized interface to separate the trap level from the E_F, thereby preventing the change in the occupancy and hence the charge state of the traps [62] (figure 3). The graded structure could be viewed as a variation of the Si δ-doped structure by spreading the negative polarization sheet charge at the AlGaN-back-barrier/GaN-buffer interface into a 3-D space charge as well as distributing the δ dopant sheet as bulk doping throughout the graded-AlGaN layer. In both cases, the ionized Si donors supply electrons to the 2DEG channel and provide the compensating positive charges for the negatively polarized interface.

To reduce gate leakage current due to the low Schottky barrier height on GaN, N-polar HEMT structures are often capped with Al(Ga)N or InAlN to take advantage of their polarization-induced electric field that opposes gate current flow and their wider bandgap to reduce tunneling. In addition, a dielectric (typically SiN_x deposited by high-temperature chemical vapor deposition (HT-CVD) [66, 67]) is commonly deposited on N-polar epilayers to protect the relatively reactive N-polar surface during device processing steps that do not normally affect the stable Ga-polar surface. The dielectric layer also serves as a gate insulator that reduces leakage and increases gate voltage swing.

3. Epitaxy of N-polar GaN

3.1. Polarity selection

Growth of polar wurtzite GaN for high frequency electronics has often required foreign substrates with only a limited number of reports of device fabrication on native GaN substrates [68–70] because low-cost large-area semi-insulating GaN substrates have been unavailable. Since the properties of *c*-plane GaN depend on the polarity [71], a number of *in situ* and *ex situ* techniques have been developed to identify the crystal orientation and the presence of inversion domains. N-polar GaN is readily etched in aqueous potassium hydroxide solutions [72, 73] and atomic hydrogen [74] whereas Ga-polar GaN is inert toward these etchants. The lack of inversion symmetry between N-polar and Ga-polar GaN manifests as reversed convergent beam electron diffraction (CBED) patterns. Moreover, N-polar GaN shows distinct surface kinetics from Ga-polar GaN that can be monitored by reflection high energy electron diffraction (RHEED) during MBE growth (section 3.2).

A common substrate for GaN heteroepitaxy is (0 0 0 1) *c*-plane sapphire (Al_2O_3) due to its relatively low cost despite its poor thermal conductivity as well as chemical dissimilarity and large lattice mismatch to GaN. Understanding and controlling the polarity of GaN on sapphire substrates using different growth techniques has therefore been an important research topic [75]. The mechanism of polarity control has been attributed to the chemical termination of the sapphire surface or growth initiation conditions such as pre-growth sapphire nitridation and the use of low-temperature (LT) buffer layers [76, 77]. While nitridation of sapphire using NH_3 leads to the formation of a thin AlN surface layer that is suggested to be N-polar [78, 79], it was found that the growth conditions of the LT GaN or AlN buffer layers play an equally important role in polarity control. Sumiya *et al* and Rouvière *et al* have conducted systematic studies into the role of growth initiation procedures in determining the properties of GaN grown by metalorganic chemical vapor deposition (MOCVD) [80–82], and proposed that crystal polarity could explain the different properties of GaN reported by various groups [83–85]. Similar studies were carried out by Wu *et al* on the MOCVD growth of AlN films with consistent results [86]. With plasma-assisted molecular beam epitaxy (PAMBE), direct growth of a GaN buffer on basal plane sapphire usually results in N-polarity, whereas an AlN buffer layer converts the film to Ga-polarity [87–90]. However, it has also been reported that the sapphire nitridation temperature as well as the growth conditions of the

GaN or AlN buffer layers would influence the polarity of the epilayers [74, 91]. The reported N-polar devices on sapphire by MBE have used GaN buffers grown directly on the substrate [90], but these epilayers suffer from residual inversion domains and poor morphology that degrade transport properties and device performance.

SiC is another preferred substrate for GaN high frequency, high power electronics due to its smaller in-plane lattice mismatch (3.4%) to GaN and higher thermal conductivity than sapphire. Different groups have studied the growth of GaN on the basal planes (Si-face and C-face) of SiC [92–96]. While polarity selection on non-polar sapphire substrates depends on the growth initiation conditions, the polarity of GaN films grown on the basal planes of SiC is unambiguously determined by the choice of substrate polarity where the Ga-polarity and N-polarity of GaN nucleate on the Si-face and C-face of SiC, respectively.

The polarity of GaN can be converted from Ga-face to N-face or vice versa. The ability to manipulate polarity on a GaN platform may be desirable for fabricating novel heterostructures. Historically, the problem of polarity inversion from Ga-face to N-face has received much attention due to the formation of inversion domains in highly Mg-doped Ga-polar GaN [97, 98]. However, doping N-polar GaN with Mg beyond low 10^{18} cm^{-3} results in the formation of a cubic polytype instead of polarity inversion [99]. No polarity inversion can be observed in N-polar GaN even with very high bulk Mg doping. Controllable polarity inversion of GaN from N-face to Ga-face has instead been achieved using Mg_xN_y interlayers [100, 101], AlO_x interlayers [102, 103], or monolayers of Al metal at the inversion interface [104].

3.2. Plasma-assisted molecular beam epitaxy

The PAMBE growth processes of Ga- and N-polar GaN share similar conditions. This is likely related to the existence of a metallic Ga surface adlayer in the MBE process when conducted under metal-rich conditions. The Ga adlayer consists of a laterally contracted bilayer in the case of Ga-polar GaN and one monolayer in the case of N-polar GaN [96, 105–107]. Since Ga is present on the surface as a surfactant for adatom diffusion in both cases, no major change in the Ga-polar growth process is required to obtain smooth N-polar films.

The structural, morphological and electrical qualities of PAMBE N-polar GaN grown on C-face SiC for HEMTs are optimized based on the best-known growth methods of PAMBE Ga-polar GaN on Si-face SiC [108, 109]. AlN grown in the N-rich regime (flux ratio $f_{Al}/f_N < 1$) is used as the nucleation layer to suppress unintentional Si and C impurity incorporation [109–111], promote 2D GaN growth by improving surface wetting [112] and reduce lattice mismatch to GaN [112]. Serving as a crystallographic template for the subsequent GaN growth, the nucleation layer has a profound effect on the mosaic structure and electrical properties of subsequent epilayers. A two-step GaN buffer scheme is employed to realize threading dislocation (TD) densities and morphologies comparable to state-of-the-art Ga-polar films

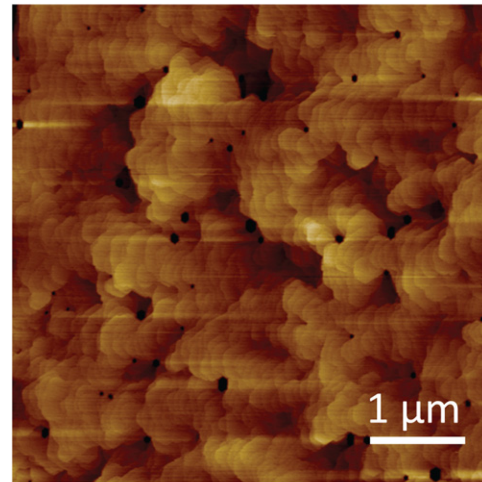


Figure 6. A 5 μm × 5 μm atomic force microscope (AFM) image of PAMBE-grown N-polar GaN showing an rms roughness of ∼1 nm. The height scale is 10 nm.

[113–116]. The scheme consists of a rough pitted GaN buffer layer (‘step-one’ GaN) grown in the Ga-rich intermediate regime (flux ratio $f_{Ga}/f_N > 1$) to increase the probabilities for dislocation fusion or annihilation, followed by a smooth GaN buffer layer grown in the Ga-rich droplet regime ($f_{Ga}/f_N \gg 1$). The N-face polarity of these films can be confirmed by observation of 3 × 3 and 6 × 6 RHEED surface reconstructions [117, 118]. The resulting N-polar GaN exhibits step-flow morphology with root-mean-square (rms) roughness of ∼1 nm (figure 6). The TD density, being dominated by edge-component TDs [119, 120], is about 1.5 × 10^{10} cm^{-2} for 0.5-μm thick films. As-grown unintentionally doped N-polar GaN is highly resistive despite its elevated oxygen levels compared to Ga-polar GaN grown in the same reactor by about one order of magnitude [121, 122], which is likely due to background carrier trapping by TDs [123]. N-polar GaN/AlGaN HEMTs grown using the aforementioned process demonstrate 2DEG densities exceeding 1 × 10^{13} cm^{-2} and room temperature Hall mobilities as high as 1700 cm^2 V^{-1} s^{-1} [51, 61, 124].

Point defect incorporation in PAMBE-grown GaN is sensitive to the crystal polarity. A combination of DLTS and deep-level optical spectroscopy (DLOS) measurements on N-polar and Ga-polar *n*-type GaN grown by PAMBE reveals very similar total deep level concentrations, but with a significant redistribution of dominant trap states in the GaN bandgap. In particular, N-polar GaN incorporates both residual, extrinsic carbon impurities and intrinsic nitrogen-related defects differently than Ga-polar GaN [125]. The different distribution of trap states may become important for understanding any difference in the behavior and reliability between N-polar and Ga-polar devices [126].

The N-polar surface exhibits enhanced indium incorporation compared to the metal-polar surface under similar PAMBE growth conditions. While In impinging on the terrace of metal-polar films only interact weakly with the In and Ga surface atoms, stronger In-N bonds form on N-polar surfaces that increase the sticking probability of In. It has been shown that N-polar InN can be grown at 100 °C above

the thermal dissociation limit of In-polar InN [127–130]. The indium incorporation efficiency in N-polar InGaN was found to be higher than in metal-polar InGaN at a given growth temperature [131]. Higher optical qualities are achieved for N-polar InGaN as a result of the higher growth temperatures [132]. The optimal growth of N-polar InAlN lattice-matched to GaN, developed for strain-free back-barriers in HEMT structures [133], is also carried out at 70 °C higher than for metal-polar InAlN [134].

3.3. Metalorganic chemical vapor deposition

Smooth PAMBE-grown N-polar GaN films are obtained on C-face SiC using knowledge from Ga-polar GaN MBE without drastic changes to the growth process. On the contrary, N-polar GaN grown by MOCVD typically exhibits hexagonal hillocks on the film surface, independent of whether the films are deposited on C-face SiC [135] or nitrided sapphire [80]. This is attributed to the absence of a metallic Ga adlayer on GaN to facilitate adatom diffusion during MOCVD growth. Under typical MOCVD growth conditions, the growth rate is limited by the transport of Ga-species to step and kink positions on the crystal surface. When Ga-species impinges on a Ga-polar surface, the relatively week $Ga_{surface}$–Ga bonds allow for easy desorption and movement to the step and kink positions that result in step-flow growth. In contrast, fairly strong $N_{surface}$–Ga bonds form when the Ga impinges on an N-polar surface, resulting in a higher activation energy for desorption that hampers diffusion to the step and kink sites and increases the probability of nucleation on the terraces. The adatom diffusion on (0 0 0 1) and (000 $\bar{1}$) GaN surfaces is discussed in detail in [136].

The problems related to the low surface mobility on N-polar surfaces in the MOCVD process are mitigated through growth on misoriented substrates. A misorientation angle of 2°, combined with modified nucleation and growth processes to ease the transport of Ga-species to step and kink sites on the surface, successfully suppress the formation of the hexagonal surface features (figure 7). In addition to the sapphire nitridation step to achieve N-polarity [71, 75], both the nucleation layer and the initial high temperature GaN layer are deposited at higher temperatures compared to the typical Ga-polar GaN growth process [137]. Moreover, low ammonia flows are beneficial for the growth of smooth N-polar GaN films by MOCVD. The N-polar growth process was found to be even more robust when using higher misorientation angles such as 3° or 4°. A significant reduction of the threading dislocation density is observed with increasing misorientation angles. The full-width at half-maximum (FWHM) values of the (000 $\bar{2}$) and (20 $\bar{2}$ $\bar{1}$) x-ray rocking curves for 0.8-μm thick GaN films are 300 arcsec and 510 arcsec, respectively, corresponding to a threading dislocation density in the high 10^8 cm^{-2} that is comparable to the quality of Ga-polar films of a similar thickness (figure 8). It was determined that misorientation toward the sapphire *a*-plane (resulting in GaN misoriented toward the *m*-plane [138]) led to a more regular surface morphology with steps parallel to the ⟨11 $\bar{2}$ 0⟩ direction. The growth process on sapphire is discussed in detail in [137]. Improvements in the quality of N-polar GaN grown on sapphire due to substrate misorientation were also reported by Sun *et al* [139, 140]. To render the N-polar GaN base layers insulating for transistor applications, Fe doping similar to the

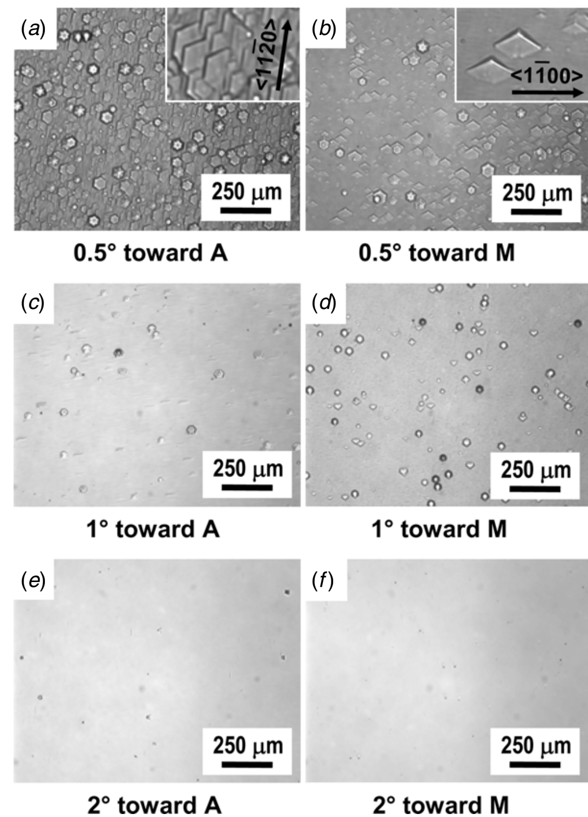


Figure 7. Optical micrographs of 0.8 μm thick GaN films grown on (0 0 0 1) sapphire substrates with misorientation angles of (*a*) 0.5°, (*c*) 1° and (*e*) 2° toward the *a* plane, and (*b*) 0.5°, (*d*) 1° and (*f*) 2° toward the *m* plane. The inserts in (*a*) and (*b*) are enlarged threefold. Reprinted with permission from [137]. Copyright 2007, American Institute of Physics.

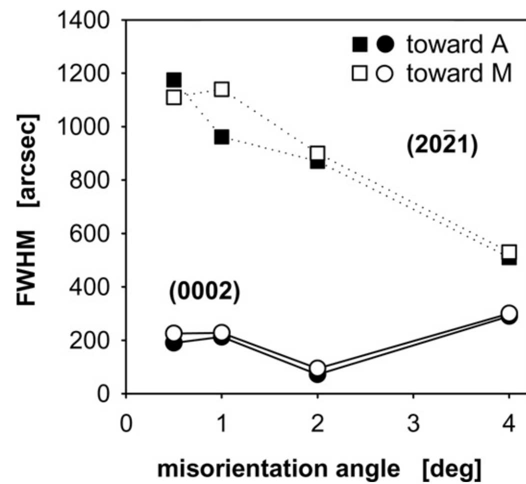


Figure 8. FWHM of the x-ray rocking curves measured for the (000 $\bar{2}$) and (20 $\bar{2}$ $\bar{1}$) diffraction peaks of 0.8 μm thick GaN films grown on (0 0 0 1) sapphire substrates with different misorientation angles and directions. Reprinted with permission from [137]. Copyright 2007, American Institute of Physics.

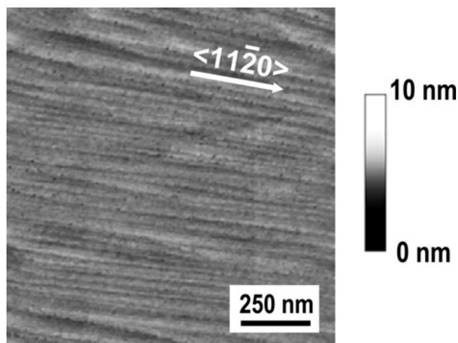


Figure 9. AFM image of a 26 nm thick $Al_{0.32}Ga_{0.68}N$ grown on a 1.5 μm semi-insulating GaN buffer by MOCVD. Reprinted with permission from [146]. Copyright 2008, American Institute of Physics.

growth of semi-insulating Ga-polar GaN films is implemented [141]. At the same time, high system purity has to be ensured to minimize the residual oxygen impurity concentration in the N-polar films, as the incorporation efficiency of residual oxygen impurities into N-polar films is significantly higher than in Ga-polar layers [121, 122, 142].

Similar to the results on sapphire substrates, smooth N-polar (Al,Ga,In)N films are obtained on C-face SiC substrates misoriented 4° toward the *m*-plane leading to (Al,Ga,In)N misoriented toward the *m*-plane. As in the growth of Ga-polar GaN films on Si-face SiC, the growth is initiated with the deposition of a thin AlN layer at a high temperature. But contrary to the Ga-polar process, a GaN layer grown at a medium temperature is inserted before the deposition of the main GaN layer at a high temperature. The addition of the medium temperature layer prevents the formation of macro-steps on the GaN surface to enable high-quality GaN/AlGaN heterostructures [143, 144]. The structural property of the GaN buffer is further improved by replacing the medium-temperature GaN layer with an AlGaN layer [145].

In N-polar GaN/AlGaN heterostructures grown on misoriented substrates, the surface steps at the GaN/AlGaN heterointerface lead to anisotropy in the 2DEG transport with lower sheet resistances for transport parallel to the steps (figure 9) [146–148]. The sheet resistance parallel to the surface steps is largely unaffected by the misorientation angle with room temperature electron mobilities as high as 1800 cm^2 V^{-1} s^{-1}, whereas the sheet resistance increases with increasing misorientation for transport perpendicular to the steps (figure 10) [149]. The energy band landscape of the surface steps creates high-density arrays of self-patterned lateral quasi-one-dimensional channels with electrostatic confinement, as a result of which significant anisotropy is also observed in the conductive charge density parallel and perpendicular to the steps [150]. The dimensionality of the electron gas in these vicinal GaN/AlGaN heterostructures can be tuned electrostatically to obtain room-temperature pure 1D transport (parallel to the atomic terraces) at technologically relevant current densities without having to lithographically synthesize nanowire structures [151].

MOCVD growth processes are also developed for high quality N-polar InGaN and InAlN for optical emitters,

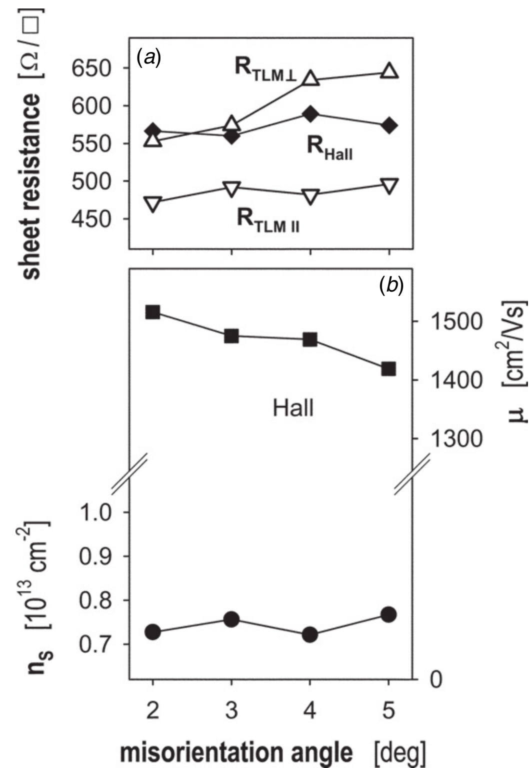


Figure 10. (*a*) Dependence of room temperature 2DEG sheet resistance on Si doping in an N-polar GaN/$Al_{0.28}Ga_{0.72}N$ heterostructure measured using transfer length method (TLM) patterns parallel (downward triangle) and perpendicular (upward triangle) to the step direction and derived from Van der Pauw Hall measurements (diamond). (*b*) Dependence of the 2DEG concentration (circle) and the electron mobility (square) on Si doping determined by room temperature Van der Pauw Hall measurements in an N-polar GaN/$Al_{0.28}Ga_{0.72}N$ heterostructure. Reprinted with permission from [149]. Copyright 2008, American Institute of Physics.

photovoltaics and transistors [152–154]. While N-polar InGaN incorporates more indium compared to metal-polar InGaN deposited at the same temperature as is the case with PAMBE [152], the indium content in InAlN is comparable for both crystal orientations under the same growth conditions [153].

4. Scattering of 2DEG in N-polar heterostructures

The 2DEG mobility in N-polar HEMTs is observed to decrease with an increasing reverse gate bias [155]. Unlike in Ga-polar AlGaN/GaN HEMTs where the 2DEG is less confined in the triangular quantum well with an increasing reverse gate bias, the electrons in N-polar HEMTs experience a stronger vertical confinement field at the GaN/AlGaN interface near device pinchoff. Alloy scattering and ionized impurity scattering become dominant with the increasing electric field in the channel due to increased penetration of the wavefunction into the AlGaN barrier and reduced screening of the background donors in the barrier, respectively [155]. Alloy scattering can be mitigated by inserting an AlN interlayer with a large conduction band offset at the GaN/AlN 2DEG interface to rapidly quench the wavefunction penetration into the AlGaN barrier [156].

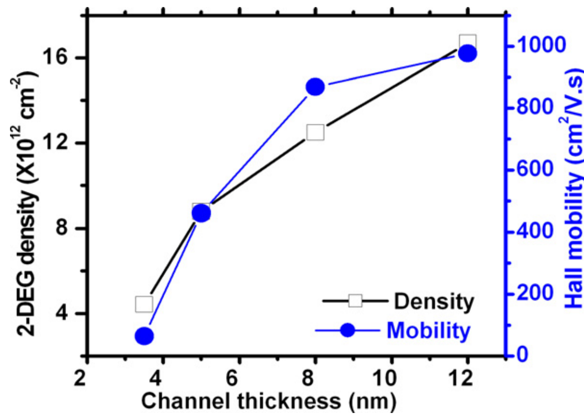


Figure 11. Measured room temperature Hall mobility and 2DEG density as a function of GaN channel thickness. Reprinted with permission from [158]. Copyright 2012, American Institute of Physics.

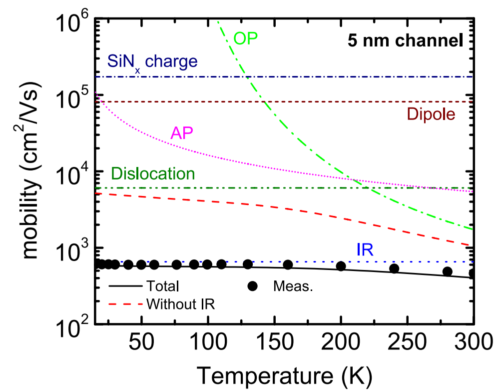


Figure 12. Calculated and measured temperature-dependent electron mobility for a 5 nm GaN channel device taking into account scattering due to interface roughness, charged dislocations, optical phonons (OP), acoustic phonons (AP), random fluctuations of dipole moments and trapped charges in the SiN_x insulator. Reprinted with permission from [158]. Copyright 2012, American Institute of Physics.

Mobility degradation is also observed with an increasing forward gate bias or at higher 2DEG charge densities in metal-oxide-semiconductor (MOS) or metal-insulator-semiconductor (MIS) HEMTs, in which case the electrons become less confined with their wavefunction spreading toward the dielectric/GaN interface leading to increased surface scattering [157]. This drop in mobility under forward gate bias was suggested to be the cause of transconductance collapse in self-aligned HEMT structures [157], which may also impact the drive current in E-mode devices. Inserting a thin AlN spacer between the dielectric and the GaN channel would suppress scattering from the disordered interface. Charge depletion due to the AlN can be compensated by increasing the polarization or thickness of the charge-inducing back-barrier.

As the GaN channel thickness is scaled to maintain electrostatic integrity in short-gate devices, thin channels were found to be detrimental to electron mobility and velocity (figure 11) [158, 159]. By analyzing the N-polar GaN channel as a double-heterostructure quantum well and eliminating alloy scattering using an AlN interlayer at the 2DEG interface, experimental and theoretical investigations were conducted on MBE-grown heterostructures that identified interface roughness scattering as the principal factor in degrading the low field electron mobility for thinner GaN channels [158] (figure 12). There are three contributing components to roughness scattering:

(i) The quantum well thickness fluctuation height and correlation length parameters extracted for N-polar HEMTs are larger than those typical for Ga-polar HEMTs [160] due to the inverted nature of the N-polar HEMT structure, where the GaN channel layer is grown on AlGaN, coupled with the high Si doping. Similar degradation in electron mobility has also been observed in inverted modulation-doped AlGaAs/GaAs heterostructures [161, 162].

(ii) The roughness scattering rate increases rapidly with decreasing quantum well thickness L as $1/L^6$ [163].

(iii) The Fermi level pinning at the dielectric/channel interface depletes the 2DEG as the channel thickness is reduced, resulting in an increase in the vertical electric field F in the channel and hence stronger electron confinement at the heterointerface that increases the scattering rate as F^2.

The high roughness leads to strong localization of electrons in the thinnest channel of 3.5 nm studied in [158], in which 2DEG conduction was believed to take place by a thermally activated hopping process with an extremely low mobility of 65 cm^2 V^{-1} s^{-1} at room temperature.

The mobility in the vertically scaled channels needs to be high to maintain low parasitic access resistance and high ballisticity [164]. To obtain both high charge density and high mobility in thin channels, a combined InAlN/AlGaN back-barrier is devised [165, 166]. The strong spontaneous polarization of InAlN lattice-matched to GaN enables the growth of relatively thick charge-inducing InAlN barriers without strain relaxation or strain-induced roughness, while the AlGaN reduces mobility degradation related to the lower growth temperature of InAlN. An MOCVD-grown heterostructure with a ~5-nm GaN channel demonstrates a 2DEG density of 1.9×10^{13} cm^{-2} and a room temperature mobility parallel to the step direction of 1350 cm^2 V^{-1} s^{-1}, corresponding to a low sheet resistance of 240 Ω sq^{-1}. In comparison, the MBE-grown 5-nm channel device studied in [158] has a much lower 2DEG density and room temperature mobility of 8×10^{12} cm^{-2} and <500 cm^2 V^{-1} s^{-1}, respectively. The higher mobility in the MOCVD device may be attributed to its higher charge density and a lower surface roughness of MOCVD materials than MBE materials that reduce components (i) and (iii) of interface roughness scattering discussed above.

5. N-polar GaN HEMT technologies

5.1. Microwave power devices

The development of N-polar microwave power HEMTs as baseline devices serves to evaluate the technology and establish the foundation for highly-scaled millimeter-wave

GaN HEMTs. Typical N-polar microwave power HEMTs reported consist of a 25-nm GaN channel layer, an Al(Ga)N back-barrier and an AlGaN cap layer for gate leakage reduction. The thickness and Al composition of the AlGaN cap are chosen to minimize its impact on channel conductance arising from 2DEG charge depletion. A CVD SiN_x gate insulator is deposited to protect the reactive N-polar surface during transistor fabrication, to further reduce the gate leakage, and to improve the gate voltage swing. Ni/Au/Ni and Ti/Al/Ni/Au metal stacks are used as the gate and alloyed ohmic contacts, respectively, with typical gate lengths of 0.6–0.7 μm. Large-signal dc-RF dispersion due to surface traps is suppressed by SiN_x passivation. Typical f_T and f_{max} values of these devices are ∼20 GHz and 40–60 GHz, respectively. Continuous-wave loadpull power measurements on N-polar HEMTs are performed with the devices biased in class AB and optimized for PAE.

Early studies of microwave power performance of N-polar HEMTs were conducted on MBE devices, which use a binary AlN back-barrier for strong back-barrier electron confinement and high electron mobility [124]. Large signal dc-RF dispersion due to the hole trap at the AlN-back-barrier/GaN-buffer interface is suppressed with Si modulation δ-doping below the AlN back-barrier. The first RF power measurements of N-polar GaN HEMTs, conducted at 4 GHz with $V_D = 40$ V, yield a maximum output power density (P_{out}) of 4.5 W mm^{-1} with an associated PAE of 34% and a transducer gain (G_T) of 10.3 dB [124]. The relatively poor power performance was ascribed to the unoptimized process steps of N-polar HEMTs including surface passivation. Significant improvement in the 4 GHz power performance is achieved by passivating the device prior to gate formation [167]. At $V_D = 35$ (40) V, loadpull measurements yield a P_{out} of 7.1 (8.1) W mm^{-1} with an associated PAE of 58% (54%) [109, 168]. Further progress in RF power performance is enabled by increasing the polarization-induced charge density using a dual-AlN back-barrier that leads to a lower on-resistance, a reduced knee voltage, a higher drain current and more optimal load impedance match. Power measurements of the dual-AlN back-barrier HEMT at 4 GHz with $V_D = 20$ (28) V yield a P_{out} of 4.1 (6.4) W mm^{-1} with an excellent PAE of 71% (67%) and an associated G_T of 13.1 (13.1) dB [169] (figure 13). At 10 GHz, the devices biased at $V_D = 28$ V deliver a P_{out} of 5.7 W mm^{-1} and an associated G_T of 7.1 dB at the peak PAE of 56%, which corresponds to an excellent peak drain efficiency (DE) of 70% (figure 14) [170]. Despite the limited output power densities due to relatively low breakdown voltages caused by a high density of conductive dislocations [171], the C-band and X-band power performance of MBE N-polar HEMTs compare favorably to state-of-the-art values reported for Ga-polar devices under similar bias conditions [172–177].

The maturity of MOCVD-grown N-polar GaN materials has enabled high performance RF devices. In contrast to the MBE devices, Si-doped graded-AlGaN back-barriers are adopted in MOCVD devices to eliminate dispersion effects caused by the interfacial hole trap [178]. While the dc characteristics are comparable between MBE and MOCVD

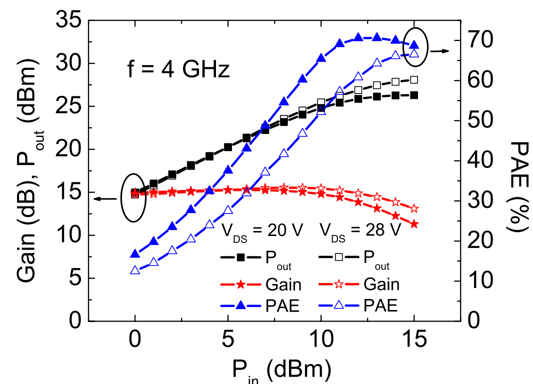


Figure 13. Large-signal performance of a PAMBE N-polar HEMT at 4 GHz with drain biases of 20 V (filled symbols) and 28 V (open symbols). A highest PAE of 71% is achieved. Copyright 2009 IEEE. Reprinted, with permission, from [169].

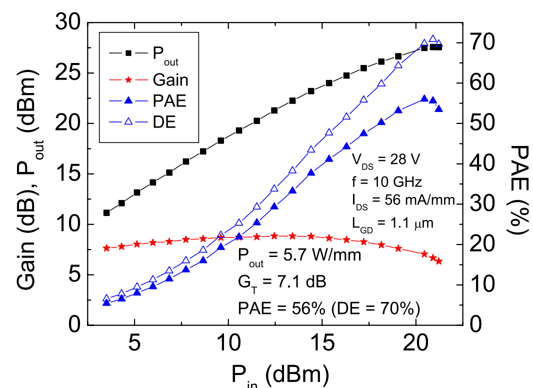


Figure 14. Large-signal performance of a PAMBE N-polar HEMT at 10 GHz with $V_{DS} = 28$ V. Copyright 2011 IET. Reprinted, with permission, from [170].

devices, the latter are able to sustain much higher breakdown voltages. Devices grown on sapphire substrates demonstrate high three-terminal breakdown voltages in excess of 170 V [179]. Power measurements at 4 GHz and $V_D = 50$ V yield a P_{out} of 12.1 W mm^{-1} with an associated G_T of 9.8 dB and an associated PAE of 55% (DE = 63%) [179]. The output power density of this device rivals that of Ga-polar HEMTs grown on sapphire [180]. Devices grown on SiC substrates experience much lower self-heating, which enables them to operate with higher power densities under continuous-wave conditions. At 4 GHz, these devices deliver a highest P_{out} of 20.7 W mm^{-1} with an associated PAE of 60% at 70 V [145] (figure 15). Peak PAE values > 74% are achieved at lower drain biases [145, 181]. At 10 GHz, a P_{out} of 16.7 W mm^{-1} with an associated PAE of 44% are achieved at 58 V (figure 16) [145], which compare well with that of Ga-polar devices reported in [176]. These results have encouraged developments of N-polar HEMTs for millimeter-wave power amplification.

5.2. *Self-aligned devices with regrown ohmics*

Significant improvements in the high frequency performance of GaN HEMTs can be achieved by reducing the source and drain access resistances to maintain scalability with decreasing gate length [182]. A self-aligned technique with regrown $n+$ InN/InGaN access regions is developed [183],

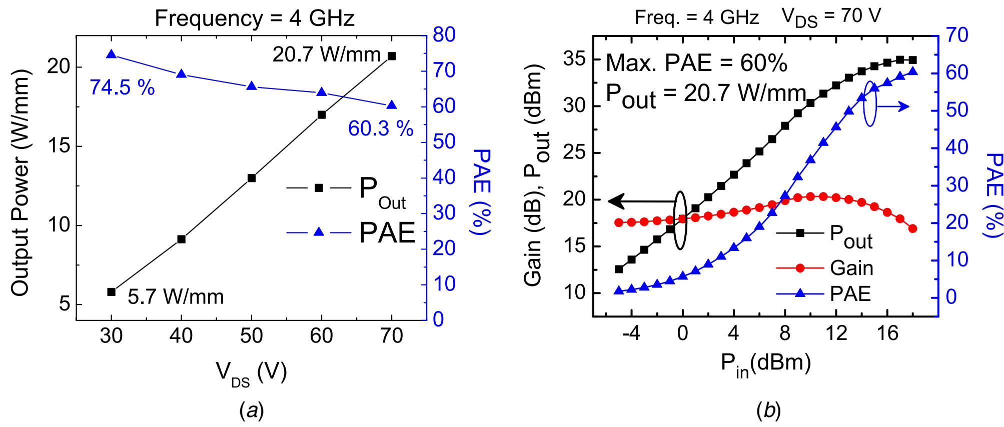


Figure 15. Large-signal performance of an MOCVD N-polar HEMT at 4 GHz. (*a*) The P_{out} increases linearly with V_{DS} without much degradation in PAE, indicating low dc-RF dispersion in the device. (*b*) Power sweep with increasing RF input power (P_{in}) at $V_{DS} = 70$ V. Copyright 2012 IEEE. Reprinted, with permission, from [145].

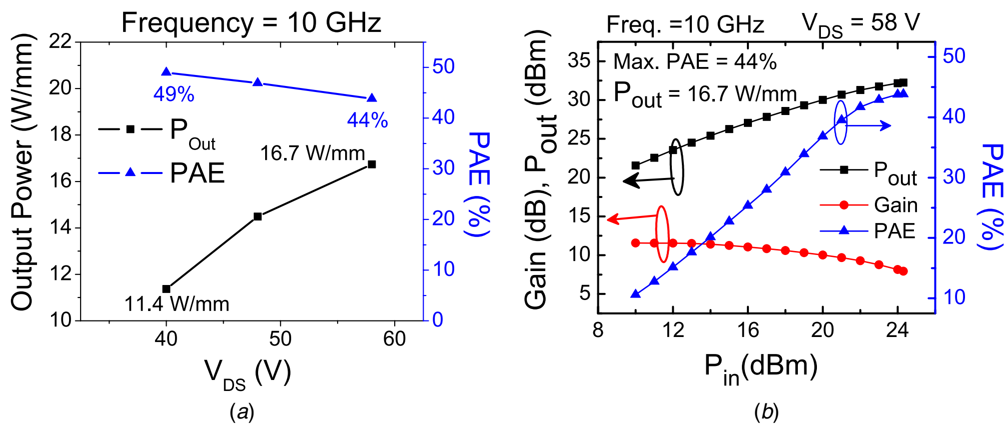


Figure 16. Large-signal performance of an MOCVD N-polar HEMT at 10 GHz. (*a*) The P_{out} increases linearly with V_{DS} without much degradation in PAE, indicating low dc-RF dispersion in the device. (*b*) Power sweep with increasing RF input power (P_{in}) at $V_{DS} = 58$ V. Copyright 2012 IEEE. Reprinted, with permission, from [145].

which minimizes the access region and improves the contact resistance value to almost an order of magnitude lower than the commonly published values in the literature. It is a scalable process that offers a huge potential in improving the high frequency performance of N-polar GaN HEMTs by decreasing parasitic resistances, decreasing parasitic delays, eliminating source-choke and reducing dc-RF dispersion.

The self-aligned technique is a gate-first technology adapted from InGaAs MOSFETs with self-aligned MBE-regrown source and drain [184, 185]. The process involves the deposition of a CVD SiN_x gate dielectric followed by a W/Cr/SiO_2/Cr refractory gate stack. The gates are then defined by electron beam lithography and subsequent selective etching. To isolate the gate metal from the regrown region, SiN_x sidewall spacers are formed by blanket deposition of PECVD SiN_x followed by a blanket vertical etch. The spacer thickness controls the source/drain access distances and hence the access resistances. After gate formation, graded-InGaN layers (40 nm) capped with InN (10 nm) are regrown in the access regions by PAMBE [57]. The polycrystalline growth on top of the gate finger is etched, followed by mesa isolation by reactive ion etching. Ti/Au-based nonalloyed ohmic contacts and probing contacts are then deposited. A cross-section

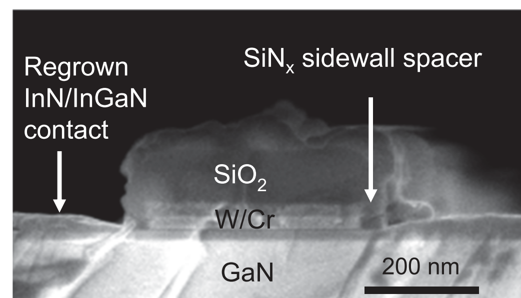


Figure 17. A cross-section SEM image of a gate-first self-aligned transistor after ohmic contact regrowth. The regrowth occurs at the gate edge without shadowing effects. Copyright 2009 IEEE. Reprinted, with permission, from [186].

scanning electron microscopy (SEM) image of a self-aligned HEMT is shown in figure 17.

The device structure in the initial studies consists of a graded $Al_xGa_{1-x}N$ ($0 < x \leqslant 0.3$) back-barrier, an AlN interlayer to reduce alloy scattering, a 10-nm GaN channel, a 5-nm SiN_x insulator and 40-nm SiN_x sidewall spacers [186]. A metal-to-2DEG contact resistance of 23 Ω-mm is achieved. The sheet resistance of the 2DEG is 600 Ω sq^{-1}, while the

combined sheet resistance of the regrown layer and the 2DEG in the access region is ~250 Ω sq^{-1}. A high saturation drain current ($I_{DS,sat}$) of 2.4 A mm^{-1}, a low on-resistance (R_{on}) of 0.6 Ω-mm and a knee voltage (V_{knee}) of 1.5 V are achieved in a 120-nm gate length device (figure 18). The I_{DS} remains high at low V_{DS}, with I_{DS} = 0.6 A mm^{-1} at V_{DS} = 500 mV for ($V_G - V_T$) = 3.5 V, where V_T is the threshold voltage. The transfer characteristics show a high peak extrinsic g_m of 530 mS mm^{-1} for V_{DS} = 5 V and 350 mS mm^{-1} for V_{DS} = 500 mV (figure 18). The extrinsic g_m remains relatively flat with increasing I_{DS} indicating that g_m-lowering due to source-choke has been suppressed by the highly doped source-access region in a self-aligned structure (figure 19). The off-state breakdown voltage measured at 1 mA mm^{-1} of leakage is 10 V with hard breakdown occurring at 25 V. A higher intrinsic drain voltage in a self-aligned structure causes lower breakdown voltages than in non-self-aligned devices. No current collapse or knee walkout is observed under pulsed *I–V* measurements, suggesting that the self-aligned devices with fully passivated narrow access regions have minimal surface-related dispersion effects. Small signal measurements show an f_T of 154 GHz and an f_{max} of 22 GHz at V_{DS} = 4.5 V for L_G = 120 nm, corresponding to an excellent $f_T \cdot L_G$ product of 18.5 GHz-μm. The f_T remains relatively constant with drain bias, indicating that a self-aligned structure minimizes drain delay. The f_{max} is low due to the high small-signal gate resistance (R_g) of 1.4 kΩ as a result of the thin (~100 nm) highly resistive W/Cr refractory gate metals, but may be readily improved with a T-gate process as will be discussed in section 5.3. An f_{max} of 270 GHz is simulated using a typical R_g of 5 Ω. With $f_T \cdot L_G$ products of 18–19 GHz-μm for L_G > 120 nm (figure 20) and exceptional dc characteristics at low supply voltages (V_{DS} = 500 mV), the performance of N-polar self-aligned HEMTs is competitive with not only the conventional AlGaN/GaN system but also narrow-bandgap technologies such as InGaAs and InSb for unipolar operation.

The variation of f_T with gate length for the device discussed in [186] was studied to assess the scalability of the self-aligned devices. As seen in figure 21, the peak f_T scales as $1/L_G$, demonstrating the advantage of a self-aligned structure in minimizing the effect of parasitic elements. The total delay (τ_{total}), which is defined as the sum of the intrinsic delay ($\tau_{intrinsic}$), the drain delay in the gate-extension region (τ_{drain}), the parasitic delay related to parasitic resistances and capacitances ($\tau_{parasitic}$), and the delay corresponding to the modulation efficiency of the gate that represents short channel effects (τ_{sc}), scales linearly with gate length (figure 21). With $\tau_{parasitic}$ reduced to ~10% of τ_{total} due to the self-aligned device architecture (figure 22), linear scaling of τ_{total} with L_G is maintained down to an aspect ratio of 6 (corresponding to L_G > ~100 nm for the device discussed in [186]), which is significantly lower than the optimum value of 15 reported for non-self-aligned Ga-polar devices [187]. The $f_T \cdot L_G$ product decreases sharply below an aspect ratio of 6 due to short channel effects, where the increasing τ_{sc} dominates the total delay.

To further improve the high-frequency performance with gate-length scaling while maintaining a high aspect ratio, the

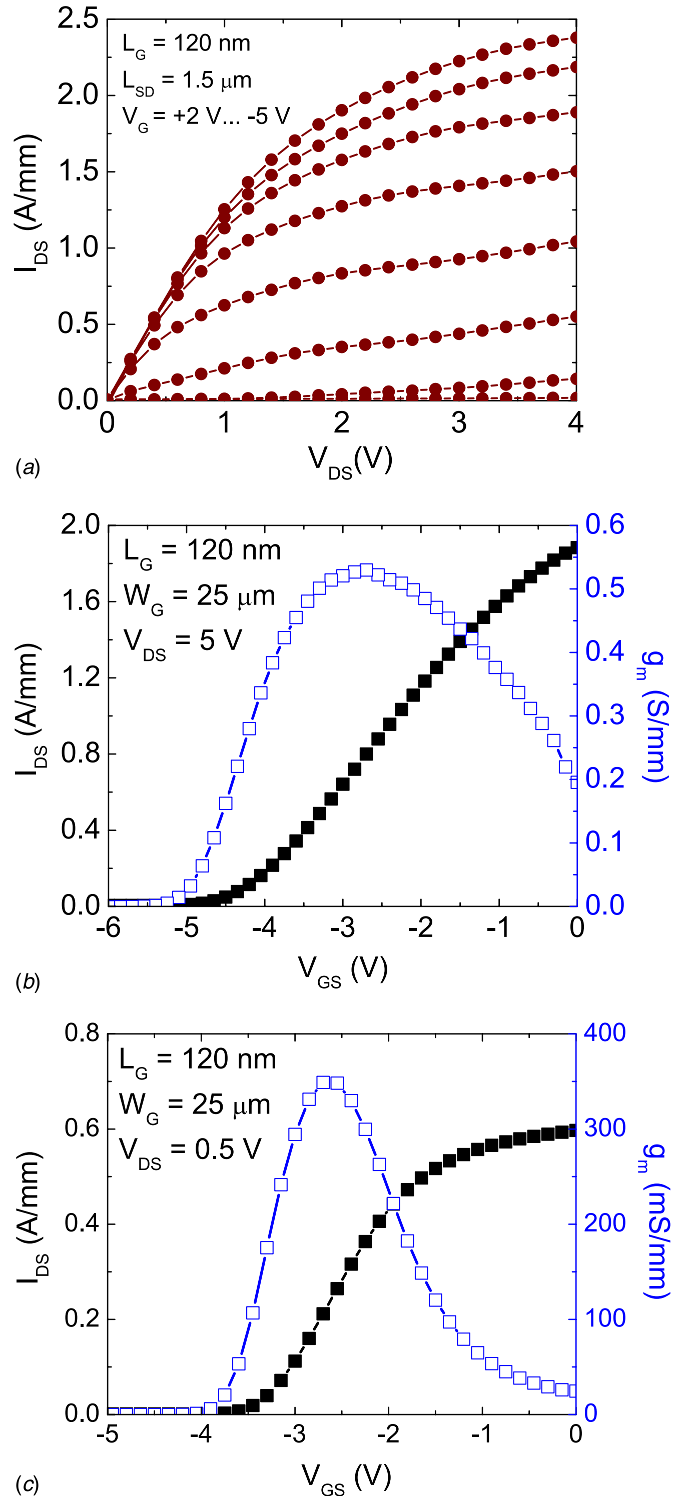


Figure 18. (*a*) Output dc characteristics of a self-aligned transistor with L_G = 120 nm showing an $I_{DS,sat}$ of 2.4 A mm^{-1} at V_{GS} = 2 V and an R_{on} of 600 Ω-μm for ($V_G - V_T$) = 7 V. (*b*) Transfer characteristics of the transistor with L_G = 120 nm showing a peak g_m of 530 mS mm^{-1} at V_{DS} = 5 V. (*c*) Transfer characteristics showing a peak g_m of 350 mS mm^{-1} at V_{DS} = 500 mV. Copyright 2009 IEEE. Reprinted, with permission, from [186].

GaN channel and SiN_x dielectric thicknesses are reduced to 7 and 3 nm, respectively, while the highest Al composition in the graded-AlGaN back-barrier is increased from 0.3 to

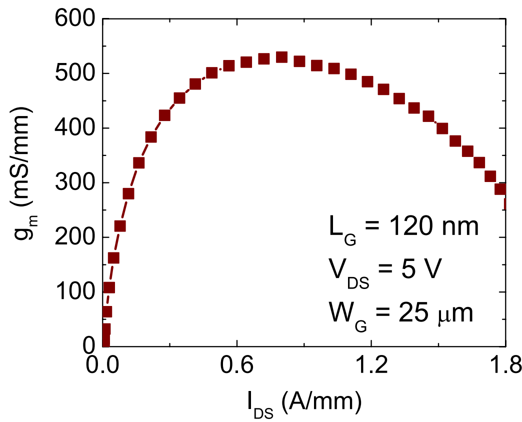


Figure 19. Variation of extrinsic g_m with I_{DS} showing little g_m-dropoff at high drain currents due to negligible source choke in the self-aligned transistor architecture. Copyright 2009 IEEE. Reprinted, with permission, from [186].

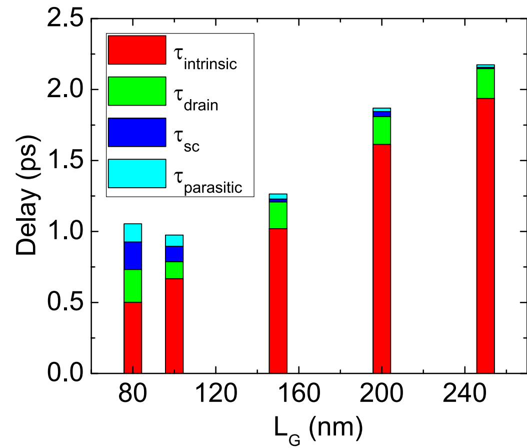


Figure 22. The various delay components for different gate lengths calculated from equivalent circuit models. Linear scaling of the total delay is maintained down to $L_G \sim 100$ nm (corresponding to an aspect ratio of ∼6 for the device discussed in [186]).

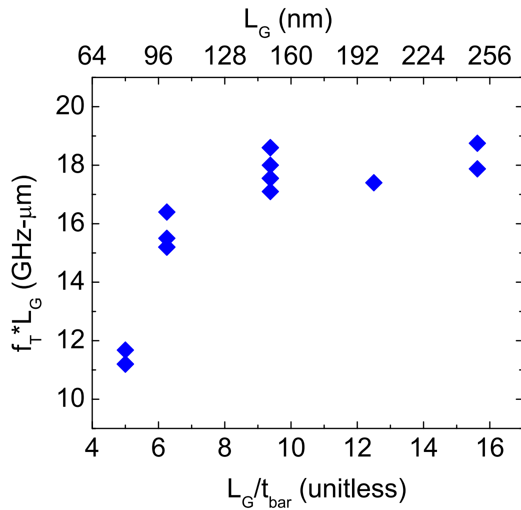
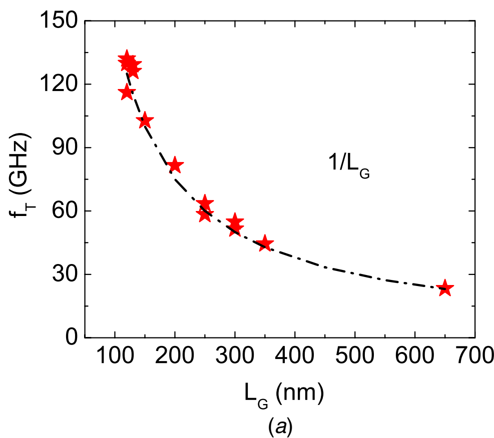


Figure 20. Variation of $f_T \cdot L_G$ product in a self-aligned transistor with aspect ratio (L_G/t_{barrier}) showing high $f_T \cdot L_G$ products of 18–19 GHz-μm for aspect ratios >10. Short channel effects severely degrade the $f_T \cdot L_G$ products for aspect ratios <6.

0.4 to compensate for the enhanced surface depletion of the 2DEG with a thinner GaN channel [159]. A sheet resistance of 750 Ω sq^{-1} is measured in this device. However, the electron mobility and average velocity are both degraded due to increased interface roughness scattering in the thinner GaN channel as discussed in section 4. The highest $f_T \cdot L_G$ product in the 7-nm channel device is only 12–13 GHz-μm for $L_G >$ 120 nm, in contrast to the 18–19 GHz-μm obtained for a 10-nm channel. A peak f_T of 210 GHz at $V_{DS} = 2$ V is obtained for $L_G = 30$ nm. With the SiN_x sidewall spacers removed and replaced by air gaps, a reduction in the gate–drain capacitance (C_{gd}) increases the f_T to 275 GHz, which is the highest f_T reported on an N-polar GaN HEMT and compares well to the state-of-the-art values of depletion-mode Ga-polar devices.

With the total contact resistance reduced to <50 Ω-μm, the relatively high 2DEG sheet resistance due to surface depletion is expected to dominate the on-resistance of the self-aligned transistors as the GaN channel thickness is reduced to <7 nm. An $\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ back-barrier lattice-matched to GaN with strong spontaneous polarization charge is used to overcome the limitations of large tensile strain and associated



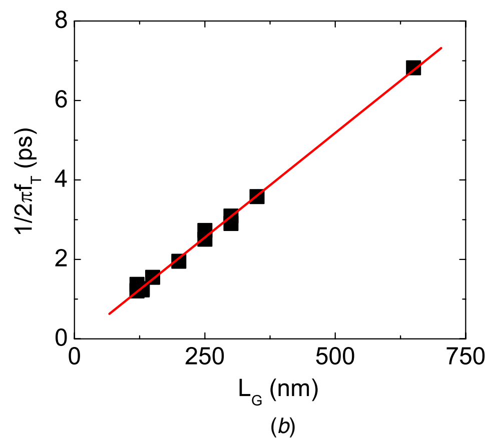


Figure 21. (*a*) The peak f_T scales as $1/L_G$ and (*b*) the total delay ($1/2\pi f_T$) scales linearly with L_G in a self-aligned device, demonstrating the advantage of the self-aligned structure in minimizing the effect of parasitic elements. Copyright 2009 IEEE. Reprinted, with permission, from [186].

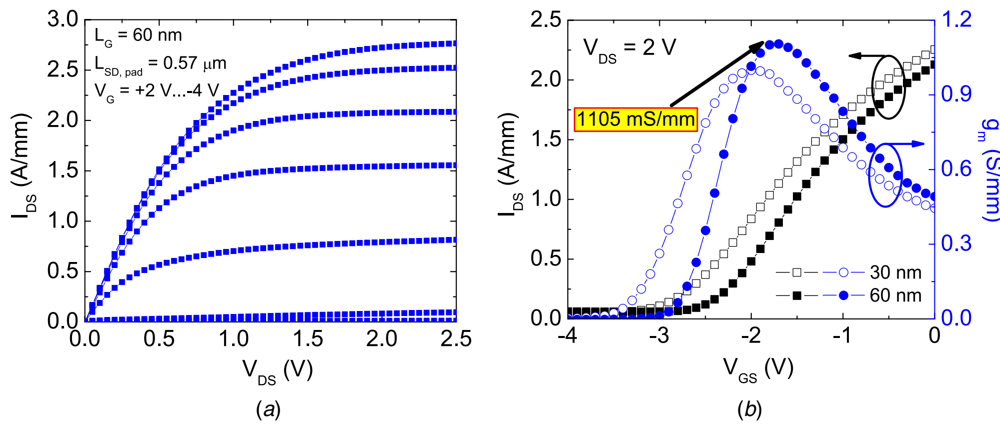


Figure 23. (*a*) Output dc characteristics of a self-aligned N-polar InAlN back-barrier HEMT with $L_G = 60$ nm, showing a maximum I_{DS} of 2.8 A mm^{-1} and an R_{on} of 0.29 Ω-mm at $V_{\mathrm{GS}} = 2$ V. (*b*) Transfer characteristics of the transistor at $V_{\mathrm{DS}} = 2$ V, showing $I_{\mathrm{DS,sat}}$ of 2.1 A mm^{-1} and 2.3 A mm^{-1} at $V_{\mathrm{GS}} = 0$ V and peak extrinsic g_m of 1105 mS mm^{-1} and 1000 mS mm^{-1} for $L_G = 60$ and 30 nm, respectively. Copyright 2012 IEEE. Reprinted, with permission, from [189].

low thermal budget imposed by high Al-composition AlGaN back-barriers on maintaining a high 2DEG charge density [188, 189]. A low sheet resistance of 330 Ω sq^{-1} is achieved with a 10-nm GaN channel, which is almost half of that obtained in the aforementioned AlGaN back-barrier device with the same channel thickness. Devices with 40-nm SiN_x sidewall spacers and a 60-nm gate show an $I_{\mathrm{DS,sat}}$ of 2.8 A mm^{-1}, a breakdown voltage as high as 24 V and a lowest R_{on} of 0.29 Ω-mm at $V_{\mathrm{GS}} = 2$ V with a peak extrinsic g_m of 1105 mS mm^{-1} (figure 23). This is the first report of >1 S mm^{-1} transconductance in a III-nitride HEMT. The f_T values scale well with the gate length for $L_G > 30$ nm with a peak f_T of 155 GHz measured at $V_{\mathrm{DS}} = 3$ V for $L_G = 30$ nm, but these values are not commensurate with the high dc g_m. It is hypothesized that the alloy composition inhomogeneity in PAMBE-grown InAlN introduces fast shallow traps that cause additional delays under high electric fields, resulting in L_G-dependent dispersion in the small-signal gate–source capacitance (C_{gs}) and g_m [188]. An $f_T > 350$ GHz is predicted in these devices with $L_G < 60$ nm if these shallow traps were eliminated using MOCVD- or ammonia-MBE-grown InAlN [190, 191].

Enhancement of the average electron velocity beyond the saturation velocity is often observed in the self-aligned transistors [159, 188, 189, 192]. This phenomenon is apparent from the increase in $I_{\mathrm{DS,sat}}$ and/or g_m with decreasing gate length for $L_G < 100$ nm (figure 24), or with thinner SiN_x sidewall spacers that effectively decrease the gate–drain distances. The velocity enhancement effect is attributed to the penetration of drain field under the gate causing a higher average electric field in the channel. This phenomenon has also been observed by Shinohara *et al* who reported significant enhancement in electron velocity with increasing drain voltage for reduced gate–drain spacing [29, 32]. Average intrinsic velocities as high as $1.5 - 1.8 \times 10^7$ cm s^{-1} are measured for the self-aligned N-polar GaN devices indicating a huge opportunity for achieving good high-frequency performance in these transistors [192].

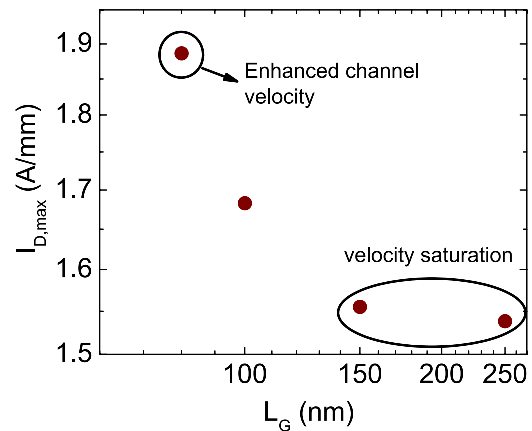


Figure 24. Scaling behavior of $I_{\mathrm{DS,sat}}$ at (V_{DS}, V_{GS}) = (2.5 V, 2 V) with L_G showing enhancement in $I_{\mathrm{DS,sat}}$ and hence increase in average electron velocity for $L_G < 100$ nm. Copyright 2011 IEEE. Reprinted, with permission, from [192].

5.3. Gate-last process with regrown ohmics

The gate-first process presented in the last section uses a thin refractory metal stack (W/Cr) for the gate to withstand the InN/InGaN ohmic regrowth temperature of ∼575 °C, as well as SiN_x sidewalls to define the source–gate and gate–drain regrowth spacings that are symmetrically self-aligned to the gate. The process results in record f_T values and clean comparisons between the gate length and all device parameters due to the absence of alignment variation. These devices demonstrate building blocks for higher frequency performance, but they suffer from a high gate resistance due to the thin gate metal stack that causes the f_{max} required of power devices to be almost one order of magnitude lower than the f_T. Attempts to increase f_{max} using a self-aligned T-gate based on the refractory-metal gate-first process have resulted in only modest success due to a large parasitic capacitance [157, 193]. Therefore, a gate-last technique with regrown ohmic contacts is developed to fabricate highly-scaled N-polar HEMTs with sub-100-nm T-gates re-aligned in sub-200-nm source–drain spacings, allowing both high f_T and record f_{max} values to be

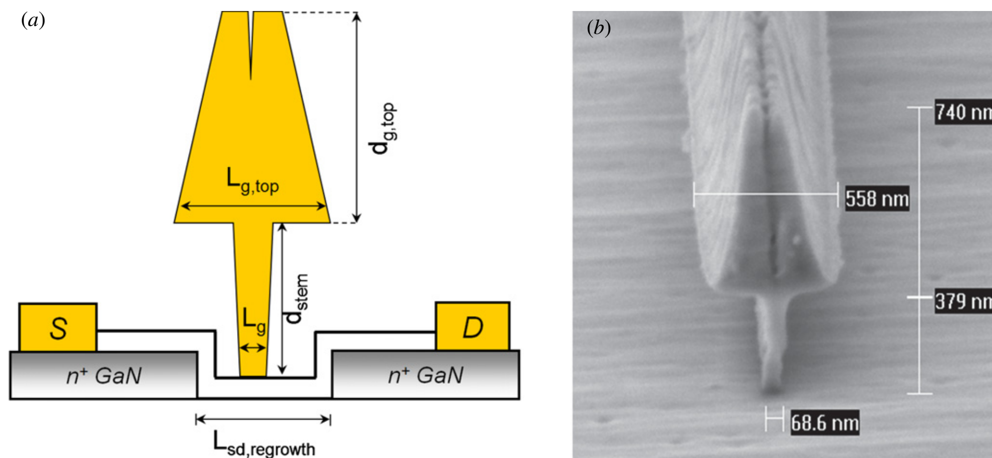


Figure 25. (*a*) A cross-section schematic of a T-gate and its layout variations for highly-scaled gate-last N-polar HEMTs. (*b*) An SEM micrograph of a Ti/Au high aspect ratio T-gate with L_G, stem height and total gate metal thickness of 70 nm, 380 nm and 1.1 μm, respectively.

achieved simultaneously in addition to flexibility in offsetting the gate [194]. This T-gate process is distinct from that developed by Nidhi *et al* who adopts an $n+$ cap layer for ohmic contacts followed by gate recess and realignment [195, 196].

The gate-last process begins with patterning a SiO_2 mask using electron-beam lithography and dry etching for selective-area $n+$ GaN or bilayer unintentionally-doped (UID)/$n+$ GaN ohmic regrowth by PAMBE. The major advantage of GaN regrowth over InN/InGaN regrowth is its ability to withstand the high temperature (~1000 °C) of subsequent CVD SiN_x gate dielectric deposition after the SiO_2 regrowth mask is stripped [197]. Moreover, the UID/$n+$ GaN bilayer is more advantageous over the single layer $n+$ regrowth for reducing dc-RF dispersion as a larger portion of the drain access region is self-passivated. Nonalloyed ohmic contacts are subsequently formed with Ti/Au, followed by mesa isolation of devices and probe pad metallization. Finally, a high aspect ratio T-gate is patterned in a two-step electron-beam resist process, and a Ti/Au gate stack is deposited in a single electron-beam evaporation followed by liftoff. Typically, the top-gate metal thickness is 750 nm with a 380-nm-tall stem, resulting in an ~1.1-μm-tall T-gate. The thick top gate reduces gate resistance by increasing the cross-sectional gate area, while the tall stem reduces the parasitic capacitance originating between the top gate and other components of the device (figure 25).

The $n+$ regrowth yields contact resistance values of 0.058–0.073 Ω-mm between the metal and the 2DEG. These low resistances, being limited by the contact resistance between Ti and the $n+$ GaN, rival those achieved using InN/InGaN regrowth. Initial demonstrations of the gate-last process flow on 10-nm GaN channel devices using an AlGaN back-barrier with unoptimized device dimensions quickly yield large improvements in f_{max} from ~200 GHz [196] to values in excess of 300 GHz [198]. Significant reductions in parasitic resistance and enhancements in channel conductivity are enabled by replacing the AlGaN back-barrier with InAlN, resulting in an f_{max} of 400 GHz which is among the highest in GaN HEMTs [199]. Further scaling of the GaN channel thickness while maintaining both high charge and high mobility is achieved with the use of a combined InAlN/AlGaN back-barrier [165, 166], resulting in a low sheet resistance of 228 Ω sq^{-1} for a 5.4 nm GaN channel. The dimensions of this device, including a source–drain spacing of approximately 200 nm, a top-gate length of 300 nm, a top-gate height of 750 nm and a gate width of 2 × 12.5 μm, are chosen after systematic small signal analyses and process optimization. For a gate length of 60 nm, this device shows a high $I_{DS,sat}$ of 2.1 A mm^{-1} at $V_{GS} = 0$ V with a V_T of −1.8 V. The peak extrinsic g_m and R_{on} of > 1.65 S mm^{-1} and 0.246 Ω-mm, respectively, are among the best for a depletion-mode GaN HEMT (figure 26) [200]. A low output conductance of 10 mS mm^{-1} and as little as 15 mV V^{-1} of DIBL are measured at the peak g_m bias point. The three-terminal breakdown voltage is in excess of 14 V. An f_T of 163 GHz and state-of-the-art peak f_{max} of 405 GHz are measured in an 80 nm device at $V_{DS} = 8$ V (figure 27) [200]. The highest f_T obtained from this device is 200 GHz at $V_{DS} = 5$ V with a 70 nm gate ($f_T \cdot L_G = 14$ GHz-μm), which is unprecedented for this gate length. According to the empirical model developed by Jessen *et al* [187], it is predicted that a 20 nm gate on this same structure would yield an f_T of 390 GHz and a 10 nm gate would yield an f_T of over 480 GHz. By further reducing the GaN channel thickness to 4 nm and the SiN_x thickness to 1 nm without degrading the sheet resistance, the f_T would be 480 and 635 GHz for 20- and 10-nm gates, respectively. These results and subsequent developments [201] promise the adoption of N-polar HEMTs for MMICs operating in the millimeter-wave band.

5.4. Enhancement-mode devices

While Ga-polar or N-polar GaN HEMTs are typically normally-on, certain applications have driven the development of E-mode devices. The lack of high-quality GaN *p*-channel FETs presents direct-coupled or super-buffered FET logic topologies featuring monolithically integrated E/D-mode HEMTs as the practical configurations for GaN digital integrated circuits that are attractive for high-performance mixed-signal circuits, high temperature electronics and smart

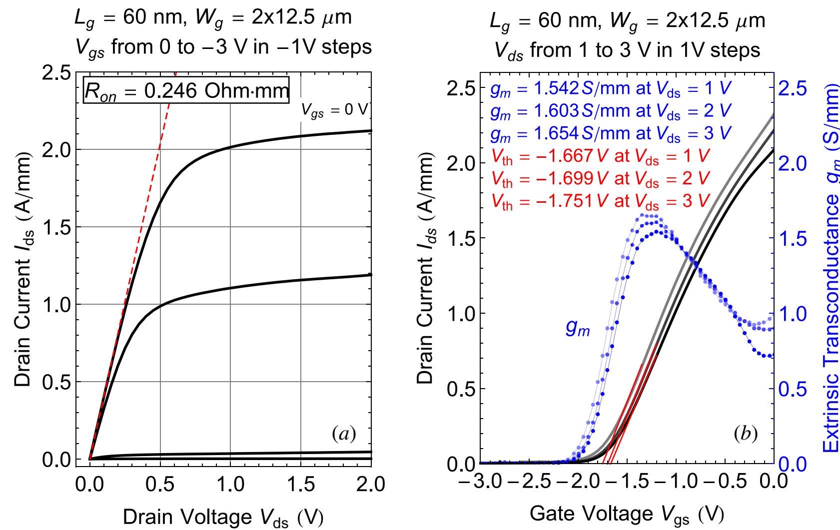


Figure 26. (*a*) Dc output and (*b*) transfer characteristics of a 60 nm N-polar HEMT using the gate-last process. The output current is over 2.1 A mm^{-1} and the R_{on} is 0.246 Ω-mm at $V_{GS} = 0$ V. A peak extrinsic g_m of over 1.65 S mm^{-1} is achieved at $V_{DS} = 3$ V.

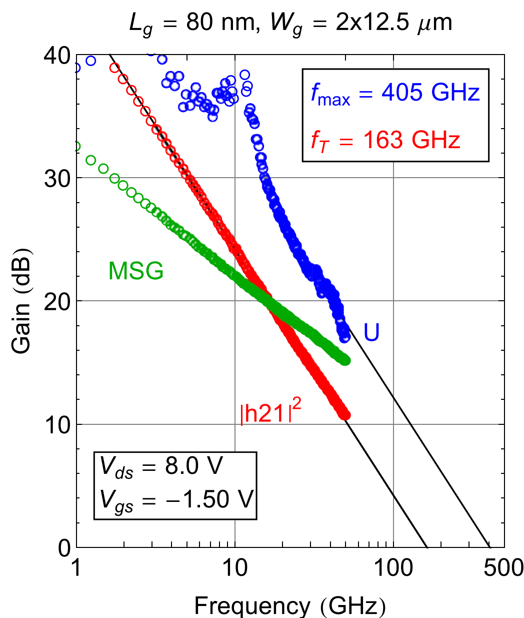


Figure 27. Small-signal high-frequency performance of an 80 nm gate-last GaN/InAlN/AlGaN HEMT with a 5.4 nm GaN channel showing a highest f_{max} of 405 GHz.

power applications. E-mode devices also allow the elimination of a negative-polarity power supply, leading to simplified circuit topologies and system architecture.

Techniques to realize Ga-polar E-mode HEMTs include gate recesses [202–205], CF_4 plasma treatment under the gate [205–210], V_T control using a thin gate dielectric [210, 211], *p*-type (Al)GaN cap layers [212, 213] and InGaN cap layers [214]. In an N-polar HEMT, E-mode operation is enabled by the polarization-induced field of a thin (2–3 nm) AlN layer grown on top of the GaN channel layer to deplete the 2DEG induced by the polarization of the back-barrier [215]. Following the deposition of a gate dielectric, a self-aligned gate-first process similar to that of D-mode N-polar HEMTs is used to fabricate E-mode devices [183–185]. The AlN in the access regions is removed to recover the 2DEG for low access resistance, and a composite W/Cr/SiN_x refractory gate stack instead of W/Cr/SiO_2 is used to allow selective wet-etch of the AlN over GaN by hydrofluoric acid [215].

The first self-aligned N-polar E-mode HEMTs comprise a strained AlN back-barrier, a 20 nm GaN channel and a high temperature CVD SiN_x as gate dielectric (figure 28) [215]. At $V_{DS} = 4$ V, devices with a 0.62 μm gate length show a peak I_{DS} of 0.74 A mm^{-1} at $V_{GS} = 5$ V, a peak g_m of 225 mS mm^{-1} and a V_T of +1.0 V. As is the case of the self-aligned D-mode devices, the breakdown voltages of the self-aligned E-mode devices are lower than that of the non-self-aligned structures reported in the literature. With decreasing gate lengths, these E-mode devices show V_T roll-off due to drain-induced barrier lowering (DIBL) with the 0.18 μm gate length device showing D-mode operation. The self-aligned drain results in a higher intrinsic drain voltage that enhances the V_T roll-off relative to Ga-polar devices of comparable aspect ratios [216].

For high frequency operation at sub-100 nm gate lengths, the vertical dimension of the devices is scaled by reducing the GaN channel thickness from 20 to 8 nm [217]. E-mode operation is maintained at a much shorter L_G of 70 nm with $V_T = +0.7$ V at $V_{DS} = 3$ V. Despite the increased gate–channel capacitance, the dc output resistance of this device shows little improvement over that of the previous device. Nevertheless, the reduced transit time due to the short gate results in much improved high frequency performance with a peak f_T of 120 GHz measured at $V_{DS} = 3$ V. The corresponding f_{max} of 11 GHz is low due to the high gate resistance.

Subsequent devices with further vertical scaling consist of a 5 nm GaN channel and a high-*k* Al_2O_3 gate dielectric instead of SiN_x to scale the equivalent oxide thickness [218]. The closer proximity of the surface to the 2DEG in scaled channels necessitates increasing the Si modulation doping density to compensate for the enhanced surface depletion and control the V_T under the gate. As a consequence, the charge density under the sidewalls increases substantially from 4.5×10^{12} cm^{-2} for

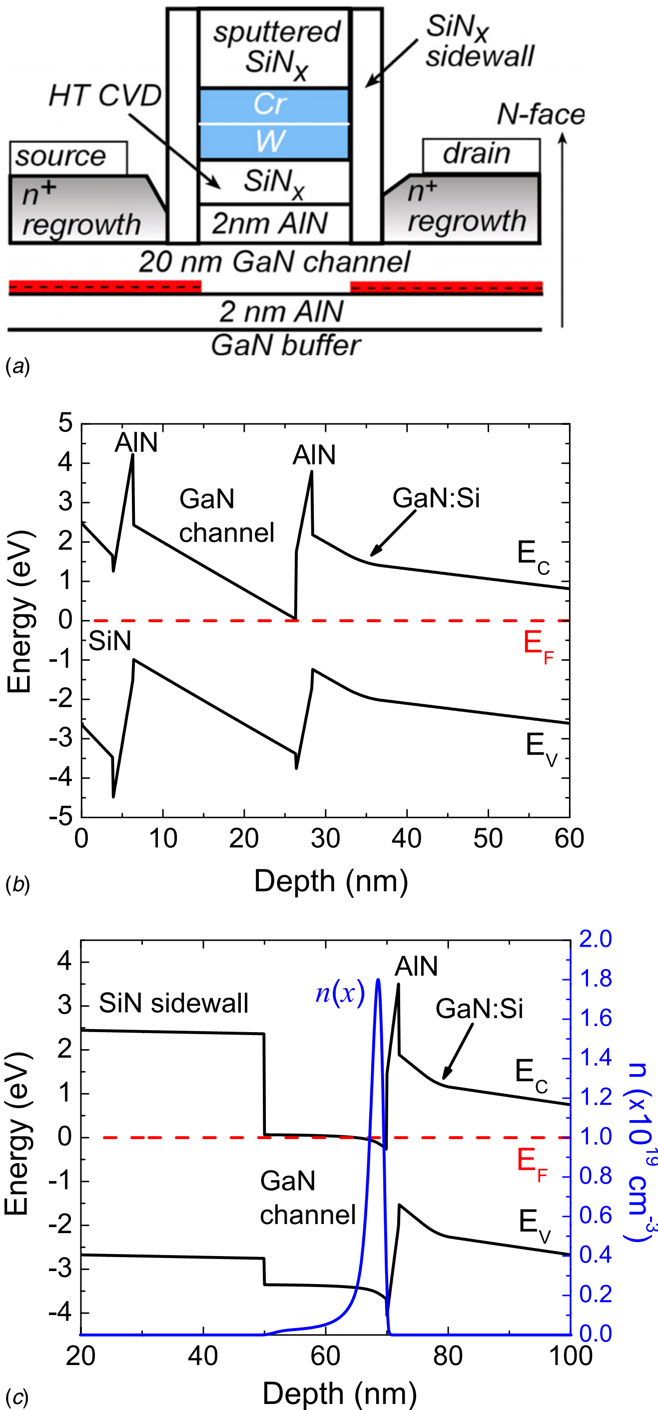


Figure 28. (*a*) A cross-section schematic of a self-aligned N-polar E-mode HEMT. (*b*) An equilibrium band diagram under the gate showing normally-off operation. (*c*) An equilibrium band diagram under the sidewall regions. Copyright 2011 IEEE. Reprinted, with permission, from [215].

the 20 nm channel device [215] to 7.5 × 10^{12} cm^{-2} for the 8 nm channel [217] and 1.7 × 10^{13} cm^{-2} for this 5 nm channel device [218]. A graded-AlGaN back-barrier is introduced into the structure to improve drain current saturation and device pinchoff over the past device generations [62]. Due to the higher output resistance, the maximum on/off current ratio (I_{on}/I_{off}) of 2.2 × 10^5 is 300–3000 times higher than that of the past device generations measured under similar bias conditions. At V_{DS} = 4 V, the device has a V_T of +1.6 V, an I_{DS} of 1.15 A mm^{-1} at V_{GS} = 5.5 V, a peak g_m of 510 mS mm^{-1} and an off-state breakdown voltage of 8.6 V. The R_{on} of 0.66 Ω-mm is the best reported for N-polar E-mode HEMTs (figure 29). A peak f_T of 122 GHz is obtained (figure 30), with the associated $f_T \cdot L_G$ product of 14 GHz-μm being a significant improvement over the 8 nm channel device. An f_T of 280 GHz can be achieved at 50 nm gate length if the same $f_T \cdot L_G$ product is maintained.

6. N-polar GaN on Si

Due to their high thermal stability, large polarization-induced charge density, high electron velocity and strong carrier confinement with heterostructures, GaN-based transistors have been envisioned to complement and even exceed the performance of the Si technology for high-performance digital circuits and high-temperature electronics [219, 220]. Heterogeneous integration of GaN with Si on the same wafer will add new functionalities to the Si circuits [221, 222]. In addition, Si substrates provide a large-area and low-cost platform for fabricating GaN devices using existing complementary-MOS (CMOS) infrastructure to reduce manufacturing costs [223, 224].

Heteroepitaxy of wurtzite GaN on Si (1 1 1) has been challenging due to the large mismatch in lattice constant and thermal expansion coefficient between the two materials. Strategies to nucleate N-polar materials on Si by PAMBE include substrate nitridation to form SiN_x followed by nucleation under N-rich conditions [225, 226], or controlled deposition of Al metal on Si prior to growth initiation [227]. The first N-polar transistors on Si substrates are demonstrated with MOCVD on misoriented Si (1 1 1) by inverting a Ga-polar film to N-polar [228, 229]. Si substrates with a miscut of 3.5° toward [1 1 $\bar{2}$] or [1 $\bar{1}$ 0] are investigated. The growth is initiated with an AlN layer, followed by the growth of strain management layers consisting of either a single AlGaN layer compositionally graded from AlN to GaN or a series of $Al_xGa_{1-x}N$ layers where x is reduced in steps from 0.65 to 0.17 [230–232]. The growth process continues with the deposition of the main GaN buffer layer followed by the HEMT structure. N-face polarity is achieved by heavy Mg doping of the AlGaN strain management layers [97, 98]. The Mg doping leads to complete polarity inversion from Ga-face to N-face; no inversion domains can be found by TEM. To avoid any impact of the Mg doping on device performance, Mg-doped layers and active device layers have to be separated by an undoped spacer layer with a thickness in excess of 600 nm. The optimum Si substrate misorentation direction is [1 1 $\bar{2}$], resulting in GaN films misoriented toward the *m*-plane with smooth surfaces and a regular step structure [229]. Room temperature electron mobility values of 1508 cm^2 $V^{-1}s^{-1}$ and 1760 cm^2 $V^{-1}s^{-1}$ parallel to the step direction are measured for samples with sheet carrier densities of 9.6 × 10^{12} cm^{-2} and 6.3 × 10^{12} cm^{-2}, respectively, in the absence of a mobility-enhancing AlN interlayer between the AlGaN back-barrier and the GaN channel [228]. The initial devices exhibit an I_{DS} of 0.35 A mm^{-1} at a V_{GS} of 0 V and a V_T of −6 V [229].

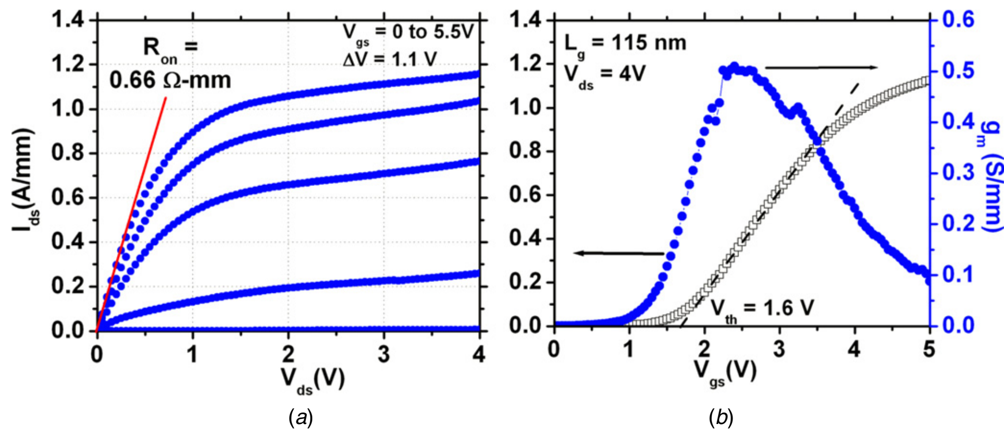


Figure 29. (*a*) Output and (*b*) input dc characteristics of a 115 nm N-polar E-mode HEMT with a 5 nm GaN channel. Copyright 2012 IEEE. Reprinted, with permission, from [218].

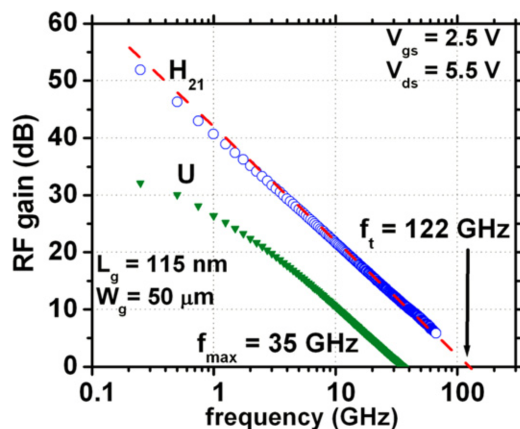


Figure 30. Small-signal high-frequency performance of a 115 nm N-polar E-mode HEMT with a 5 nm GaN channel showing a peak f_T of 122 GHz. Copyright 2012 IEEE. Reprinted, with permission, from [218].

A wafer bonding technology is also developed to fabricate N-polar GaN HEMTs on Si. A Ga-polar heterostructure grown on a Si (1 1 1) substrate is bonded to a Si (100) carrier wafer, followed by Si (1 1 1) substrate removal to expose the N-polar surface for device fabrication [233, 234]. This process, scalable to 100-mm wafers [234], circumvents the technical challenges of N-polar GaN epitaxy on Si and realizes high-quality GaN devices on the mainstream CMOS Si (1 0 0) platform without the need for substrate miscut [235–238]. The resulting N-polar HEMTs show a low sheet resistance of 240 Ω sq^{-1} [233], a low surface roughness of 1 nm [234] and a high electron mobility of 1700 cm^2 V^{-1} s^{-1} preserved from its native Ga-polar reference device [234]. Further process optimization is needed to fully develop the performance of these devices.

7. Polarization-induced doping

Polarization charges in wurtzite GaN can be harnessed to generate polarization-induced *n*-type or *p*-type layers that are highly conductive without carrier freezeout at cryogenic temperatures [239]. When a polar heterojunction is compositionally graded, the fixed polarization sheet charge at the heterointerface spreads to a fixed bulk charge. In response to the macroscopic electric field created by the fixed polarization charge, neutralizing mobile carriers also spread from a sheet charge into a 3D bulk charge to screen the electric field. High carrier densities are possible in the graded layers since dopants are ionized by an electrostatic field without being limited by low thermal ionization efficiencies. Polarization-induced doping is first demonstrated for both *n*-type and *p*-type conductive layers on metal-polar heterostructures [240–242]. Field-effect transistors with tailored transconductance profiles for improved linearity have also been demonstrated with this technique [243, 244]. The formation of a mobile electron gas in a graded metal-polar III-N semiconductor layer does not require extrinsic doping since the semiconductor surface provides remote donors [63].

The concept of polarization-induced doping has been applied to N-polar heterostructures for low-resistivity ohmic contact layers in HEMTs and hole injectors in UV light-emitting diodes [57, 245, 246]. By grading an N-polar crystal from GaN to InGaN, the fixed polarization charge is positive and should induce the formation of a 3D electron gas. Grading in the opposite direction from GaN to AlGaN should result in a 3D hole gas. Carriers in compositionally graded layers may be localized by traps or defects within the layers [239], as a result of which Si and Mg dopants are supplied to the graded N-polar InGaN and AlGaN layers, respectively, to compensate the traps/defects before mobile carrier gases could form.

8. Conclusion

N-polar GaN heterostructures offer intrinsic scaling advantages for high-frequency transistors. Contact resistance values below 25 Ω-μm are obtained using $n+$ InN/InGaN contact regrowth. D-mode devices exhibiting extrinsic g_m of 1.65 S mm^{-1}, $I_{DS,sat}$ of 2.8 A mm^{-1}, f_T of 275 GHz and f_{max} in excess of 400 GHz are demonstrated, which are among the best performing GaN HEMTs reported in the literature (figures 31, 32). High $f_T \cdot L_G$ products of 18–19 GHz-μm are achieved for $L_G > 120$ nm with aspect ratios >10, and linear scaling of delay with L_G is maintained down to a gate length of 30 nm using

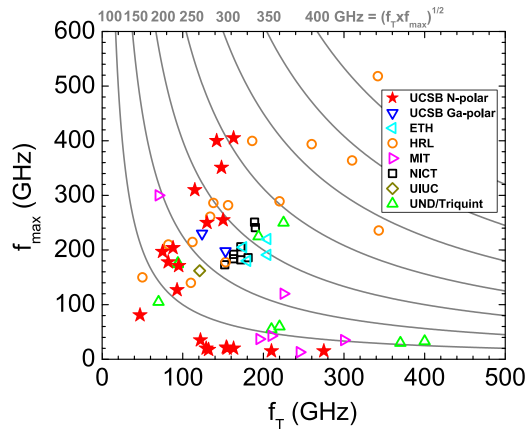


Figure 31. Comparison of peak f_T and f_{max} of N-polar GaN HEMTs with state-of-the-art Ga-polar GaN HEMTs. The UCSB N-polar data are obtained from this work. The other data are obtained from [2–50].

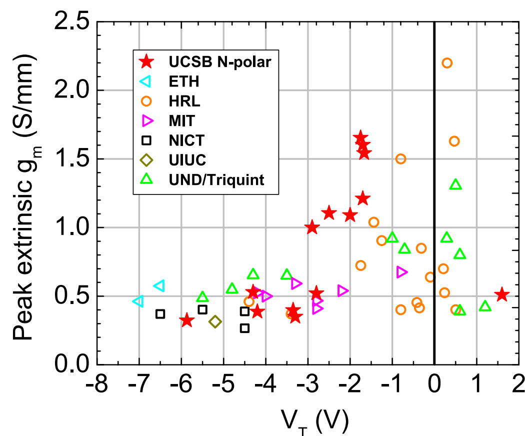


Figure 32. Comparison of peak extrinsic g_m versus V_T of N-polar GaN HEMTs with state-of-the-art Ga-polar GaN HEMTs. The UCSB N-polar data are obtained from this work. The other data are obtained from [2–50].

InAlN back-barriers. The concurrent development of E-mode devices will enable high-performance digital and mixed-signal circuits based on N-polar GaN. Outstanding microwave power performance in the C- and X-band with PAE > 70% and P_{out} > 20 W mm^{-1} at 4 GHz promise the adoption of N-polar HEMTs for MMICs operating at millimeter-wave frequencies.

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