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# Nanopatterned Graphene Field Effect Transistor Fabricated Using Block Co-polymer Lithography

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We demonstrate a successful fabrication of Nanopatterned Graphene (NPG) using a PS-*b*-P4VP polymer, which was never used previously for the graphene patterning. The NPG exhibits homogeneous mesh structures with an average neck width of ~19 nm. Electronic characterization of single and few layers NPG FETs (field effect transistors) were performed at room temperature. We found that the sub-20 nm neck width creates a quantum confinement in NPG, which has led to a bandgap opening of ~0.08 eV. This work also demonstrates that BCP (block co-polymer) lithography is a pathway for low-cost, high throughput large-scale production of NPG with critical dimensions down to the nanometer regime.

**Keywords:** Graphene, Multilayer Graphene, Block Copolymer Lithography, Graphene Nanopatterning, Field Effect Transistor

**1. Introduction** Recently, graphene has emerged as a new material for its remarkable electronic properties.[1,2] Besides single-layer graphene (SLG), two and few layers graphene (FLG) are of interest for future device applications.[2,3] Electronic transport in graphene is dramatically different from that of a conventional 2D material since energy dispersion of electrons linearly scales with momentum near the Dirac point.[4] A high electron mobility value such as 200,000 $cm^2V^{-1}s^{-1}$ was observed in suspended graphene sheets.[5] Thus, its superior mobility over silicon makes it a promising candidate for the future electronic devices. However, due to the semi-metallic nature of graphene it lacks a bandgap, which is necessary for technological applications such as field effect transistors (FETs). Hence, this results in a very low on/off ratio in graphene FET devices. For practical applications, an on/off ratio on the order of $10^5$ is needed. One way to open a bandgap in graphene is to create geometrical constrictions of graphene material. This will lead to a confinement of electrons, thus opening a bandgap. A bandgap opening up to 200 meV has been observed in graphene nanoribbons (GNRs) fabricated by lithographic methods.[6] However, this requires expensive fabrication methods and the driving current is very low in such nanoribbon structures.

In order to increase the driving current for practical applications, the fabrication of dense, ordered nanoribbon arrays is required, which has been achieved by electron-beam lithography.[7,8] Although conventional lithographic methods can provide precisely located nanoarrays, the size of the area that can be patterned is often limited to the micrometer scales due to its intrinsic time-consuming nature of serial processing in addition to the limited processing resolution. Sinitskii and Tour [9] used nanosphere lithography to prepare a porous metal film, which was then employed as an etch mask for fabrication of graphene nanomesh (GNM), however it had unsatisfactory geometrical dimensions. As an alternative, self-assembly nanoarrays have been extensively investigated, such as a block co-polymer (BCP) and anodized aluminum oxide. One of the most fascinating properties of self-ordered nanoarrays lies in the readiness of its fabrication on length scales that are difficult to obtain by standard semiconductor lithography technique.[10]

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Liang et al. combined the self-assembly of BCPs and nano-imprint lithography to prepare GNM with neck width ($w$) down to less than 10 nm, but the template preparation process is complicated.[11]

Recently, Kim et al. reported the fabrication of nanoperforated graphene materials with sub-20-nm features, using a P(S-*b*-MMA)-based cylinder-forming BCP.[12] However, for the nanostructuring, a thin cross-linked P(S-*r*-MMA-*r*-GMA) buffer layer had to be employed between the P(S-*b*-MMA) template and the graphene layer. An introduction of a controlled buffer layer and the eventual removal of such an extra material layer adds to the complexity of the material structure and processing as well as the cost, with an implication to the scale-up manufacturing. Therefore, we have employed a different BCP based on PS-*b*-P4VP with which we could eliminate the extra buffer layer.

Moreover, P(S-*b*-MMA) is known to undergo desirably structured two-phase separation in thin films when annealed only at temperatures above the glass transition temperature ($T_g$) of both polymers.[13–15] However, sometimes annealing causes a problem of macrophase separation in the BCP, with small molecules undesirably crystallizing out of BCP.[16,17] Ikkala and coworkers pointed out that extensive annealing at elevated temperatures can cause macrophase separation in their BCP.[17] Therefore, a Poly(styrene-*b*-4-vinylpyridine) (PS-*b*-P4VP) BCP was used instead in the present work. PS-*b*-P4VP has a high Flory–Huggins interaction parameter, which is expected to minimize the edge roughness and is scalable for producing dense periodic arrays and high selectivity between the two blocks.

An additional advantage of PS-*b*-P4VP over P(S-*b*-MMA) is that PS-*b*-P4VP is much more versatile, allowing either solvent vapor annealing or thermal annealing in order to induce ordered micro-phase separated structures. The solvent annealing process is useful in the processing of BCP films because the structural orientation can be controlled by the evaporation rate and the high residence time of the solvent in the film, which can provide enough polymer mobility to attain long-range structural order. The use of P(S-*b*-MMA) on the other hand does not easily allow such a solvent annealing process.

Here, we report the production of a graphene nanostructure that can open up a bandgap in a large sheet of both SLG and FLG. While extensive studies have been carried out on the physical properties of SLG, less is known about the electrical properties of FLG structures, with few previous reports. We also present experimental results in FLG FET devices comparing with SLG devices and discuss the implications for the device performance. The patterned graphene is prepared using a BCP lithography and the more versatile BCP PS-*b*-P4VP (as compared to the previously investigated BCPs), which is the first-ever demonstration for PS-*b*-P4VP-based graphene nanopatterning application to our knowledge.

Such nanostructuring process using PS-*b*-P4VP can effectively open up a conduction bandgap in a large piece of graphene. The fabrication of nanopatterned graphene (NPG) using the PS-*b*-P4VP BCP approach allows easier and scalable fabrication of nanoscale pores in graphene on a $SiO_2$-coated Si substrate. The BCP lithography fabrication of patterned graphene can enable a continuous semiconducting graphene thin film for flexible electronics, nanoelectronics, and optoelectronics applications.[18]

## 2. Methods

***2.1. Synthesis of Large Scale Graphene.*** Graphene was synthesized using thermal chemical vapor deposition (CVD) of methane ($CH_4$) at 1,000°C. An SLG material was purchased from ACS Material, USA. A thin Cu foil (25 μm thickness) was purchased from Alfa-AESAR, USA and cut in 20 mm × 13 mm sized sheets and annealed at 1,000°C for 1 h in an inert gas atmosphere followed by hot acid treatment and cleaning. After that, the metal foil was placed inside a thermal CVD system and the temperature was increased up to 1,000°C with a heating rate of 120°C $min^{-1}$. The atmosphere of the CVD furnace was maintained at 0.8 atmospheric pressure in the presence of an inert gas (Ar) and $CH_4$:$H_2$ (1:4) was used as a precursor gas mixture for graphene growth. Before graphene on Cu was transferred to a substrate, the back of the graphene was removed by oxygen plasma. The top side of graphene was protected by a poly(methyl methacrylate) (PMMA) layer during the $O_2$ plasma etching. The graphene film was then transferred onto a 300 nm $SiO_2$-coated Si substrate ($Si/SiO_2$) using a chemical process. The chemical process for graphene transfer consists of the etching of the Cu foil and then transferring the floating graphene onto a $Si/SiO_2$ substrate, followed by washing with water, acetone, and isopropyl alcohol as described elsewhere.[19] After that, the PMMA layer was removed by dissolving it in acetone. Furthermore, the rapid thermal annealing was carried out for graphene on the $Si/SiO_2$ substrate at 400°C under an $N_2$ atmosphere to remove the residual PMMA and promote the adhesion between graphene and the oxide layer.

***2.2. DBCP Film Fabrication.*** The patterned structure was made by the Di-BCP (DBCP) self-assembly. Poly(styrene-*b*-4-vinylpyridine) (PS-*b*-P4VP) (number-average molecular weight, $M_{n,PS} = 41.5$ kg/mol, $M_{n,P4VP} = 17.5$ kg/mol, $Mw/Mn = 1.07$, where $Mw$ is the average molecular weight) was purchased from the Polymer Source (Montreal, Canada) and used without further purification. A 20-nm-thick silicon oxide film was deposited onto graphene as the protecting layer and also

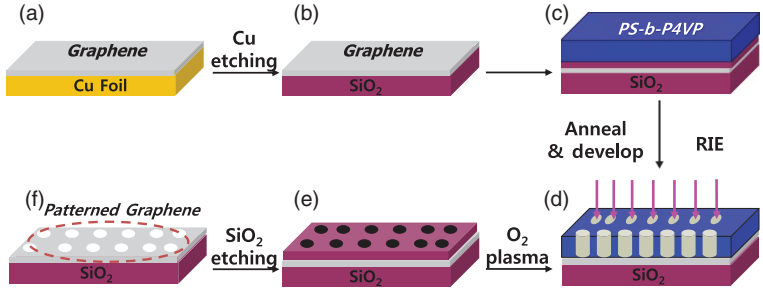


Figure 1. Schematic illustration of NPG fabrication. (a) CVD grown graphene on Cu foil, used as a starting material of the nanopatterning process. (b) After Cu was etched by using 1M $FeCl_3$, the graphene is transferred onto a $SiO_2$/Si substrate (Si layer is not shown). (c) A thin layer of $SiO_2$ is deposited on graphene, followed by spin-coating of the BCP PS-b-P4VP on top of the sample. (d) The PS-b-P4VP BCP film is annealed and developed, leaving the porous nanopatterned PS matrix as the template for further patterning. (e) Fluoride-based RIE penetrates the oxide layer, partially degrade the PS film, and form the $SiO_2$ hard mask. (f) Graphene in the exposed area is etched away by $O_2$ plasma and then $SiO_2$ layer is removed. Finally, porous graphene on $SiO_2$ is obtained.

as the grafting substrate for the subsequent BCP nanopatterning. Then, 0.5 wt.% PS-*b*-P4VPcopolymer solution dissolved in toluene was spin-coated at 2,000 rpm for 60 s on the substrate. This film was then exposed to tetrahydrofuran vapor in a closed glass vessel for 3 h to induce mobility and allow phase separation to occur. The film was then immersed in pure ethanol for the poly(4-vinylpyridine) (P4VP) phase to swell, thus leading to a porous structure. The PS-*b*-P4VP BCP thin film with cylindrical domains normal to the surface was then fabricated and used as the etching template, and a reactive-ion etching (RIE) process is used to punch holes into the graphene layer.

***2.3. Formation of the Porous Graphene.*** For efficient nanopatterning, two consecutive RIE processes were applied. As a shallow depth hole generation in graphene, no additional deposition to enhance RIE resistance was applied prior to the RIE process. The first RIE etching was for P4VP residual layer removal located at the bottom of the holes. RIE process parameters were empirically determined by using $CF_4$ gas (Oxford Plasmalab 80 RIE) and optimized at 50 mTorr under 65 W, plasma power for 30 s. The latter was to create shallow prepatterns on $SiO_2$ thin film exposed to air formed at the previous RIE step and optimized at 40 mTorr under 200 W with $CHF_3$ and Ar gases. An $O_2$ plasma process was then used to remove the remaining copolymer. $CHF_3$ and Ar plasma was then used to punch holes into the evaporated $SiO_2$ to expose the underlying graphene layer. Additional $O_2$ plasma was used to completely etch away an exposed region of graphene.

***2.4. Characterization.*** The sample microstructure was characterized by ultra-high resolution scanning electron microscopy (UHR SEM; FEI XL30). Raman spectroscopy was used as a nondestructive tool for probing the edge structure and the crystallinity of $sp^2$-bonded graphene.[20] Raman spectra were collected using a Renishaw Raman spectrometer inbuilt with $Ar^+$ laser of wavelength of 514 nm for quantifying the degree of structural order and charge-transfer characteristics.

**3. Results and Discussion** Figure 1 illustrates the present approach for fabricating NPG. For initial demonstrations, the CVD grown graphene layer on Cu foil was used as the starting material. After the Cu substrate was etched away by 1M $FeCl_3$, the floating graphene in the solution was transferred onto $SiO_2$-coated Si substrate. A 20-nm thick silicon oxide film was first evaporated onto graphene as a protecting layer and also as the grafting substrate for the subsequent BCP nanopatterning. The PS-*b*-P4VP BCP film with cylindrical domains normal to the surface was then fabricated and used as the etching template, and a $CHF_{3-}$ based RIE process followed by the oxygen plasma etch that was employed to punch holes into the graphene layer. We present here the first experimental study on SLG and FLG FETs structures nanopatterned by using a facile, PS-*b*-P4VP-based BCP approach.

Raman spectroscopy was used as a nondestructive tool for probing the edge structure and the crystallinity of $sp^2$-bonded graphene. Figure 2 demonstrates the Raman spectra of pristine graphene, and NPG. The Raman data were taken from different spots on graphene. Prior to patterning, the G (~1,580 $cm^{-1}$) and 2D (~2,680–2,700 $cm^{-1}$) bands were prominent. Raman spectroscopy can also be used to determine the number of layers of multilayer graphene and to discriminate between the single and the few layers using the intensity ratios of the G band and the 2D band. For an SLG, $I_G/I_{2D}$ intensity ratio is ~0.24 which increases with the number of graphene layers thus making it possible to estimate the thickness of graphene layers.[21,22] In this regard, it is well known that the $I_G/I_{2D}$ ratio increases up to six to eight layers.

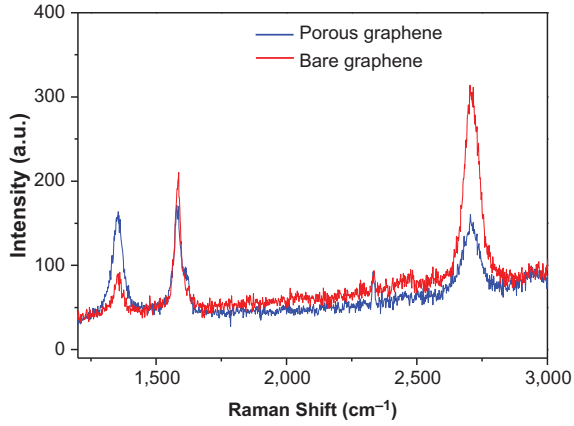


Figure 2. Comparison of Raman spectra of pristine and NPG with their characteristic D, G, and 2D bands at the respective positions.

In order to measure the actual thickness of the graphene sample and obtain the number of layers, sensitive metrology techniques such as AFM analysis or a high resolution TEM technique may be utilized. Figure 2 shows that the ratio of $I_G/I_{2D}$ in our graphene is around 0.7 and therefore it is estimated that there are four to seven layers of graphene.[22] In addition to the differences in the $I_G/I_{2D}$ ratio, the full width half maxima (FWHM) of 2D band also increases as the graphene thickness increases.[23] The shape of the 2D mode evolves significantly with the number of layers. The 2D band becomes broader when the graphene thickness increases from an SLG to the multilayer graphene. As the 2D band originates from a two phonon double resonance process, it is closely related to the band structure of graphene layers.

Ferrari et al. [24] have successfully used the splitting of the electronic band structure of multilayer graphene to explain the broadening of the 2D band. For mono- and bi-layer graphene, the FWHM of the 2D band is ~30 [25] and for the FLG according to our data, is ~63.24. It is believed that the 2D peak broadening can be attributed to the number of layer increases in the graphene structure.[26] The D peak at ~1,330 cm$^{-1}$ is related to defects and disorder. This is forbidden in perfect graphitic systems, and requires a defect for its activation, and so is observed at the edges of graphene samples.[27,28] The integrated intensity ratio of the D band and G band ($I_D/I_G$) is a parameter sensitive to the defect density.[29,30] In Figure 2, the high D peak was observed on porous graphene, which suggests that defects in our samples are significantly and mostly formed by nanopatterning. After nanopatterning, there is a systematic upshift in the position of the G band. The G-band position for porous graphene was observed at ~1,586 cm$^{-1}$, which can be compared with the G position of pristine graphene (~1,580 cm$^{-1}$). This upshift in the G-band position further confirms the hole-doping in the NPG by the formation of oxygen dangling bonds with graphene as reported earlier.[31] We also note that there is an increase in the intensity ratio of the $I_G/I_{2D}$ with more defects. The increase in $I_G/I_{2D}$ in NPG is likely due to the alteration of its electronic transformation from semi-metallic to semiconducting with a successive opening of the band gap.[32,33] The detailed explanation of the change in the electronic structure of NPG by a band-gap opening is discussed in the latter section of this manuscript.

Figure 3 shows the image of the steps of nanopores fabrication on graphene. Scanning electron microscope (SEM) image of the annealed BCP film on graphene shows the hexagonal-packed P4VP domains in the PS matrix. The sample was immersed into ethanol for 20 min to develop the porous structure (Figure 3(a)). The domain center-to-center distance is approximately 48.3 nm ±2.7 nm by using PS-*b*-P4VP with the number-average molecular weight, $M_{n,PS}$ = 41.5 kg mol$^{-1}$, $M_{n,P4VP}$ = 17.5 kg mol$^{-1}$. Changing the molecular weight while keeping the volume ratio constant can result in vertical aligned domains with a variable center-to-center distance. We used RIE in order to remove P4VP domains, which causes a porous structure of the PS matrix with hexagonally arranged nanoholes vertically penetrating through the film as shown in Figure 3(a).

The following etching process begins to drill holes into the underlying $SiO_2$ layer, leaving a $SiO_2$ nanomesh that can serve as the mask for subsequent oxygen plasma etch to form porous graphene (Figure 3(b)). The oxide mask can be easily removed by dipping the sample into the etching solution for a short period of time and the NPG structure can be seen under SEM. Figure 3(c) shows the SEM images of a porous graphene with an average neck width ($w$) of ca. 19.1 nm, but a neck width as small as 5.6 nm was also observed. Furthermore, it is possible to tune the mesh periodicity by using a BCP of different molecular weight.[34] By applying longer etching time to remove the grapheme, the neck width can be further reduced in order to create the quantum confinement effect and open up an effective bandgap.[11,35,36] While the pore diameter and inter pore distances can be controlled by the co-polymer molecular weight and the ratio of the components, other parameters such as the degree of etching affects the sizes and interdistances of the nanomesh or nanopore structures so as to alter the average ribbon or neck width, which in turn influences the electronic bandgap of NPG as it inversely scales with the ribbon width.[11,36–40]

As the neck width represents the smallest dimension that controls charge transport through the system, we have carried out a statistical analysis of the neck widths (Figure 4) of the NPG obtained after $SiO_2$ etching (Figure 3(c)). It is noted from Figure 3 that the nanopatterned polymer structures are slightly deformed, presumably due to the generally soft nature of the polymer

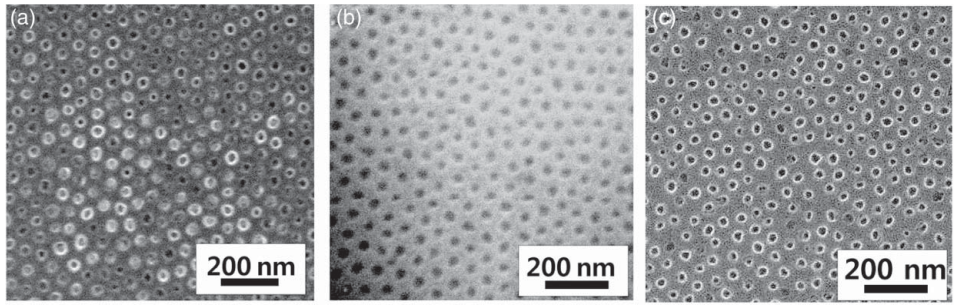


Figure 3. Images illustrating the steps of the PS-*b*-P4VP-based nanopatterened graphene fabrication process. (a) SEM image of the annealed BCP film on graphene, showing hexagonal-packed P4VP domains in the PS matrix. The sample was immersed into ethanol for 20 min to develop the porous structure. (b) SEM image of the $SiO_2$ mask after RIE with the PS mask. (c) SEM image of the NPG surface after removing the top $SiO_2$ mask (high magnification). The pores have 29.14 nm ±2.54 nm diameters and 19.16 nm ±2.25 nm neck widths after removing the top $SiO_2$ mesh mask.

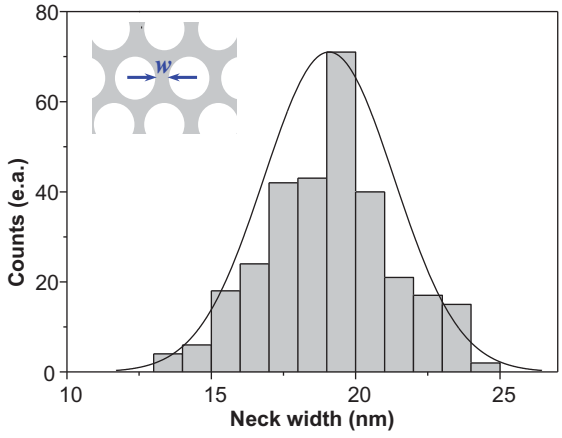


Figure 4. Histogram of the neck width after the PS-*b*-P4VP-based nanofabrication. This plot shows a distribution of graphene neck width in the NPG of with average neck widths of 19.162 nm (SD ±2.250 nm).

materials. Such defects could be minimized with a more careful control of process parameters.

The histogram plot (Figure 4) resulting from the statistical analysis shows that the NPGs exhibit an average neck width of 19.1 nm and the standard deviation of the neck width is found to be less than 3 nm. However, it should be mentioned that our BCP assembly process is not yet optimized to the best it can offer, and hence it is possible that our future optimized BCP self-assembly structure can lead to a more uniform porous graphene, as well as a further reduced neck width. It is envisioned that a pore-widening process, such as utilizing a controlled oxygen plasma etch, could be utilized, which can lead to a substantially reduced neck width and associated interesting change in the degree of bandgap opening. These SEM studies together with previous studies [41,42] clearly demonstrate that reasonably highly uniform porous graphene can be obtained with controllable periodicities and neck widths by using the BCP nanolithography.

Figure 5 displays the electrical characteristics of FETs in NPG at room temperature. Figure 5(a) schematically illustrates the structure of the patterened graphene FET device, in which a rectangular-shaped patterened graphene having a neck width $w$, total 300 μm of channel width $W$, and 10 μm of channel length $L$serves as the conduction channel. A pair of Ti/Au metallic pads (with a thickness of 26 nm Au/4 nm Ti) serves as a drain and source contact. A 275-nm thermal oxide $SiO_2$ layer and degenerated ($p^{++}$)Si wafer are used as the gate dielectric and the back gate, respectively. Figure 5(c) and 5(d) show the electrical transport characteristics of a typical patterned graphene transistor with an average neck width of ~19 nm. Drain current ($I_d$) versus gate voltage ($V_g$) characteristics for the transistor show a typical p-channel transistor behavior (Figure 5(c) and 5(d)). The increase in p-doping is likely due to the increase in oxygen plasma exposure, resulting in dangling bonds on the edges of the holes.[35] Most of the devices were fabricated using a buffer layer process, the unintentional severe doping by $CHF_3$ RIE processes was observed as reported in other studies.[35] However, the hole-doping observed in the NPG is similar to that of GNR devices, and can be attributed to edge oxidation in the $O_2$ plasma process or physisorbed oxygen from the ambient and other species during the nanofabrication process.

In Figure 5(c), this NP FLG transistor exhibits a typical ambipolar transport behavior with the minimum drain current ($I_{off}$) at the neutral point ($V_g = V_0$) and a relative low on/off current ratio ($I_{on}/I_{off} \sim 1.5$ measured).The ability to control the NPG periodicity and neck width is very important for controlling their electronic properties because charge transport properties are highly dependent on the width of the critical current pathway. In the case of GNRs, both theoretical and experimental works have shown that the size of the electronic bandgap is inversely proportional to the ribbon width.[37,43,44] For the estimation of approximate bandgap, the NPG can be viewed as a highly interconnected network of GNRs. Therefore, we expect that the electronic bandgap

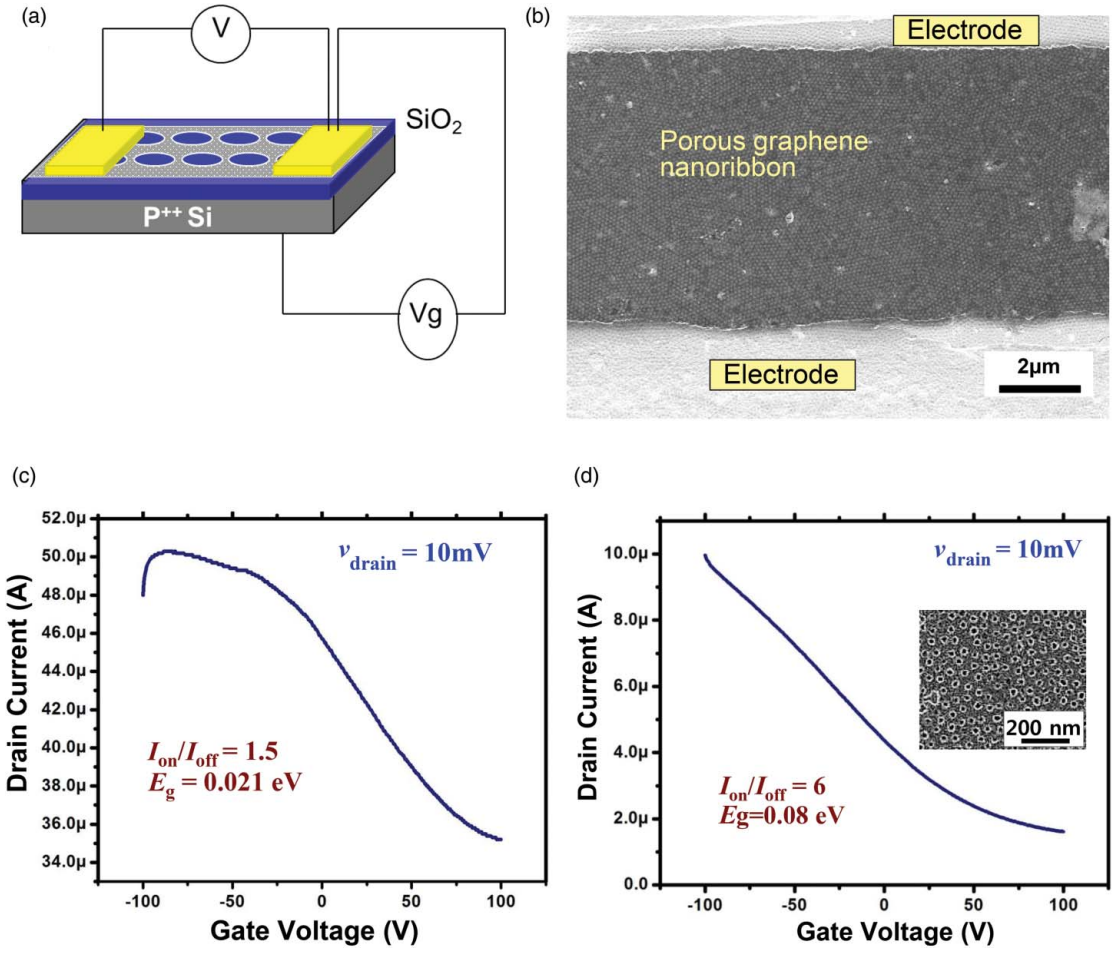


Figure 5. Electrical properties of NPG using the PS-*b*-P4VP-based process. (a) Schematic illustration of the FET device fabricated using the NPG. (b) SEM image showing the top-view of the nanopatterned FLG-based FET device. (c) Drain current ($I_d$) versus gate voltage ($V_g$) for a FET device of NP FLG. (The electronic measurement was carried out in ambient conditions at room temperature). (d) Drain current ($I_d$) versus gate voltage ($V_g$) for a device and the inset shows the SEM image of NP SLG.

of NPG inversely scales with the average ribbon width (i.e., $E_g \sim \alpha/w$, and $\alpha$ is a coefficient with 0.95 nm eV for nanomesh).[36,45] Furthermore, the on/off current ratio of an FET device exponentially scales with the bandgap (i.e., $(I_{on}/I_{off} \approx \exp(E_g/kT)$, where $k$ is Boltzmann constant and $T$ is the absolute temperature).[46] So the $I_{on}/I_{off}$ value of the NPG transistor is expected to inversely scale with the average neck width, as expressed in Equation (1), where $C$ is a dimensionless constant. Equation (1) can be simplified to Equation (2) related to bandgap energy.

$$\frac{I_{on}}{I_{off}} \approx e^{\alpha/kTw} = Ce^{\alpha/kTw}, \quad (1)$$

$$E_g = kT\left[\ln\left(\frac{I_{on}}{I_{off}}\right) - \ln(C)\right]. \quad (2)$$

The expected bandgap from the relation of $E_g \sim \alpha/w$ by the averaged neck width of ~19 nm was 0.05 eV. In Figure 5(c), however the estimated value is 0.021 eV from Equation (2) with measured $I_{on}/I_{off}$ of 1.5. There is a difference between the calculated values from the relations with neck width by the averaged neck width of ~19 nm and with an on/off current ratio measured. Although this equation does not take into account the entire complex physics occurring in nanostructured graphene, it is still appropriate as it seems to have a reasonable match with experimental data for various NPG structures.[47]

While extensive studies have been carried out on the physical properties of SLG, less is known about the electrical properties of FLG structures. We find that the electrical properties in graphene nanoscale transistors are strongly affected by the number of graphene layers, the channel width, and the trapped charge in the $SiO_2$ substrate, consistent with the findings by Lin and Avouris [48] and Sui and Appenzeller [49]. Their work presented the scaling effect of the graphene thickness on device performance and proposed a resistor network model describing the coupling between graphene layers, including the impact of interlayer screening. They showed the $I_{on}/I_{off}$ ratio of the FLG FET with respect to the graphene

thickness. The $I_{on}/I_{off}$ ratio indicates thickness$^{-1}$ dependence and reaches unity at around 10 layers of graphene. As apparent from their work, $I_{off}$ increased slowly with graphene thickness while $I_{on}$ decreased with thickness. Thus, the $I_{on}/I_{off}$ ratio decreased rapidly with increasing thickness of graphene and approaches unity at or around 10 layers of graphene. This is the combined effect of the Coulomb interaction and the interlayer coupling that are responsible for the particular thickness dependence of the $I_{on}$, $I_{off}$, and the on-off ratio for the FLG FETs.

For single-layer NPG (Figure 5(d)), the device is fabricated with the same process and structure as for the NP FLG device. SLG device also exhibits an ambipolar transport behavior and has a much higher on/off current ratio ($I_{on}/I_{off} = 6$ measured) compared to the control NP FLG transistor. Obviously, both screening and interlayer coupling is able to be considered to account for our experimental findings of the $I_{on}/I_{off}$ dependence on the numbers of graphene layers. Further studies are needed to fully understand the interaction between the graphene layers and how the stacking sequence affects the topology of the $\pi$ bands as well as an electronic transition from two-dimensional (2D) to the bulk (3D) character when going from one layer to multilayer graphene. There are six consecutive current on/off ratio values achieved with the same or a little higher values than those for the previously reported FET devices of GNRs and GNMs.[11,36–40] In NP SLG FET, the calculated bandgap is 0.08 eV by Equation (2) and it roughly corresponds to an expected value based on previous research.

Figure 5(d) demonstrates an $I_D - V_g$ plot for the NPG devices with ~19 nm average neck width, with the calculated mobility of 14 $cm^2/(V \cdot s)$, which is substantially lower than that of pristine graphene. Prior to patterning, pristine CVD graphene FET devices showed a hole mobility of 500–1,000 $cm^2/(V \cdot s)$, which is typical for CVD grown graphene.[50] We calculated the hole mobility ($\mu$) of the fabricated FETs using a standard transistor model as shown in Equation (3), where $d_{ox}$ is the thickness of the gate oxide, $\varepsilon_{ox}$ is the permittivity of silicon dioxide, $L$ is the channel length, and $W$ is the channel width.

$$\mu = \frac{d_{ox}}{\varepsilon_{ox}} \frac{L}{W} \frac{1}{V_d} \frac{dI_d}{dV_g}. \quad (3)$$

The RIE process is known to degrade the mobility of NPG. Moreover, because of the inherent crystal grain boundaries present in the CVD grown graphene layer as well as variations in growth directions along the crystal lattice of the catalytic metal substrate, the mobility of CVD grown graphene is typically one to two orders of magnitude lower than that of the mechanically exfoliated grapheme.[50,51] We also observed that the grain boundaries in CVD grown graphene are essentially retained in the lattice of patterned graphene, possibly contributing to significant mobility degradation. More importantly, the mobility of NPG is limited by charge carrier scattering caused by several possible factors which include line edge roughness, interior defects, disordered edges, ionized impurities and acoustic and optical phonons.[52,53]

**4. Conclusions** We have successfully fabricated and characterized NPG with an average neck width of ~19 nm. This semiconducting graphene structure was fabricated for the first time using PS-*b*-P4VP BCP, which is more facile and convenient than other BCPs as the use of the cumbersome buffer layer is eliminated. We also presented the first experimental study on current distribution in not only SLG based, but also multilayer NPG-based FETs. The NPG allowed experimental confirmation of the relationship between electrical conductance and the bandgap. Electrical characterization of NPG devices confirmed that the current on/off ratio is inversely proportional to the neck width, indicating the formation of an effective gap due to the confinement effect. We showed a dependence of the $I_{on}/I_{off}$ ratio on thickness, which is explained in terms of the interlayer coupling. From these comprehensive studies, we have shown that both electronic transport and Raman characteristics change in a concerted manner as graphene patterning is applied. The availability of such NPG fabricated by a facile PS-*b*-P4VP approach will provide an interesting opportunity for fundamental investigation of transport behavior in the highly interconnected graphene network, and will enable exciting application opportunities in sensitive biosensors and a new generation of devices. The new and simpler nanofabrication process, using the PS-*b*-P4VP route is scalable, by which BCP lithography can be implemented and scaled to large-area graphene layers by either the convenient solvent annealing phase separation process or the thermal phase separation method. The effective controllability of processes and nanostructuring could be utilized for control of the electronic properties of graphene, which could enable practical, large-area, manufacturable applications of graphene in thin film electronics, flexible electronics, optoelectronics, and sensors.

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