IOP PUBLISHING NANOTECHNOLOGY

Nanotechnology 21 (2010) 065502 (11pp)

doi:10.1088/0957-4484/21/6/065502

Nanopores in solid-state membranes engineered for single molecule detection

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Received 19 August 2009, in final form 9 November 2009 Published 11 January 2010 Online at stacks.iop.org/Nano/21/065502

Abstract

A nanopore is an analytical tool with single molecule sensitivity. For detection, a nanopore relies on the electrical signal that develops when a molecule translocates through it. However, the detection sensitivity can be adversely affected by noise and the frequency response. Here, we report measurements of the frequency and noise performance of nanopores ≤ 8 nm in diameter in membranes compatible with semiconductor processing. We find that both the high frequency and noise performance are compromised by parasitic capacitances. From the frequency response we extract the parameters of lumped element models motivated by the physical structure that elucidates the parasitics, and then we explore four strategies for improving the electrical performance. We reduce the parasitic membrane capacitances using: (1) thick Si₃N₄ membranes; (2) miniaturized composite membranes consisting of Si₃N₄ and polyimide; (3) miniaturized membranes formed from metal-oxide-semiconductor (MOS) capacitors; and (4) capacitance compensation through external circuitry, which has been used successfully for patch clamping. While capacitance compensation provides a vast improvement in the high frequency performance, mitigation of the parasitic capacitance through miniaturization offers the most promising route to high fidelity electrical discrimination of single molecules.

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(Some figures in this article are in colour only in the electronic version)

1. Introduction

A nanopore is an analytical tool with single molecule sensitivity [1]. It operates in a way that is reminiscent of Coulter's original idea of using dielectric objects within a constricted current path to alter the electrical resistance [2]. A nanopore relies on the electrical signal that develops when a single molecule immersed in electrolyte translocates across a membrane through a pore. Ions passing through the pore are forced into contact with that portion of the molecule in the constriction. At low bias, the electric potential of the molecule presents an energy barrier to the passage of ions. Because the passage rate is exponentially related to the height of the barrier, differences in the heights for different molecules have a substantial effect on the current-voltage characteristic. If each molecule has a characteristic signature, then ostensibly a pore could be used to electrically read-out the chemical constituency of an unknown sample.

One compelling application is sequencing DNA with a nanopore [1]. Both the promise and limitations associated with a nanopore sensor used for sequencing double-strand λ -DNA (dsDNA) are illustrated in figure 1. Figure 1(a) shows a 2.2 \pm 0.2 nm diameter pore—smaller than the double helix [3] sputtered through a silicon nitride membrane approximately 15 nm thick. In normal operation, the thin membrane with a nanopore through it separates two chambers, each filled with electrolyte. When a bias is applied across the membrane, a corresponding electrolytic current, $I_0 \sim 3.3$ nA, flows through the 2.2 nm diameter pore. The driving bias causes a charged molecule in the vicinity to migrate towards the pore and eventually it is captured by the field and pulled into the pore as illustrated in figure 1(b). When a molecule enters the pore, there is an electrical signal, e.g. the ionic current through the pore changes drastically. The effective cross-sectional area of the pore that is open to the ionic current changes due to the charge and the excluded volume that ions could previously

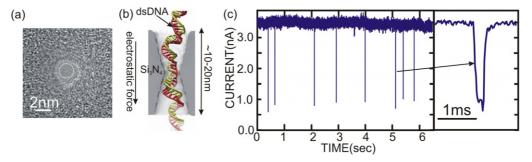


Figure 1. Nanopore in thin membrane used for single molecule detection. (a) A TEM image of a pore with a diameter of 2.2 ± 0.2 nm in a 15 nm thick Si₃N₄ membrane. (b) A schematic representation of a cross-section through a 2 nm nanopore in a silicon nitride membrane showing a double-stranded DNA in the pore. (c) A measurement of the electrolytic current through the 2.2 nm pore interacting with a λ-DNA in 100 mM KCl with 1.0 V applied across the silicon nitride membrane. The current blockades are observed as λ-DNA translocates through the pore with $\Delta I/I_0 > 0.78$. The figure on the right is an expanded view of one blockade.

travel through. So, for example, when λ -DNA translocates through the pore of figure 1(a), the current through the pore is reduced, resulting in a temporary blockade of the current, $\Delta I/I_0 = 0.78 \pm 0.08$, like that illustrated in figure 1(c).

We expect the largest blockade signal for the smallest pore diameter consistent with the size of the molecule. A solid-state nanopore offers an advantage over its proteinaceous counterparts [4] in that the geometry of the pore can, in principle, be sculpted with sub-nanometer precision. While it can be more sensitive than a proteinaceous pore or even a nanowire, one shortcoming of a nanopore sensor is the response time measured by the diffusion equivalent capacitance [5]. The diffusion capacitance governs the time required to capture a molecule [6]—about 1 s in figure 1(c) and leads to a trade-off between response time and the detectable concentration [5]. However, the main performance limitation associated with nanopore detection is fidelity of the electrical signal used to discriminate between molecules relative to the noise. And the noise is inextricably linked to the bandwidth of the nanopore and therefore to the throughput through the translocation velocity [7–11].

Seeking a compromise between signal-to-noise and bandwidth, Smeets et al [9, 10] analyzed the electrical characteristics of solid-state nanopores > 10 nm in diameter, representing them by an equivalent lumped element circuit consisting of a resistance associated with the pore, $R_{\rm p}$, in parallel with an effective capacitance, $C_{\rm m}$, associated with the electrolyte contact to the chip, and a series resistance, $R_{\rm el}$, associated predominately with the electrolyte. Without really addressing the frequency response of the pore current [8], they discovered that the capacitance is a key feature affecting the current noise performance at high frequency [9]. However, both the high frequency and noise performance of the pore current are critical for applications like sequencing because the translocation velocity of the DNA is so high in a solidstate nanopore, exceeding 1 bp/10 ns [11]. According to the model of Smeets et al [9], the frequency response is essentially determined by the product of $C_{\rm m}$ and $R_{\rm el}$, so that $R_{\rm el}C_{\rm m} > 1$ -10 μ s for the 2.2 nm pore in a 15 nm thick nitride membrane in 100 mM KCl, corresponding to a bandwidth of $\Delta f =$ $1/2\pi R_{\rm el}C_{\rm m} \sim 100$ kHz. Thus, if the translocation velocity is high, it becomes difficult to resolve that portion of the blockade associated with a single base; >16 MHz bandwidth would be required. More gain cannot resolve this problem due to the concomitant increase in electrical noise.

Here we report measurements of the high frequency and noise performance of nanopores 2-7.5 nm in diameter comparable to the size of the hydrated DNA double helix (~2.6-2.9 nm in diameter) in solid-state membranes compatible with semiconductor processing. frequency response we extract the parameters of a small signal model, motivated by the physical structure, which represents the nanopore as a distributed circuit comprised of several lumped elements associated with: the semiconductor handle wafer; the various dielectric layers comprising the membrane; the electrolytic double layer; and the electrolyte. We find that measurements of the frequency and noise performance can generally be captured using this lumped element model consisting of three high-pass filters in parallel with the pore resistance. We find that both the high frequency and noise performance are compromised by parasitic capacitances associated primarily with the handle wafer. Illuminated by the model, we then explore four strategies for improving the electrical performance by reducing the parasitic membrane capacitances: (1) increasing the thickness of Si₃N₄ membranes; (2) miniaturizing composite membranes consisting of Si₃N₄ and polyimide; (3) miniaturizing membranes formed from metal-oxide-semiconductor (MOS) capacitors; and finally, (4) compensating for the capacitance through external circuitry, which has been used successfully for patch clamping. While capacitance compensation provides a vast improvement in the frequency response, the external circuitry introduces noise. On the other hand, mitigation of the parasitic capacitance through miniaturization offers the most promising route to high fidelity electrical discrimination of single molecules.

2. Experimental details

Following several innovations in the fabrication of nanopores in solid-state membranes [13–16], we have developed the two process flows delineated in figures 2(a)–(f): one for fabricating pores in nitride membranes and another for creating pores

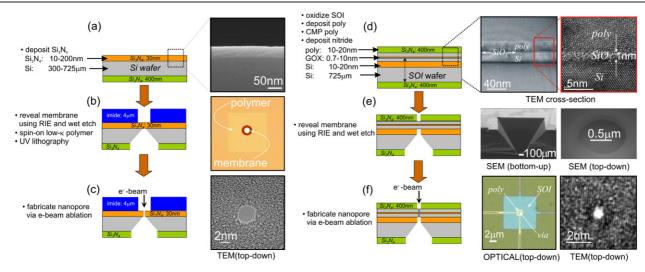


Figure 2. Processing flow to produce membranes. (a) Membranes are formed by depositing a Si_3N_4 layer onto a silicon substrate. A TEM cross-section through the membrane structure is shown on the right. (b) DUV lithography and a combination of dry and wet etching through the backside of the wafer reveal the membrane. Subsequently, a photosensitive polyimide layer on the front surface is deposited and patterned to reduce the stray capacitance. An optical micrograph of a $10~\mu m$ window in polyimide used to define the membrane area is shown on the right. (c) After revealing the membrane, a pore is sputtered in it using a tightly focused, high energy electron beam. A nanopore through the membrane is shown on the right. (d) MOS membranes are formed by depositing a gate oxide and polysilicon layer (PSY) onto a thinned silicon-on-insulator (SOI) substrate with a thick buried oxide layer (BOX). A TEM cross-section through the membrane structure is shown on the right of (d). Using DUV lithography and a combination of wet and dry etching, a membrane is revealed as illustrated in (e). Two scanning electron micrographs: one from the bottom up (left) shows the through-wafer via; and the other from the top-down (right) shows the capacitor membrane. After revealing the membrane, a pore is produced using electron beam sputtering (f). An optical micrograph of the finished capacitor defined by the poly (left) showing the leads used to measure the capacitor voltage and a TEM micrograph of a \sim 0.7 nm diameter pore (right) through the membrane capacitor.

in membranes formed from MOS capacitors. The silicon nitride membranes shown in figures 2(a)-(c) are fabricated by depositing an LPCVD Si₃N₄ film ranging from 30 to 200 nm thick (nominally) on the top of a 300 μ m thick (unintentionally doped, \sim 10–15 Ω cm) Si handle wafer. A wet chemical etch (tetramethylammonium hydroxide-TMAH) starting from the backside of the wafer etches Si anisotropically along the 110 direction, as indicated in figure 2(b), preferentially removing the Si handle wafer under the Si₃N₄ film and eventually revealing an area ranging from 15 μ m \times 15 μ m to 500 μ m \times $500 \mu m$. To reduce the thickness, either the nitride membrane is sputtered in a 5 μ m \times 5 μ m area using focused ion beam milling or it is uniformly etched in 20:1 H₂O:49%HF for 30-40 min at room temperature. Afterward, a polyimide photoresist (HD8820, HD MicroSystems) with a thickness of $3.6 \pm 0.6 \,\mu \text{m}$ is spin deposited on top of the chip as shown in figure 2(b), and a 5–10 μ m window is then opened over the membrane using UV lithography.

We have also developed a process to produce nanometer diameter pores in membranes formed from an ultra-thin MOS capacitor, as illustrated in figures 2(d)–(f). We have produced MOS capacitor membranes 40–50 nm thick, $\geqslant 2~\mu m \times 2~\mu m$ in area with >0.7 nm diameter pores in them. As illustrated in figure 2(d), a membrane is formed on an SOI (siliconon-insulator) substrate using conventional silicon processing technology. The electrodes of the capacitor are fabricated from heavily doped layers of silicon, appropriately thinned using a combination of oxidation and CMP (chemical–mechanical polishing). The capacitor dielectric is formed by growing an

oxide on crystalline silicon using rapid thermal oxidation at \sim 1000 °C. The thickness of the SiO₂ insulator separating the electrodes of the capacitor is a crucial specification. As shown in figure 2(d), we are using oxides ranging from 1 to 5 nm thick. We use deep-ultra-violet (DUV) lithography in conjunction with reactive ion and wet chemical etching to define the size of the capacitor. Subsequently, the membrane is revealed using a through-wafer etch. The via associated with the through-wafer etch is shown in figure 2(e). This via, in combination with the thickness of the wafer, determines the 1 mm² size of chip. A top view of the membrane revealed through a 1 μ m window in the sacrificial nitride is shown on the right in figure 2(e); a larger optical micrograph from the same perspective is shown in figure 2(f). The MOS capacitor membrane defined by DUV lithography is as small as 2 μ m × 2 μ m, corresponding to a measured capacitance of \sim 210 fF. After the membranes are formed, a narrow via is milled in the 1 μ m window using a focused ion beam, and then a pore is sputtered using a tightly focused, high energy electron

After a 15 s O_2 plasma clean, the membrane thickness is measured *in situ* (nondestructively) using electron energy loss spectroscopy (EELS), and then a nanometer-size pore is sputtered in it using a tightly focused (1.6 nm spot-size) 9° α (cone angle), high energy (200 kV) electron beam emanating from a JEOL 2010F transmission electron microscope (TEM) operating in convergent beam diffraction mode, biased at 170 μ A emission current, using a 150 μ m condenser aperture. The beam current is typically >0.5 nA. The sputtering time

is typically about ~ 30 s for a 15 nm nitride membrane and ~ 10 min for a MOS capacitor. Using TEM images taken at different tilt angles, we model the pore geometry as two intersecting cones (bi-conical) each with a $> 20^{\circ}$ cone angle [13].

A membrane with a nanopore in it is then mounted in a custom-made two-chamber acrylic holder. Silicone Orings are used to seal the chip into the holder between the two chambers, leaving the nanopore as the only connection between the two chambers. The cis chamber has a volume of 100 μ l; the *trans* chamber has a volume of approximately 13 ml. Voltage is applied and the DC, AC, current response, and noise characteristics of the nanopore are measured in buffered KCl solution at 23 \pm 1 °C using Ag/AgCl electrodes (Warner) in each chamber. The frequency response of nanopores is obtained with a Signal Recovery 7280 lock-in amplifier. A small AC voltage signal (50 mV-rms amplitude) at various frequencies is applied to the cis chamber, and the inphase and out-of-phase components of the membrane current are measured by a phase-sensitive lock-in technique. The frequency response is then fitted to a physical lumped element model using Advanced Design System (ADS) software.

To measure the step response at the Ag/AgCl electrodes and at the MOS capacitor electrodes we used a digitizing oscilloscope along with a high input impedance (1 $M\Omega$ and 6 pF, including stray capacitances) voltage pre-amplifier head stage attached to the respective electrodes to eliminate cable capacitance. A pulse generator with a 10 ns risetime (Agilent 6321) was used to apply a voltage step from 1 to 0 V, which triggered the oscilloscope trace.

Finally, we also used the Axopatch 200B low noise amplifier in whole cell configuration ($\beta=1$) to characterize the noise of the nanopore-membrane mechanism. The full bandwidth of the amplifier was used, but before the signal was digitally sampled at 250 ksamples s⁻¹, it was passed through a four-pole low-pass Bessel Filter with a cutoff frequency of 100 kHz. All noise spectra are taken at 100 mV voltage applied across the membrane with all the capacitance and transient compensation circuitry off. For each pore 16 traces, each lasting \sim 4 s, were recorded, the noise power spectrum of each trace was computed (using PClamp 9.2 software), and the average of the 16 power spectra was reported here.

3. Results and discussion

We measured the current frequency response, the transient response to a voltage step, and the noise performance of the nanopore-membrane structures and used them to create and test a comprehensive, small signal model derived from the physical structure. Such a model is indispensable for optimizing signal detection and analyzing noise sources as it can be used to elucidate strategies for improving the signal-to-noise related changes in the pore-membrane structure. The membrane voltage represents a crucial test of the models because it determines the electric field in the pore, which affects the translocation kinetics as well as the potential barrier associated with the molecule in the constriction and therefore the blockade current.

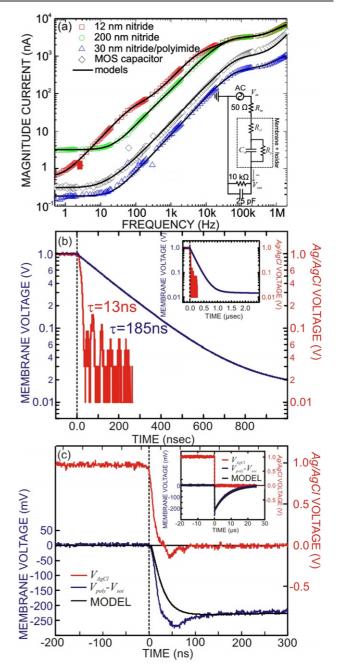


Figure 3. (a) Magnitude of the pore current as a function of frequency measured in 1 M KCl through four different membranes: one with a nitride layer about 12 nm thick with a $3.3 \times 4.8 \pm 0.2$ nm pore, another with a 200 nm thick nitride layer with a $3.0 \times 3.8 \pm 0.2$ nm pore, the third with a 30 nm thick nitride layer with a $1.7 \times 2.8 \pm 0.2$ nm pore and polyimide coating, and the fourth one with the MOS structure with a $7.1 \times 7.3 \pm 0.3$ nm pore; the corresponding fits to the data (solid lines) are also shown. At low frequency (flat region) the pore resistance dominates and the current is independent of frequency. At higher frequency, on the other hand, the membrane capacitance predominates, and the current increases with frequency. (b) The response on the Ag/AgCl electrodes (red) and predicted membrane voltage transient response (blue) for the 12 nm silicon nitride membrane due to a step in the applied voltage from 1 to 0 V; the inset shows that according to the model there are two time constants associated with the membrane voltage. (c) The response on the MOS capacitor membrane $(V_{ply}-V_{soi})$ due to a voltage step from 1 to 0 V applied across the Ag/AgCl electrodes; the inset shows the longer time constant associated with the voltage response.

Figure 3(a) shows the current frequency responses in 1 M KCl electrolyte that typifies four types of membranes with nanopores: two associated with different nitride thicknesses 12 and 200 nm on a silicon substrate, a third associated with a composite 30 nm nitride membrane coated with a $3.6 \pm 0.6 \,\mu \text{m}$ polyimide film on a silicon substrate and a fourth associated with a membrane formed from a MOS capacitor. We examined nanopores in eleven 12–30 nm thick membranes, two 200 nm thick membranes, three \sim 30 nm membranes with polyimide, and two MOS capacitor membranes. Each membrane has a nanopore in it ranging in diameter from 2 to 7.5 nm—comparable to the DNA double helix in crosssection. In figure 3(a), the 12 nm membrane has a $3.3 \times$ 4.8 ± 0.2 nm cross-section pore in it; the 200 nm membrane a $3.0 \times 3.8 \pm 0.2$ nm pore; the 30 nm membrane with polyimide on top—a $1.7 \times 2.8 \pm 0.2$ nm pore; and the MOS membrane—a $7.1 \times 7.3 \pm 0.3$ nm pore. Generally, we find that the frequency response of the current through the membrane consists of two components: one associated with the conductance through the pore that predominates at low frequency and is manifested by zero-slope versus frequency; and another due to the displacement current associated with the membrane capacitance and associated parasitics. While both depend linearly on the applied voltage, the displacement current increases with frequency, which is why the current grows so large at high frequency.

These general observations are well described by the simplified model proposed by Smeets *et al* [9], which is represented schematically in the inset to figure 3(a). According to this model, the Fourier transform of the ac current response, i, is related to the voltage applied at the Ag/AgCl electrodes $v_{\rm in}$, and the ac voltage, $v_{\rm m}$, by:

$$i(\omega) = \frac{(1 + \mathrm{j}\omega R_\mathrm{p} C_\mathrm{m})}{R_\mathrm{p} + R_\mathrm{el} (1 + \mathrm{j}\omega R_\mathrm{p} C_\mathrm{m})} \upsilon_\mathrm{in}.$$

Thus, the frequency at which the displacement current predominates is identified with zero in the numerator: i.e. product of the pore resistance and the membrane capacitance $f_z=1/2\pi\,R_{\rm p}C_{\rm m}$. Beyond this frequency the response is essentially determined by the membrane capacitance since $R_{\rm p}\gg R_{\rm el}$, generally. We infer that a change in the resistance due to the translocation of a molecule through the pore primarily affects the current response at low frequency. This hypothesis is supported by the observation in figure 3(a) that the magnitude of the current response at 1 Hz scales according to the changing pore diameter. A change in the pore resistance also affects the (Fourier transform of the) membrane voltage, $v_{\rm m}$, according to:

$$\upsilon_{\mathbf{m}}(\omega) = i(\omega) \frac{R_{\mathbf{p}}}{(1 + j\omega R_{\mathbf{p}}C_{\mathbf{m}})} = \frac{R_{\mathbf{p}}}{R_{\mathbf{p}} + R_{\mathbf{el}}(1 + j\omega R_{\mathbf{p}}C_{\mathbf{m}})} \upsilon_{\mathbf{in}}$$

$$\cong \frac{1}{1 + j\omega C_{\mathbf{m}}R_{\mathbf{el}}} \upsilon_{\mathbf{in}} \tag{1}$$

so that the voltage across the membrane has a pole at $f_{\rm p}=1/2\pi\,R_{\rm el}C_{\rm m}$ so that the transient response is characterized by: $\upsilon_{\rm m}(t)=\upsilon_{\rm in}{\rm e}^{-t/C_{\rm m}R_{\rm el}},$ which has a transient response time of $\tau=C_{\rm m}R_{\rm el}\sim 1~\mu{\rm s}$ for typical values found in our experiments (i.e. with $C_{\rm m}=100~{\rm pF}$ and $R_{\rm el}=10~{\rm k}\Omega$). To

improve the sensitivity and frequency response, the change in the resistive component to the current response associated with a translocation should be exaggerated. One way to accomplish this is by reducing $C_{\rm m}$, which has the effect of pushing the zero in the current and the pole in the membrane voltage to higher frequencies.

In the simple model shown in figure 3(a), the membrane capacitance is actually lumped together with various parasitic elements associated with the handle wafer, the Debye layer, etc, but to mitigate the effect of the parasitics, we first have to identify their physical origin. To identify the parasitic elements we used the models shown in figures 3(a)–(c) that correspond respectively to the nitride, the composite nitride/polyimide and the MOS capacitor membranes and are based on the physical structures. In addition to the capacitance of dielectric materials such as polyimide, Si₃N₄, SiO₂, and tetraethyl orthosilicate oxide (TEOS), the models also account for the depletion layer capacitance in the Si handle wafer, the dielectric loss in each case, the resistivity of the substrate, the resistivity of the KCl electrolyte, the double layer that is associated with the interface between a charged surface and an electrolyte solution, and the Faradaic impedances associated with charge transfer. To determine the parameters governing the model, the values of the various lumped elements were first estimated from the geometry and bounded, and then the data were fitted to the model using a least-squares minimization algorithm to converge to the final values. As a test of the uniqueness of the parameters, different measurement configurations such as membranes with and without a pore, and with and without polyimide were used in combination with different electrolyte concentrations (ranging from 100 mM to 1 M KCl), different membrane thicknesses and/or different membrane areas were used. Fits to the corresponding models are represented by the solid lines in figure 3(a). Table 1 delineates the model parameters used to fit the data of figure 3.

These models accurately account for the measured current The fit to the data taken on the and voltage responses. 12 nm thick nitride membrane on a silicon substrate using the model of figure 4(a) reveals that the frequency response cannot be accurately represented by the single capacitor model, but rather consists of a parallel combination of three highpass filters in parallel with the pore resistance. As illustrated in the figure, the pore conductance (121 M Ω) predominates at low frequency, but as the frequency increases beyond $f_{z0} = 1/2\pi R_{\rm p} C_{\rm mem1} \sim 0.9$ Hz the admittance associated with the membrane capacitance eventually shorts out the pore resistance. The capacitances associated with the nitride $(C_{\rm mem1} \sim 1520 \ {\rm pF})$ and the depletion layer $(C_{\rm db} \sim 900 \ {\rm pF})$ are comparable and much smaller than the series capacitance associated with the double layer, and so they predominate.

However, the admittance due to the depletion layer capacitance is smaller than the silicon conductance and so the admittance at very low frequency is predominately due to the membrane capacitance associated with the nitride layer spanning the entire silicon handle. Thus, the low corner frequency corresponds to the time constant due to the membrane capacitance and the pore resistance, as expected. The corner frequency related to the first high-pass filter

Table 1. Values for the lumped elements associated with the models of figure 4 extracted from fits to data shown in figure 3.

	12 nm Si ₃ N ₄ 50 μm × 50 μm	$\begin{array}{c} \text{Imide/Si}_3\text{N}_4 \\ 10 \ \mu\text{m} \times 10 \ \mu\text{m} \end{array}$	200 nm Si ₃ N ₄ 500 μ m × 500 μ m	MOS cap $10 \ \mu\text{m} \times 10 \ \mu\text{m}$	Units
$R_{\rm el}$ electrolyte resistor	0.85	0.61	0.9	0.3	kΩ
$F_{\rm dlt1}$ top double layer Faradaic coefficient	28.0	7.3	4.0	26.0	$G\Omega$
$C_{\rm dlt1}$ top double layer capacitor	303	303	184	6.7	nF
$R_{\rm im1}$ polyimide resistor	n/a	122	n/a		$G\Omega$
$C_{\rm im1}$ polyimide capacitor	n/a	18.3	n/a		pF
$R_{\text{mem1}} \text{Si}_3 \text{N}_4$ resistor	0.80	1.60	3.89	1.92	$T\Omega$
$C_{\text{mem1}} \text{Si}_3 \text{N}_4$ capacitor	1.52	0.73	0.15	0.041	nF
$R_{\rm dt}$ top depletion region resistor	22.7	22.7	91.2	29	$k\Omega$
$C_{\rm dt}$ top depletion region capacitor	308	308	46.7	454	pF
$R_{\rm si}$ Si resistor	25	25	21.8	18	Ω
$R_{\rm db}$ bottom depletion region resistor	706	706	800	580	$k\Omega$
$C_{\rm db}$ bottom depletion region capacitor	0.90	0.90	0.30	1.19	nF
$R_{\rm ins}$ native oxide/nitride layer resistor	86.3	86.3	147	101	$G\Omega$
$C_{\rm ins}$ native oxide/nitride layer capacitor	30.2	30.2	21.7	4.73	nF
F_{dlb1} bottom double layer Faradaic coefficient	5.60	9.90	9.50	35.0	$G\Omega$
$C_{\rm dlb1}$ bottom double layer capacitor	3.3	3.0	1.57	0.0102	μ F
$F_{\rm dlt2}$ top double layer Faradaic coefficient		1.20			TΩ
$C_{\rm dlt2}$ top double layer capacitor		2.70			nF
$R_{\rm im2}$ polyimide resistor		1.41			$T\Omega$
C_{im2} polyimide capacitor		7.0			fF
$R_{\text{mem}2}$ Si ₃ N ₄ resistor		15.0			$T\Omega$
$C_{\text{mem}2}$ Si ₃ N ₄ capacitor		3.7			pF
F_{dlb2} bottom double layer Faradaic coefficient		80.0			$G\Omega$
$C_{\rm dlb2}$ bottom double layer capacitor		2.18			nF
F_{dlt3} top double layer Faradaic coefficient	680	140	100		GΩ
$C_{\rm dlt3}$ top double layer capacitor	2700	28	250 000		pF
$R_{\text{mem}3} \text{Si}_3 \text{N}_4 \text{ resistor}$	11.6	56.7	503		$T\Omega$
$C_{\text{mem}_3} \text{Si}_3 \text{N}_4$ capacitor	8.1	0.08	169		pF
F_{dlb3} bottom double layer Faradaic coefficient	34.0	0.28	300		$G\Omega$
C_{dlb3} bottom double layer capacitor	2.18	0.28	245		nF
$R_{\rm elp}$ electrolyte resistor over PLY	2.10	0.20	213	3.6	kΩ
F_{dlp} double layer over PLY Faradaic coefficient				23.0	GΩ
C_{dlp} double Layer over PLY capacitor				0.25	nF
C_{tnp} TEOS/SiN capacitor over PLY				2.0	рF
R_{tnp} TEOS/SiN resistor over PLY				2.4	$G\Omega$
$C_{ m mos}$				0.92	pF
$R_{ m mos}$				384	$M\Omega$
$C_{\rm bs}$ BOX under SOI capacitor				4.2	pF
$R_{\rm bs}$ BOX under SOI resistor				9.5	$G\Omega$
F_{dls} double layer under SOI Faradaic coefficient				250	$G\Omega$
$C_{\rm dls}$ double layer under SOI capacitor				0.6	nF
$R_{\rm els}$ electrolyte resistor under SOI				5.0	kΩ
$R_{\rm sp}$ PLY resistor				7.0	kΩ
$L_{\rm sp}$ PLY inductor				38	nH
*					kΩ
R _{ss} SOI resistor				8.0 2.3	
L _{ss} SOI inductor				۷.3	nН

is found at: $f_{\rm p1}=1/2\pi(R_{\rm dt}+R_{\rm db}+R_{\rm L})C_{\rm mem1}\sim 1/2\pi(705~{\rm k}\Omega+23~{\rm k}\Omega+10~{\rm k}\Omega)C_{\rm mem1}=145~{\rm Hz},$ corresponding to the time constant given by the product of the membrane capacitance, and the sum of the top and bottom depletion resistances in series with the load resistance associated either with the electrolyte and/or the current amplifier, depending on the electrolyte concentration. The corner frequency associated with the second high-pass filter is found at: $f_{\rm p2}=1/2\pi(R_{\rm dt}+R_{\rm L})C_{\rm db}\sim1/2\pi(22~{\rm k}\Omega+10~{\rm k}\Omega)C_{\rm db}=5.5~{\rm kHz}.$ At this frequency, the admittance associated with the membrane capacitance, $C_{\rm mem1}$, is so large that it effectively shorts the nitride resistance, and the depletion layer capacitance $C_{\rm db}$ dominates the response. Finally, we find a third corner frequency associated with another high-pass

filter at: $f_{\rm p3}=1/2\pi\,R_{\rm L}(C_{\rm mem3}+C_{\rm c})\sim 1/2\pi\,(10\,{\rm k}\Omega)\times(8.1+210\,{\rm pF})=73\,{\rm kHz}$, corresponding to the time constant given by the product of the capacitances due to the membrane over the via in the silicon handle ($C_{\rm mem3}$) and the coaxial cable ($C_{\rm c}$) used for the measurement and the electrolyte resistance. Near 650 kHz, the lock-in amplifier admittance (25 pF in parallel with 100 M Ω) becomes larger than the load resistor we used for the measurement and the current increases again because the lock-in loads the nanopore circuit.

To test these assignments, we analyzed the frequency response of two other pores in a nitride membrane: one in a 200 nm thick nitride membrane with a 500 μ m \times 500 μ m area and another in a composite membrane consisting of a 30 nm thick nitride layer with a 10 μ m diameter window defined by

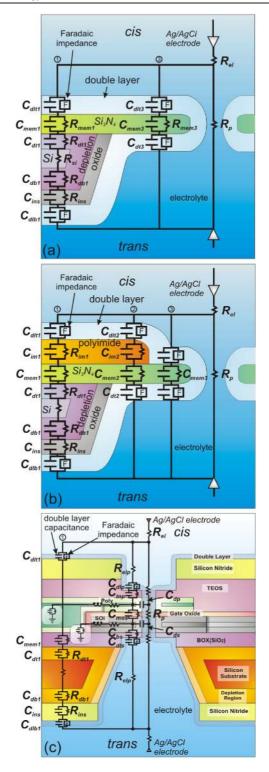


Figure 4. Schematics of the lumped element models superimposed on the physical geometry (not to scale) and used to analyze the frequency response of (a) a nitride membrane. (b) A composite polyimide/nitride. (c) A nanopore in a membrane formed from a MOS capacitor. The Faradaic impedances, double layer capacitances, depletion capacitance, and series resistances are all represented and fitted using ADS software.

an \sim 4 μ m thick polyimide layer, also shown in figure 3(a). In each case, the concomitant increase in membrane thickness decreases a portion of the parasitic membrane capacitance,

making it small compared with the depletion layer and double layer capacitances, and eliminating their contributions to the frequency response. The fits to these two membranes reveal that the pore resistance is in parallel with a single dominant capacitance, and a single high-pass filter now predominates. For example, in the case of the polyimide-covered membrane, the zero occurs at $f_{z0} = 1/2\pi R_{\rm p}C_{\rm im1} \sim 23$ Hz and the pole is at $f_{\rm p3} = 1/2\pi R_{\rm L}(C_{\rm im1} + C_{\rm c}) \sim 1/2\pi(10~{\rm k}\Omega) \times (18 + 210~{\rm pF}) = 70~{\rm kHz}$. Thus, the frequency response improves because the effect of the silicon nitride, depletion and double layer capacitances is diminished.

The step response of the membrane voltage represents an especially stringent test of these models, but a direct measurement of it is generally inaccessible in the nitride and nitride/composite membranes due to the intervening parasitic elements. Figure 3(b) shows measurements of the voltage response to a 1 V step measured at the Ag/AgCl electrodes in 1 M KCl along with the predicted voltage drop across the membrane according to the model of figure 4(a). The voltage drop on the Ag/AgCl electrodes can be characterized by a single time constant 13 ns, which is determined largely by the bandwidth of the function generator and the oscilloscope (TDS2024) with which the measurement was taken, while the corresponding membrane voltage is predicted to have two components: a fast response at $R_{\rm el}C_{w1}=185$ ns time constant $(C_{w1}$ is dominated by the series combination of C_{mem1} , C_{dt} , $C_{\rm db}$, in parallel with $C_{\rm mem3}$) delineated in figure 3(b) and a slower response at $R_{\rm dt}C_{w2}=9.2~\mu{\rm s}$ (on this timescale the impedance of $C_{\rm dt}$ is comparable to but larger than $R_{\rm dt}$, C_{w2} is dominated by the series combination of $C_{\text{mem}1}$ and C_{db}) shown in the inset to the figure. The discrepancy between the modeled membrane response and the measured response at the Ag/AgCl electrodes is associated with the silicon nitride membrane and frame depletion capacitances and the electrolyte resistance.

Since DNA translocation velocity depends sensitively on it, the membrane voltage is critical to applications such as sequencing, and so we attempted to measure it directly using polysilicon and silicon electrodes in the MOS capacitor membrane. The difference voltage measured at the polysilicon and SOI electrodes comprising the MOS capacitor of figure 3(a), along with the corresponding predictions of the model based on the parameters extracted from the fit to the current response, are shown in figure 3(c). The voltage response across the membrane tracks the voltage at the Ag/AgCl electrodes, but it is attenuated by a factor of \sim 4. We also observe a fast time constant associated with charging of the amplifier capacitance through the polysilicon lead: i.e. $R_{\rm sp}C_{\rm amp}=24~{\rm ns}$.

The attenuation is mainly due to the finite impedance of the amplifier with which the measurement was taken (1 $M\Omega$ resistor in parallel with a 6 pF capacitor including stray capacitances denoted by 1 $M\Omega$ \parallel 6 pF hereafter) and also to the parasitics in the structure. To validate the model we placed 1 $M\Omega$ \parallel 6 pF across the measurement pads and tried to predict the measured voltage. Figure 3(c) shows the measured as well as the predicted response of the membrane. The model accurately accounts for the measured step response except for times <100 ns. (Since the model was developed from

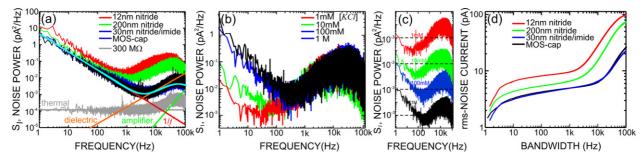


Figure 5. Current noise spectra measured in nanopores of figure 2. (a) Noise power spectra of nanopores in the four membranes of figure 3(a) measured in 1 M KCl with different effective capacitance. From bottom to top, a 300 MΩ resistor, a $7.1 \times 7.3 \pm 0.3$ nm pore in a MOS membrane, a $1.7 \times 2.8 \pm 0.2$ nm pore in a polyimide coated Si₃N₄ membrane, a $3.0 \times 3.8 \pm 0.2$ nm pore in ~200 nm Si₃N₄ membrane, and a $3.3 \times 4.8 \pm 0.2$ nm in 12 nm Si₃N₄ membrane. The low frequency 1/f noise (red), the high frequency dielectric noise (orange) along with the amplifier noise(green) are analyzed for the ~2.4 nm pore in the polyimide coated membrane. The fit to the total noise is shown in blue. (b) Noise spectra of a $2.1 \times 2.3 \pm 0.2$ nm pore in 12 nm nitride membrane for different electrolyte concentrations. (c) The same noise spectra shown in (c) but offset to show the high frequency noise without overlap. (d) The rms-current noise versus bandwidth for the membranes of (a); the largest contributor to the rms-current noise is dielectric noise prevalent above 1 kHz frequency.

measurements made at frequencies ≤ 2 MHz, it may not be accurate for t < 80 ns.) The model also accurately captures the longer time voltage transient that occurs after the voltage has been turned off when the capacitances in the system are discharging (see inset of figure 3(c)). The time constant is about 7 μ s and is dominated by the amplifier input impedance (1 M Ω || 6 pF). The rise time of <50 ns shown in figure 3(c) indicates that an MOS membrane is particularly suitable for performing measurements on timescales appropriate for applications such as sequencing that require high bandwidth.

The noise power spectra of the same four nanopores described in figure 3(a) measured in 1 M KCl are shown in figure 5(a) along with the spectrum of a 300 M Ω resistor, a value comparable to the resistance of the 2.2 nm pore in figure 1. We analyzed the noise into three components: thermal, 1/f, and dielectric noise. We expect that the thermal noise spectral density associated with the pore resistance, S_t = $4k_BT/R$, will be negligible over the band < 100 kHz since the noise from the resistor is below all of the nanopore spectra. White noise arising from charge fluctuations is typically negligible in our membranes, because we are focusing primarily on short 12-30 nm ion channels. In recent work, Hoogerheide et al [17] fabricated longer channels (55 nm) with larger surface area where the white noise spectrum is on the order of $3 \times 10^{-3} \text{pA}^2 \text{ Hz}^{-1}$, but we do not observe a white noise spectrum.

At low frequencies we observed that the noise power density is inversely proportional to the frequency, which is indicative of excess or 1/f, noise. Its noise power spectrum is modeled by: $S_{1/f} = I^2 A/f^\beta = I^2 (\alpha/N_c)/f^\beta$ where I is the current through the device, α is the Hooge parameter (an empirically determined proportionality constant that depends on the type and concentration of charge carriers), N_c is the total number of current carriers, f is the frequency, and β is an exponent that is typically unity [10]. This portion of the spectrum can be described with mean $\beta = 1.09 \pm 0.31$, depending on the electrolyte concentration. As illustrated in figures 5(b), (c), we find that the noise spectrum <1 kHz is sensitive to the electrolyte concentration, while the high

frequency noise is not. Hooge suggested that 1/f noise occurs in bulk conductors due to the fluctuating mobility of charge carriers that produces current fluctuations [18, 19]. In contrast, there are surface models in which charge traps located on the pore surface have a fluctuating charge state that affects the ionic current and likewise exhibits a 1/f characteristic [10]. The two models can be differentiated by the dependence of the coefficient, A, on the number of charge carriers (or pore conductance.) It has been previously reported that charge fluctuations due to surface traps are relatively unimportant in pores ~ 9 nm diameter in membranes about ~ 25 nm thick, and that Hooge's relation better describes low frequency 1/f noise [10].

Using a $2.1 \times 2.3 \pm 0.2$ nm cross-section pore in a 12 nm thick nitride membrane, we measured the dependence of A on the electrolyte concentration, (assuming an activity factor of 1 independent of concentration). The results are displayed in figure 6. The low frequency current noise spectral density was obtained with 100 mV bias across the membrane. Fits to the spectra revealed $\beta = 0.84 \pm 0.08$, 0.94 ± 0.08 , 1.04 ± 0.07 , and 1.53 ± 0.09 at 1, 10, 100 mM, and 1 M KCl concentrations, respectively. Then, after fixing the exponent $\beta = 1.0$, we determined the coefficient A as a function of electrolyte concentration in the same pore. We found that the data shown in figure 6(a) can be described by $A = A_0[KC1]^{\gamma}$, where $A_0 = 9.3 \pm 5.1 \times 10^{-5}$ and $\gamma = -0.39 \pm 0.12$, as illustrated in figure 6(b), which is consistent with prior estimates obtained from both larger diameter pores (~10 nm) in 20 nm thick nitride membranes [10] and proteinaceous pores [20]. Figure 6(b) also illustrates the coincidence we observe between the scaling of A and the pore resistance with electrolyte concentration. The coefficient A scales with the pore resistance according to the law: $A = R_p^n$ with $n = 0.68 \pm$ 0.17 in this case. The pore resistance depends on both the ion mobility and the fixed charge in the pore [13], and so we tested Hooge's model further by examining the coefficient A derived from the 1/f noise spectra of pores with different diameters ranging from 1.9–4.2 nm in membranes of various thicknesses ranging from 11 to 30 nm at electrolyte concentrations ranging from 1 mM to 1 M KCl. The results, which are summarized in

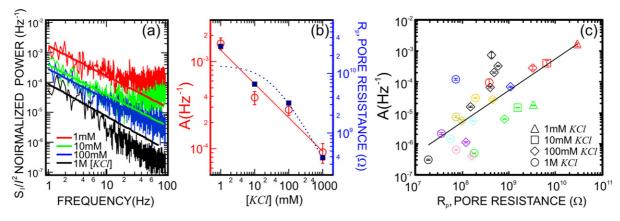


Figure 6. The current noise scales with pore resistance. (a) The low frequency current noise spectral density was obtained with 100 mV bias across the membrane with a $2.1 \times 2.3 \pm 0.2$ nm pore. The noise data is fitted to $S_I/I^2 = A/f^\beta$, with corresponding vales of $\beta = 0.84 \pm 0.08$, 0.94 ± 0.08 , 1.04 ± 0.07 , and 1.53 ± 0.09 for 1, 10, 100, and 1000 mM KCl concentration. (b) Plot of Hooge coefficient A and the pore resistance, R_p , as a function of KCl concentration with fit to $A = A_0$ [KCl] $^\gamma$, with $A_0 = 9.3 \pm 5.1 \times 10^{-5}$ and $\gamma = -0.39 \pm 0.12$. (c) The coefficient A of several nanopores as a function of pore resistance (for electrolyte concentrations ranging from 1 mM to 1 M) with respect to the pore resistance. A fit to $A = A_{0p}/G_p^n$ or $A = A_{0p}R_p^n$ reveals $n = 1.03 \pm 0.44$.

figure 6(c), show a systematic dependence of the coefficient A on the pore resistance over a factor of $10\,000\times$, categorically supporting the conclusion that $A \sim R_{\rm p}^n$, where $n=1.03\pm0.44$.

Figure 5(d) illustrates that 1/f noise becomes negligible at frequencies >1 kHz, and the spectrum exhibits linear frequency dependence up to about 50 kHz. According to the figure, the noise in the range 100 Hz-50 kHz is the dominate contribution to the rms-current noise—it is exponentially larger than the 1/f component. The linear frequency dependence coupled with the lack of a dependence of the noise in this part of the spectrum on the electrolyte concentration, which is evident from figures 5(b) and (c), indicates dielectric noise with a spectrum of the form: $S_D = 4k_BTDC_D(2\pi f)$, where $k_{\rm B}$ is Boltzmann's constant, T is the absolute temperature, and D and C_D are the loss tangent and the effective capacitance of the dielectric material. This capacitance and loss tangent are directly related to the lumped elements comprising the circuits in figures 4(a)–(c): i.e. the loss tangent is the tangent of the angle between the capacitor impedance vector and the negative reactance. Figure 7(a) supports this hypothesis by showing how the rms-current noise increases with the effective capacitance over a range in capacitance from 8 pF to 900 pF. We calculated the effective capacitance from an appropriate model for either nitride membranes and nitride membranes coated with polyimide and found that $\Delta I_{\rm rms} \sim \sqrt{C_{\rm eff}}$ as shown by the line fitted to the data, indicative of dielectric noise.

Thus, reducing the membrane capacitance is the key to improving both the frequency and noise performance. From the close correspondence between our models and the measurements of the frequency response, we assert that this can be accomplished by either using a composite membrane consisting of a polyimide and nitride layers to reduce the effect of parasitic elements such as the depletion layer in the substrate or by replacing the silicon handle wafer altogether with a dielectric substrate. For example, figure 7(b) explicitly shows the improvement in the signal to noise ratio that can be achieved by using a composite membrane of polyimide

and nitride layers. The figure compares a current blockade associated with a single λ -DNA translocating through a 3.9 \pm 0.2 nm diameter pore in a 30 nm thick nitride membrane 50 μ m \times 50 μ m in area with a current blockade in a 3.0 \pm 0.2 nm pore in the same type of membrane but with a polyimide layer nominally 4 μ m thick coating it, reducing the effective area of the membrane to a 10 μ m window. We observe a substantial reduction in the peak-to-peak noise in the open pore current at 1 V (940–370 pA overall and 890–290 pA excluding low frequency 1/f noise) as well as the blockade current (920–330 pA), which facilitates the examination of the current fluctuations during a blockade that may provide information on the DNA sequence.

Another alternative for mitigating the effect of parasitic capacitance is compensation through external circuitry. This technique has already been used successfully for patch clamping [21]. We compensated for the capacitance associated with the three high-pass filters that represent the frequency response of a thin nitride membrane with the circuitry represented in the block diagram shown in figure 8(a). Essentially, the circuit works by using feedback to sense the change in the voltage across the Ag/AgCl electrodes and provides the necessary current to charge the capacitors in the high-pass filter elements that constitute the membrane effectively restoring the high frequency response and nullifying the effect of the membrane capacitance on the current measured by the Axopatch 200B. Each high-pass filter has to be separately compensated to improve the fidelity at high frequency response—a single element cannot compensate for the membrane capacitance—however, this introduces further complications into the compensation circuit. Figure 8(b) shows the step response of a 2.2 ± 0.2 nm diameter pore in a 30 nm membrane 15 μ m \times 15 μ m in area. This circuit compensates for three (poles) high-pass filters, extending the frequency response of the pore to >650 kHz so that the voltage response time is on the microsecond timescale, but the noise is excessive, increasing from \sim 28 to nearly 250 pA-rms.

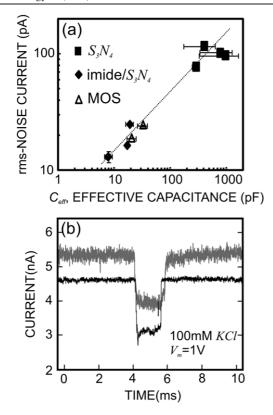


Figure 7. Dielectric noise predominates at high frequency. (a) The rms-current noise measured at 1 M KCl of several engineered membranes (silicon nitride, a composite membrane formed from polyimide and nitride, and an MOS capacitor membrane) with respect to effective capacitance derived from a simple one-capacitor model. The rms-noise scales as $\sim C_{\rm eff}^{1/2}$ as expected for dielectric noise. (b) Current blockades observed in 100 mM KCl due to the translocation of λ -DNA through a 3.9 ± 0.2 nm pore in a 30 nm membrane (grey trace) and a 3.0 ± 0.2 nm pore in a 30 nm membrane with polyimide on it (black trace); both traces are taken in 100 mM KCl at 1 V applied across the membrane; the peak-to-peak noise is dramatically improved in the membrane covered with $\sim\!4~\mu{\rm m}$ of polyimide (black trace).

4. Conclusions

Single molecule detection with a nanopore can be compromised by the poor high frequency and noise performance. To illuminate strategies for improving the performance, we measured the frequency and noise characteristics of nanopores in a variety of membranes and modeled the results. We found that measurements of the frequency and noise performance can generally be captured by lumped element models consisting of three high-pass filters in conjunction with the pore resistance that are motivated by the physical structures. We then explored four strategies to improve the electrical performance by reducing the membrane capacitance using: (1) thick Si₃N₄ membranes; (2) miniaturized composite membranes consisting of Si₃N₄ and polyimide; (3) miniaturized membranes formed from metal-oxide-semiconductor (MOS) capacitors; and (4) capacitance compensation through external circuitry, which has been used successfully for patch clamping. While capacitance compensation provides a vast improvement in the frequency response, mitigation of the parasitic capacitance

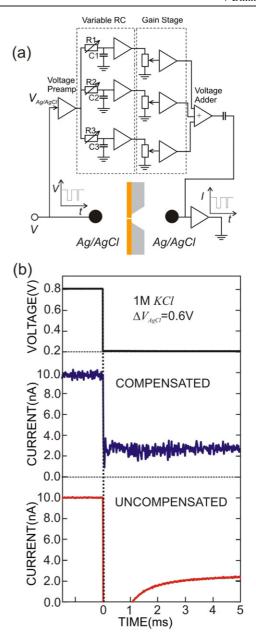


Figure 8. Capacitance compensation improves the high frequency performance. (a) The feedback circuit used for charging the distributed membrane capacitance and eliminating its effect on the current measured by the amplifier; (b) the response of the measured current in 1 M KCl to a voltage step from 800 to 200 mV in a 2.2 ± 0.2 nm pore in a 30 nm membrane 15 μ m \times 15 μ m in area, with and without compensating for the membrane capacitance. The capacitance compensation circuit helps to reveal the response of the current through the pore to a change in the applied voltage, but it introduces noise into the measurement.

through miniaturization offers the most promising route to high fidelity electrical discrimination of single molecules.

The high frequency and noise performance of the pore current are especially critical for applications like sequencing because the translocation velocity of the DNA is so high in a solid-state nanopore, exceeding 1 bp/10 ns [11]. According to the model of Smeets $et\ al\ [9]$, the frequency response is essentially determined by the product of $C_{\rm m}$ and $R_{\rm el}$ so that

 $R_{\rm el}C_m > 1-10~\mu{\rm s}$ for the 2.2 nm pore in a 15 nm thick nitride membrane in 100 mM KCl, corresponding to a bandwidth of $\Delta f = 1/2\pi R_{\rm el} C_{\rm m} \sim 100$ kHz. Thus, if the translocation velocity is high, it becomes impossible to resolve that portion of the blockade associated with a single base; >16 MHz bandwidth would be required. More gain cannot resolve this problem due to the concomitant increase in electrical noise. If dielectric noise associated with the membrane capacitance predominates for f > 1 kHz, then $I_{\rm rms}^2 = 4$ kT $DC_{\rm m}\pi \Delta f^2$ where D is the dielectric loss constant. Thus, the membrane capacitance has to be chosen for adequate signal-to-noise. The data shown in figure 1(c) indicate that the relative change in current associated with λ -DNA blockading a pore is $\Delta I/I$ 0.78, which translates into a $\Delta I \sim 2-3$ nA for a 2.2 nm diameter pore. Therefore, to detect a molecule with signal-tonoise ratio SNR > 2, we need peak-to-peak noise < 1.5 nA or an rms value of $\Delta I_{\rm rms} \sim 1.5 \, {\rm nA/8} = 190 \, {\rm pA}$. For a bandwidth of $\Delta f < 100$ kHz, we estimate that $DC_{\rm m} \sim 70$ pF is required to detect a current signature. Correspondingly, according to molecular dynamics simulations [12] to detect a single basepair in a pore smaller in diameter than the double helix of DNA, we must resolve a difference signal of $\Delta I \sim 15$ pA so that $\Delta I_{\rm rms} \sim 1.90$ pA at a bandwidth commensurate with a translocation velocity of 1 bp/10 ns ($\Delta f \sim 16$ MHz). This noise specification is less than the thermal noise ($I_{\rm rms} =$ $\sqrt{4kT\Delta f/R} \sim 30$ pA) associated with the pore resistance for a 2.2 nm pore. If only dielectric noise is considered, then signal-to-noise considerations demand $DC_{\rm m} \sim 0.3$ aF for a $\Delta f \sim 16$ MHz, consistent with a translocation velocity of 1 bp/10 ns. Thus, for D = 0.0001, we required $C_{\rm m} = 3$ fF, which corresponds to a parallel plate capacitor ~300 nm on edge with a 1 nm thick SiO₂ dielectric between the electrodes, which can be easily achieved with current silicon device technology. From this extrapolation, we conclude that a solidstate nanopore in a membrane engineered with state-of-theart fabrication techniques could have adequate frequency and noise performance for high-throughput DNA sequencing.

Acknowledgments

This work was funded by grants from National Institutes of Health [R01 HG003713A, PHS 5 P41-RR05969] and the National Science Foundation Physics Frontier Center [TH 2008-01040 ANTC].

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