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Nanoscale Electrolytic Switching in Phase-Change Chalcogenide Films**

By *Ramanathaswamy Pandian, Bart J. Kooi,* George Palasantzas, Jeff T. M. De Hosson, and Andrew Pauza*

This Communication presents the important finding that certain chalcogenide materials, well-known from rewritable optical recording, allow resistive memory states that are a combination of two electrically-induced (reversible) switching processes, i.e., an actual amorphous-crystalline phase transformation and a (electrolytic) polarity-dependent resistance change. Nanometer-sized crystalline marks were written electrically in amorphous $Ge_2Sb_{2+x}Te_5$ films using atomic force microscopy (AFM), and their resistance was found to depend on the polarity of the applied voltage with a resistance difference of three orders of magnitude. However, no contrast in current has been detected between the crystalline higher-resistance state and the surrounding amorphous phase. This resistance switching is reversible for bias voltages well below the threshold voltage required to induce the phase transformation. The switching mechanism is attributed to the solid-state electrolytic behavior due to the presence of excess Sb in the films. Our results render exciting technological opportunities for data storage and encryption by combining both switching concepts.

Following his seminal work in 1968,[1] Ovshinsky demonstrated in chalcogenide alloys a fast reversible transformation between amorphous and crystalline phases induced by electrical or optical (laser) pulses.[2–4] The two phases exhibited clear contrast in electrical and optical properties and, hence, these materials were suggested for binary data-storage applications. However, it took considerable time before rewritable optical compact discs (CD) and digital versatile discs (DVD) based on these findings came to the market. In recent years, the main focus of phase-change data-storage research returned to resistance switching. So-called chalcogenide or phase-change random access memory (CRAM/PRAM) and ovonic unified memory (OUM) based on the phase-dependent resistance switching are currently under intense investigations,[5–13] because they show great promise as next-generation nonvolatile solid-state memory replacing flash memory.

In certain chalcogenides a special phenomenon of polarity-dependent resistance switching (induced by an electric field) has been identified.[14–19] This is related to the solid-state electrolytic character and high ionic conductivities of chalcogenides, and hence is called ionic/electrolytic switching. For one polarity, the chalcogenide medium is electrically conductive by forming conducting filamentary pathways between electrodes, whereas for the reverse polarity it becomes relatively insulative or at least less conductive because of rupture of the previously formed electrical pathways. Memory elements (or structures) based on this switching have been demonstrated in some Ag-saturated chalcogenides including Ag–S,[14,15] Ag–Ge–Se,[16,17] Ag–Ge–Te,[18] and Ag–In–Sb–Te.[19] This switching seems more attractive for applications than phase-dependent switching, because i) it can be performed at lower voltages (e.g., < 0.5 V); and ii) does not involve major structural changes and, hence, effects like phase separation are limited, providing enhanced device life.

Data writing at the nanometer scale is essential for increased storage density fulfilling future requirements. Impetus to data-storage technologies has been given by AFM since data writing down to 20 nm is readily possible, and AFM has potential to read/erase the data.[20–27] AFM data writing can occur via thermal or electrothermal means. The former technique so far led to a potential data density of 3.3 Tb inch^{-2} although it is not yet functional.[27] To the best of our knowledge, data writing and erasing operations in chalcogenides have not been successfully demonstrated for multiple cycles using AFM only. Generally, crystalline marks in an amorphous surrounding were written and read, but mark erasing with AFM represents a formidable barrier for further advancement of this technique. Moreover, electrolytic switching in chalcogenides has been shown only for memory cell structures produced using lithography, but not yet studied with AFM at the nanometer scale.

Although the two resistance switching mechanisms (phase- and polarity-dependent) were up to now treated separately, it was recently conjectured that they were "different faces of a chameleon" that should be brought together and studied in a unified approach.[28] To the best of our knowledge, this is the first study exploiting these two mechanisms simultaneously.

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We demonstrate that in $Ge_2Sb_{2+x}Te_5$ (GST) films the contrast between crystalline marks and the amorphous background can be written and erased for a significant number of cycles using AFM only.

The electrical resistance of the chalcogenide material decreases several orders of magnitude when the amorphous phase is crystallized.[29,30] This large resistance change enables the bistable memory states of the OUM[8,31] or line cell concepts.[29] When the applied electric field (of either polarity) within the entire amorphous volume exceeds the threshold level, the amorphous phase becomes in a dynamic state with highly conductive paths for electrons. When current flow is maintained along these paths, Joule heating occurs and the structural change can be induced. This (initial) threshold switching in the amorphous phase is fast and seems to be a pure electronic process. The structural (or phase) transformation is generally accompanied by a density change; a density increase due to crystallization from 6 to 9% has been reported for amorphous $Ge_2Sb_2Te_5$ films.[30,32]

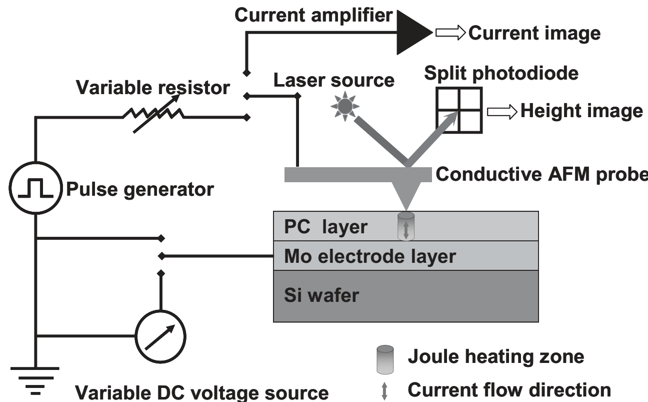

Figure 1. Schematic illustration of the C-AFM experimental setup, showing the sample structure and electronic circuit with various components. This setup simultaneously provides information on topography and electrical conductance of the sample.

In our study, we analyzed 20 or 40 nm thick sputtered amorphous $Ge_2Sb_{2+x}Te_5$ films. A conductive-AFM (C-AFM) was used for data writing and reading. Crystalline marks (i.e., data) were written on the amorphous film by passing electrical current via the AFM tip into the film (along the thickness), and reading was done by sensing the conductance and topography of the marks in comparison with the amorphous background. A schematic illustration of the experimental setup for write and read operations and sample structure is shown in Figure 1.

As an example, an array of crystalline marks written in an amorphous background (at a density of ~50 Gb inch^{-2}) is shown in Figure 2a. These nanocrystalline marks were written by injecting dc voltage pulses with +5 V amplitude and 500 ms temporal width from the tip into the electrically grounded film. Figure 2b and c indicates the density and resistivity variations of the film due to the structural change from amorphous to crystalline phase after the writing operation. The pits visible in Figure 2b are the nanocrystalline marks/bits. A line profile drawn along a row of crystalline pits in the topography image (Fig. 2c) shows a thickness decrease (due to crystallization) of about 2.5 nm, which corresponds to an increase in density of about 6%. This increase is in agreement with a density change of 6–7% observed by X-ray reflectometry (XRR) and AFM measurements in Ref. [32] for the transformation from amorphous to the rocksalt (face-centered cubic; fcc) phase in $Ge_2Sb_2Te_5$ films. Moreover, according to Ref. [32], it is likely that AFM crystallization favors formation of crystalline metastable fcc phase rather than the stable "hexagonal" one.

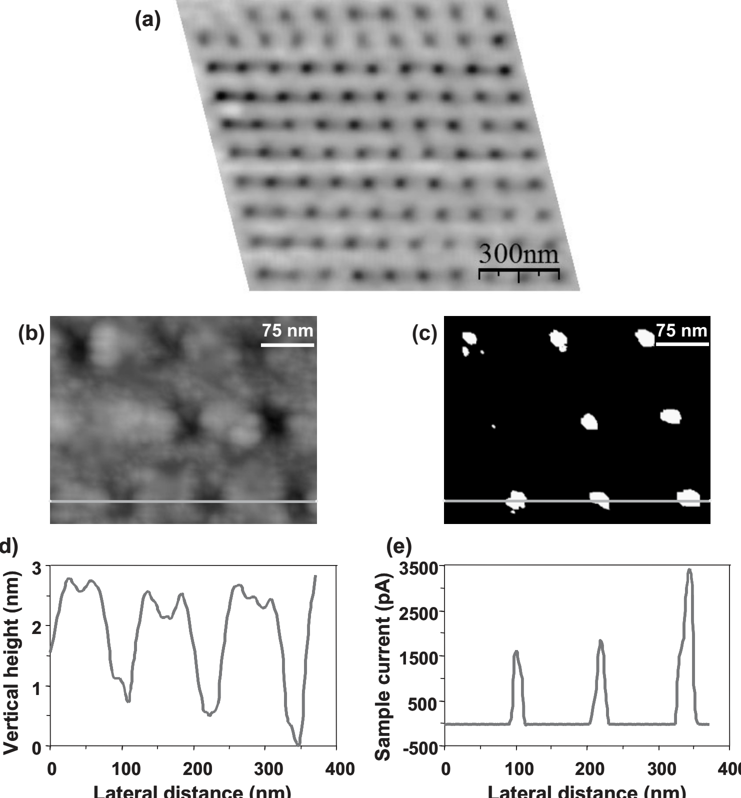

Figure 2. Electro-thermal data writing. a) A contact mode AFM topography image showing a written crystalline bit pattern in a 20 nm amorphous GST film. b,c) Simultaneously recorded topographic (or) height and current images, respectively, showing crystalline bits in a 40 nm amorphous GST film. d) Line profile, drawn over a row of crystalline bits of (b) showing the written bits as small nanovalleys. e) Line profile drawn on a row of highly conductive spots of (c). These spots are well distinguishable from the amorphous background with a current contrast of about three orders of magnitude, even though the current flow through them is only a few nanoamperes.

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In the current image of Figure 2c, which was recorded simultaneously with the topography image of Figure 2b, the crystalline pits are identified as current peaks because of their lower electrical resistance compared to the amorphous surrounding. This current image was taken by keeping the tip grounded and the film at +1 V dc bias. The nanocrystalline marks in the current image are clearly distinct from the amorphous background with a current contrast of three orders as shown in Figure 2e. Our C-AFM experimental setup allows current measurement down to 5 pA. Scanning the amorphous area with lower dc bias voltages (1 to 2 V) did not show any significant current flow above this lower limit.

Further investigations on the electrical pulse induced crystallization indicated that our samples exhibit a polarity-dependent resistance switching, i.e., the resistance of the crystalline written marks switched between a lower- and higher-resistance state when the polarity of the applied electric field across the sample was reversed. Figure 3a is a contact-mode AFM topography image showing an array of nanocrystalline marks in an amorphous background. The marks were written with voltage pulses of amplitude –5 V and width 500 ms. Continuous scanning of an area around the marks with a positive bias voltage, referred as a SET operation, brought them into a relative lower-resistance, or ON, state. On the other hand, a negative bias scanning, referred as a RESET operation, takes the marks to a higher-resistance, or OFF, state. The resistance of the amorphous phase remains below the current detection limit (5 pA) during these SET–RESET operations.

An example for SET and RESET operations, in a nanocrystalline mark, is shown in Figure 3. Figure 3b is the topograph of one of the crystalline marks considered for examination, from the bit pattern shown in Figure 3a. SET operation with +1.5 V brings the mark to a lower-resistance state, and hence it is visible as a highly conductive (bright) spot in the current image shown in Figure 3e. For a RESET operation with –1.5 V, the crystalline mark became equally insulating as the background. Therefore in the current image, Figure 3f, and the current profile, Figure 3i, no significant difference between the mark and the amorphous background is noticed. When the SET operation is repeatedly performed with +1.5 V, the mark switches back to the lower-resistance state and hence it is visible in the current image shown in Figure 3g. During SET and RESET operations the topography of the nanosized mark did not alter markedly (Fig. 3b–d), indicating that polarity-dependent resistance switching did not involve a phase-change. The ON-state current profiles shown in Figure 3h and j reveal that the mark has an electrical contrast of three orders of magnitude with its surrounding. The operating voltage required for this switching (±1.5 V) is clearly lower than the threshold voltage (> ±4 V) needed for inducing the amorphous–crystalline phase transition, indicating that the former type of switching is more advantageous for future device applications. Since the switching causes no detectable density changes, it should also be advantageous from a cyclability point of view.

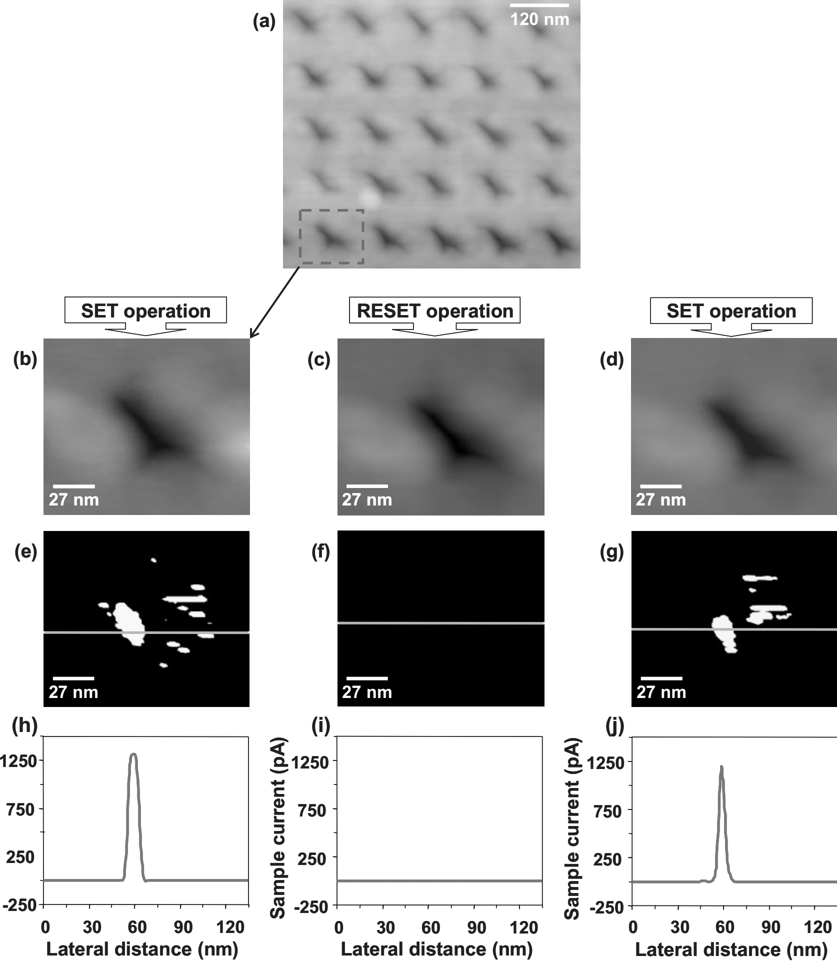

Figure 3. Polarity-dependent resistance switching at the nanometer scale. a) AFM topography image showing a crystalline bit pattern in a 40 nm amorphous GST film. b–d) Topography images of a bit during the SET, RESET, and SET operations, respectively. e–g) Current images recorded with ±1.5 V biasing showing ON, OFF, and ON states of the bit, respectively. h–j) ON, OFF, and ON state current profiles, corresponding to the images (e–g), respectively. Images (b–d) indicate that there is no detectable topographical change upon SET–RESET operations. ON-state current profiles, (h,j), show three orders current contrast between the high-conductivity written bit and the amorphous background. The current image (f) and current profile (i) of the bit at OFF state indicate that the OFF state conductivity of the bit is as low as the background amorphous phase.

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In the current images shown in Figure 3e and g, the ON-state (high-conductive) mark does not appear as a single spot, but discontinuously spreads over a small area around the center position of the mark, which is considered as the center of the pit in the topographs shown in Figure 3b and d. Note that such a discontinuous spot is also seen in the current image shown in Figure 2c. This is probably due to various issues that stem from the high current density in the nanosized tip-surface contact area and/or friction between the tip and sample during the writing and reading operations. These include: i) nonuniform tip–surface contact force, ii) increase in tip radius, iii) increase in roughness at the tip and sample surfaces, and iv) damage of the conductive coating on the tip.

Previous experimental work that shows resemblance with our work was performed on a $Ge_1Sb_2Te_4$ film.[21] Conductive marks in an insulating surrounding were written using an AFM. It was shown that a conductive mark could also be (once) erased by applying a low dc voltage (–1 V) to the tip, but for rewriting a higher voltage (3 V) was used. This voltage appeared to be above the threshold voltage for phase transformation in their setup. This observation poses restrictions on applications, since polarity-dependent memory switching could work at lower threshold voltages (e.g., ±1 V, as is demonstrated in this work). Polarity-dependent resistance switching was not reported in Ref. [21] and information on cyclability and data retention was not presented. Only current images were shown, but no topographic images. Further, the writing–erasing process was not attributed to either structural change or to electrolytic behavior of the phase-change material.

We also tested the resistance switching governed by the polarity of the applied field over a larger area of 500 nm × 500 nm, which was electrically treated with a negative bias voltage of 5 V at a scanning speed of 5 μm s^{-1}. The pretreated area was considered for SET–RESET operations by scanning an area of 1 μm x 1 μm, incorporating the treated (crystallized) area, with lower dc voltages (±1 V) as shown in Figure 4.

The experimental setup for SET–RESET operations is schematically illustrated in Figure 4a. During the SET operation, the sample was biased with +1 V with respect to the scanning tip that is electrically grounded, and the pretreated area was at a lower-resistance (ON) state (see Fig. 4b). In the current profile, shown in Figure 4c, the ON state of the mark shows approximately three orders higher electrical conductance than the background. When the polarity is reversed for the RESET operation (i.e., now the sample is at –1 V and tip at ground potential), the pretreated area reached the OFF-state, which made it completely indistinguishable from the amorphous surrounding, as shown in Figure 4d and e. Repeating the SET operation with a bias voltage of +1 reproduces the highly conductive ON state with almost the same contrast with respect to the untreated background (see Fig. 4f and g).

Figure 4b or f shows that the electrical conductivity inside the treated area (dashed square) is not uniform. A considerable fraction of treated area is still at a lower conductance state, which otherwise is expected to be homogeneously conductive during the SET operation. This inhomogeneous electrical conductivity is predominantly caused by an incomplete

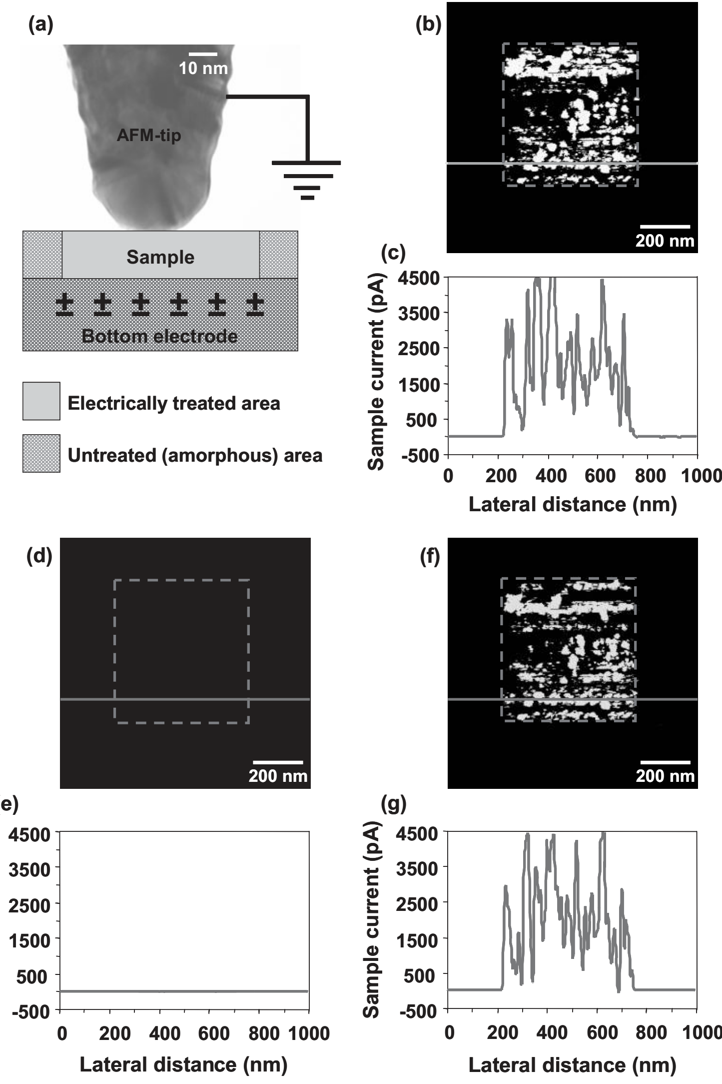

Figure 4. Polarity-dependent resistance switching at the sub-micrometer scale. a) Experimental setup for SET–RESET operations. b) Current image recorded with +1 V biasing showing a high-conductive area, which is previously treated with -5 V dc, in a low-conductive amorphous surroundings. c) Current profile of (b) showing the ON-state current, which is three orders higher than the untreated background current. d) Current image recorded during the RESET operation with –1 V biasing. e) Current profile of (d), indicating that the RESET operation brings back the resistance of the treated area to a higher value (OFF state) that is not distinguishable from the amorphous resistance. f,g) The current image and current profile, respectively, showing the reproducibility of the ON-state upon a repetitive SET operation with +1 V biasing.

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crystallization within the square area as can be deduced from the topography image (data not shown) and from the reproducibility of Figure 4b and f. The incomplete crystallization is most likely caused by an improper tip–sample electrical contact due to a relative fast tip scanning, surface roughness of the sample and/or tip damage, i.e., removal of the conductive coating from the tip.

Unlike the memory-cell structures, measuring write–erase cyclability with C-AFM is highly limited by the tip–sample electrical contact problems. Successive write–erase operations reduce the written mark contrast with its background owing to the wear followed by damage or removal of the conductive tip-coating despite the fact that our measurements were performed at optimum tip–sample contact forces. Indeed, melting damage of the conductive coating, resulting from very high current densities at the tip-edge, was difficult to control. Replacing the damaged tip with a new one did recover the current contrast, but this added the difficulty of relocating the written marks. Despite these practical limitations, we examined the cyclability up to ten times without significant loss of the mark conductivity contrast. In addition, testing the retention time of the data is also limited by several factors, including i) relocating the written mark became difficult after a prolonged period owing the thermal drift; and ii) keeping the sample in air, after writing the marks, for an extended period leads to formation of insulating layers on the sample/tip surfaces. Nevertheless, we succeeded to detect the written marks still after two days, indicating that it is a relatively stable (non-volatile) memory state. Further investigations concentrating on cyclability and data stability (retention times) are in progress. In our recent investigations with simple capacitor-like cells, where the conductive AFM tip is replaced by a static metallic contact, the voltage pulses (of amplitudes ≤ 1.25 V) showed write–erase operations within time scales of microseconds for up to a few hundred cycles. These results will be published in detail elsewhere.[33]

The electrical-resistance switching driven by the polarity of the applied electric field can be related to the solid-state electrolytic behavior of the chalcogenide material. When a solid electrolyte is subjected to an electric field, electrochemical reactions (near the electrodes) lead to ionic conduction. If the electric field strength is sufficiently large, electrically conductive filamentary pathways appear between the electrodes within the electrolyte media leading to a lower-resistance (ON) state. When the polarity of the electric field is reversed, the pre-existing electrical pathways become discontinuous due to ion migration in the opposite direction and lead to a higher-resistance (OFF) state. Figure 5a and b schematically illustrate the formation and rupture, respectively, of such a conducting filaments driven by the polarity of the applied electric field in a solid-state electrolyte.

Systems showing polarity-dependent resistance switching of chalcogenide materials include Ag–S,[14,15] Ag–Ge–Se,[16,17] Ag–Ge–Te,[18] Ag–In–Sb–Te,[19] and Cd–Pb–S.[34] Lower- and higher-resistance states are a result of the formation and rupture of conducting Ag dendrite filaments, respectively, due to ion migrations driven by the electric field. Switching voltages ranged from 0.2 to 6 V, and the resistance difference between ON and OFF states was up to four orders of magnitude. This type of switching has not been observed in Ag-free chalcogenides (e.g., Ge–Sb–Te) used in optical phase-change recording or in the OUM concept. Ag–In–Sb–Te is the only phase-change chalcogenide for which this electrolytic behavior was recently reported.[19] However, this system showed a higher threshold voltage (> 6 V), which is a significant drawback for this material.

A similar electrolytic switching mechanism probably holds for our Sb rich GST chalcogenide material, where conductive Sb instead of Ag filaments can be formed and dissolved in amorphous phase that still persists with a small volume fraction when the GST crystallites are formed. Points in favor of this mechanism are i) (fast) crystallization of this type of material leads, as shown in Ref. [35], to phase separation, where the stoichiometric $Ge_2Sb_2Te_5$ nanocrystals form with the excess Sb as amorphous phase at the grain boundaries; and ii) cross-sectional TEM studies showed that in Ge–Sb–Te films a strong tendency exists to form crystallites near the film sur-

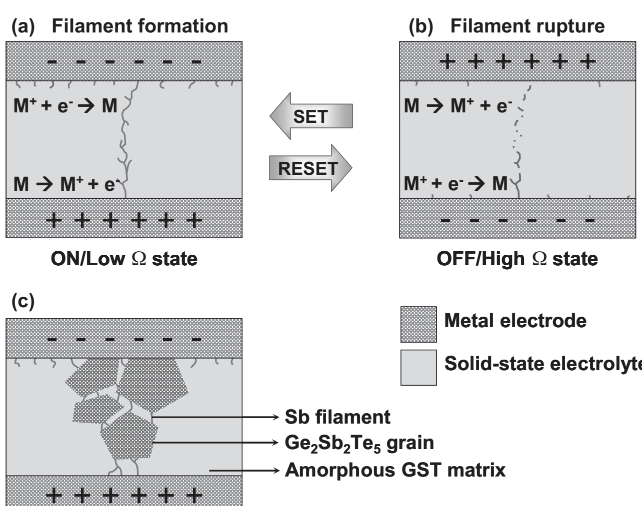

Figure 5. Schematic representation of the polarity-dependent resistance switching mechanism in a solid-state electrolyte. a) Filament formation due to SET operation. During SET operation, metal ions are produced at the bottom (+ ive) electrode and migrate towards the top (– ive) electrode, where the neutral metal atoms accumulate. Due to these solid-state electrochemical reactions, one or more (dendritelike) conductive filamentary pathways form in the solid electrolyte material. This conductive filament formation leads the material to a lower-resistance or ON state. b) Filament rupture due to RESET operation. During the RESET operation, the ions produced at the top (+ ive) electrode start to migrate towards the bottom (– ive) electrode, resulting in rupture of the existing conductive pathway(s), especially to a larger extend near the top electrode. At this stage new dendrites start to grow from the bottom electrode. The filament breakage brings the material into a higher-resistance or OFF state. c) Schematic diagram representing the formation of electrically conductive pathways in Sb rich $Ge_2Sb_{2+x}Te_5$ solid-state electrolyte layer. During SET operation, excess Sb at $Ge_2Sb_2Te_5$ grain boundaries form filaments electrically connecting the grains surrounded by amorphous phase with the electrodes. These Sb filaments remain until they are dissolved by a sufficiently high electric field with a reverse polarity.

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face leaving some amorphous volume near the film-substrate interface.[36,37] Note that (metallic) Sb is also several orders of magnitude more conductive than Ge and Te within the GST system. Therefore, when a sufficiently strong electric field is applied, conducting (dendritelike) Sb filaments form (see Fig. 5c) and can bridge the $Ge_2Sb_2Te_5$ grains through the amorphous matrix with the electrodes. The conducting Sb bridges persist until they are dissolved or ruptured by application of a reverse polarity electric field. Instead of Sb filaments also a similar (electrolytic) mechanism where grain boundaries can switch between a conductive and insulating state can explain the observations. Cross-section TEM studies are in progress to investigate the filament formation or the conductive or insulating grain boundaries in this GST system.

In Ref. [38], it is stated that laser-induced crystallization of a stoichiometric $Ge_2Sb_2Te_5$ film leads to formation of Sb-rich nano-grains with compositions closer to $GeSb_2Te_4$ in a Sb-deficient amorphous matrix. Even though this seems to point against the Sb filament or bridge-formation mechanism, there exist however significant differences in film composition, film thickness and crystallization method when comparing Ref. [38] with our present study. When the starting material is Sb-rich (as in our case), upon crystallization, it is very likely to have stoichiometric $Ge_2Sb_2Te_5$ grains with Sb-rich surroundings as reported in Ref. [35] for a Sb-rich $Ge_2Sb_{2+x}Te_5$ material.

In conclusion, the electrical resistance switching behavior of Sb rich amorphous $Ge_2Sb_{2+x}Te_5$ films is attributed to the solid-state electrolytic (ionic conducting) behavior of the films, where the formation and rupture of electrically conductive Sb bridges between the crystallites and the electrodes are driven by the polarity of the applied electric field. This reversible switching was possible with dc voltages of magnitude ≤ 1.5 V, whereas in our experimental setup, the threshold voltage of the amorphous–crystalline phase transformation is at least 4 V. The ON-state current, which is in the order of few nanoamperes, shows three orders of magnitude contrast with the OFF-state current. No detectable contrast occurred between the OFF state of the crystalline marks and the amorphous surrounding. At present, the write–erase cyclability is limited by various practical factors, but more than ten cycles and two days retention time were at least feasible. We stress that it is shown for the first time that a material from the Ge–Sb–Te family allows resistive memory states that are a combination of the (reversible) structural change and a polarity-dependent resistance change. Therefore, the present findings render powerful opportunities for data storage and data encryption technologies by proper combinations of these two switching concepts in phase-change chalcogenide films.

Experimental

20 or 40 nm thick amorphous $Ge_2Sb_{2+x}Te_5$ films and 100 nm Mo bottom electrode layers were deposited (at room temperature) by employing dc and rf magnetron sputtering techniques, respectively. A digital instruments atomic force microscope (Veeco metrology group, model: Dimension 3100) operating under atmospheric pressure at room temperature was used for write, read, and erase operations. For these operations, a sufficiently good electrical contact between the AFM tip and sample surface was essential. A number of factors affecting the tip–sample electrical contact (e.g., tip–sample contact force, tip scanning speed, wear of the conductive coating on the tip, stiffness of the cantilever, and surface roughness of the sample) were properly optimized. Data writing at the nano- and sub-micrometer scale in our experimental setup (see Fig. 1) was done with pulsed and continuous dc voltages. Write pulses of either polarity generated by a pulse generator were injected via the AFM tip into the electrically grounded sample. Write–erase operations with continuous voltages were performed by biasing the sample with a dc voltage and scanning areas containing the written marks with an electrically grounded AFM tip. Commercially available high-conductive Pt/Ir coated (n-type Sb doped) Si AFM tips were used. The spring constant of the cantilever was ~0.2 N m^{-1} and the initial tip radius of curvature was 20–25 nm. Our experimental setup provides information simultaneously on both the surface topography and electrical conductance of the phase-change layer. The cantilever deflection using a laser and split-photodiode setup gives topographical information. Biasing the sample with smaller dc voltages (well below the threshold limit for crystallization) and measuring the electrical current passing across the thickness of the sample with a conductive AFM tip that is virtually grounded, gives the conductance image. A high-gain current amplifier connected electrically in series with the tip detects currents down to 5 pA. In our experimental setup, scanning the amorphous area with lower dc bias voltages (1–2 V) did not show any significant current flow above this lower limit.

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