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Nanoscale epitaxial lateral overgrowth of GaN-based light-emitting diodes on a SiO_2 nanorod-array patterned sapphire template

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High efficiency GaN-based light-emitting diodes (LEDs) are demonstrated by a nanoscale epitaxial lateral overgrowth (NELO) method on a SiO_2 nanorod-array patterned sapphire substrate (NAPSS). The transmission electron microscopy images suggest that the voids between SiO_2 nanorods and the stacking faults introduced during the NELO of GaN can effectively suppress the threading dislocation density. The output power and external quantum efficiency of the fabricated LED were enhanced by 52% and 56%, respectively, compared to those of a conventional LED. The improvements originated from both the enhanced light extraction assisted by the NAPSS and the reduced dislocation densities using the NELO method. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2969062]

High-brightness GaN-based light-emitting diodes (LEDs) in the UV/blue/green wavelength range have been under immense demand for a variety of applications, including large full-color displays, short-haul optical communications, traffic and signal lights, backlights for liquid-crystal displays, and general lightings.[1] To address the next-generation applications in projectors, automobile headlights, and high-end general lightings, further improvements on the optical power and the external quantum efficiency (EQE) are required. The development of GaN-based LEDs has shown significant progress over the past decade, in particular, the metal-organic chemical vapor deposition (MOCVD) growth of GaN on lattice-mismatched sapphire substrates.[2,3] It has been shown that the epitaxial lateral overgrowth (ELO) method with a microscale SiN_x or SiO_x patterned mask on as-grown GaN seed crystals can effectively reduce the threading dislocation density (TDD).[4–6] However, the requirements of the two-step growth procedure and a sufficient thickness for GaN coalescence are costly and time consuming. Moreover, high quality GaN-based LEDs have been demonstrated on a microscale patterned sapphire substrate (PSS) by wet etching,[7] where the microscale patterns served as a template for the ELO of GaN and the scattering centers for the guided light. Both the epitaxial crystal quality and the light extraction efficiency were improved by utilizing a microscale PSS. Recently, the MOCVD growth of InGaN/GaN LEDs on the PSSs with microscale and nanoscale pyramidal patterns has been reported and compared.[8] The LEDs grown on the nanoscale PSS showed more enhancement in the EQE than those grown on the microscale PSS. However, the fabrication of nanoscale PSSs generally required electron-beam lithography[9] or nanoimprinting techniques,[10] making it unfavorable for mass production. In this letter, we report a relatively simple technique to fabricate a SiO_2 nanorod-array PSS (NAPSS), serving as a template for the nanoscale ELO (NELO) of GaN by MOCVD to produce high efficiency GaN-based LEDs. The transmission electron microscopy (TEM) images showed that the TDD was significantly reduced by the voids between SiO_2 nanorods and the stacking faults introduced during the NELO. Moreover, the NAPSS LEDs demonstrated an enhanced EQE and light-output power compared to a conventional LED epitaxially grown on a flat sapphire substrate.

The GaN-based LEDs used in this study were grown on a 2 in. SiO_2 NAPSS using a low-pressure MOCVD system (Aixtron 2400 G). The preparation of the SiO_2 NAPSS template started with the deposition of a 200-nm-thick SiO_2 layer on a *c*-face (0001) sapphire substrate by plasma enhanced chemical vapor deposition, followed by the evaporation of a 10-nm-thick Ni layer, and the subsequent rapid thermal annealing with a flowing nitrogen gas at 850 °C for 1 min. The resulting self-assembled Ni clusters then served as the etch masks to form a SiO_2 nanorod array using a reactive ion etch system for 3 min. Finally, the sample was dipped into a heated nitric acid solution (HNO_3) at 100 °C for 5 min to remove the residual Ni masks. As shown in Fig. 1(a), the field-emission scanning electron micrograph (FESEM) indicated that the fabricated SiO_2 nanorods were approximately 100–150 nm in diameter with a density of 3×10^9 cm^{-2}. The spacing between nanorods was about 100–200 nm. Figure 1(a) also shows that the exposed sapphire surface was flat enough for epitaxy. As the deposition process began, localized and hexagonal islandlike GaN nuclei were first formed from the sapphire surface to initiate GaN overgrowth, as shown in Fig. 1(b). Figure 1(c) shows the cross-sectional FESEM image of the GaN epilayer, where voids with a size varying from 150 to 200 nm were observed between the highlighted SiO_2 nanorods. The existing of the voids between nanorods observed from the micrographs suggested that not all the exposed surface enjoyed the same growth rate. Hence, only the regions with higher growth rates, which might be originated from larger exposed surface,

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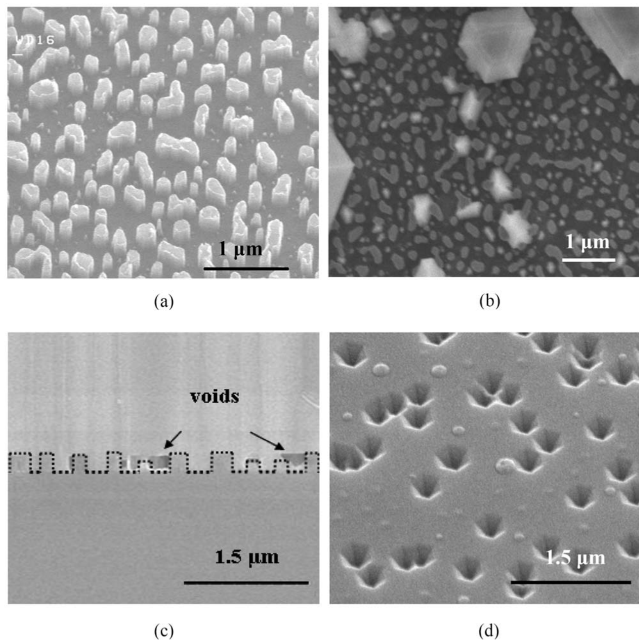

FIG. 1. FESEMs of (a) the fabricated SiO_2 nanorod array, (b) GaN nuclei on the SiO_2 NAPSS as growth seeds, (c) the GaN epilayer on a NAPSS in the cross-sectional view, and (d) the epitaxial pits on the *p*-GaN surface.

could play the role of a seed layer, facilitating the lateral coalescence of GaN. Lastly, the growth of a conventional LED structure, which consists of ten periods of InGaN/GaN multiple quantum wells and a 100-nm-thick *p*-GaN layer, was completed by MOCVD. The *p*-GaN layer of the NAPSS LED was grown at the relatively low temperature of 800 °C, leading to the formation of hexagonal pits due to insufficient migration length of Ga atoms.[11] The FESEM image of the roughened *p*-GaN surface with randomly distributed pits is shown in Fig. 1(d).

The TEM was employed to investigate the crystalline quality of GaN layers epitaxially grown on a planar sapphire substrate and on a NAPSS. As shown in Fig. 2(a), the TDD of GaN on the planar sapphire substrate was higher than 10^{10} cm^{-2} due to both the large lattice mismatch (13%) and the high thermal coefficient incompatibility (62%) between sapphire and GaN. On the other hand, the crystalline quality of GaN epilayer on a NAPSS was drastically improved from that grown on a planar sapphire substrate, as shown in Fig. 2(b). We found that a number of stacking faults often occurred above the voids between SiO_2 nanorods, where visible threading dislocations (TDs) were rarely observed in the vicinities. It is believed that the presence of stacking faults could block the propagation of TDs.[12] Moreover, the TDs of the GaN layer on a NAPSS mainly originated from exposed sapphire surface, which could be bent due to the lateral growth of GaN. The inset of Fig. 2(b) shows the TEM image of the dislocation bending with visible turning points. We summarized four potential mechanisms that were involved in the suppression of TDD, denoted as Types 1–4 and illustrated in Fig. 3.

As shown in Fig. 3(a), the TDs originated from the sapphire surface during the initial formation GaN growth seeds on a NAPSS. The presence of voids confirmed the lateral coalescence of GaN, leading to the bending of dislocations near the edge of SiO_2 nanorods. The bent TD eventually developed into stacking faults,[7] as depicted by Type 1 in Fig.

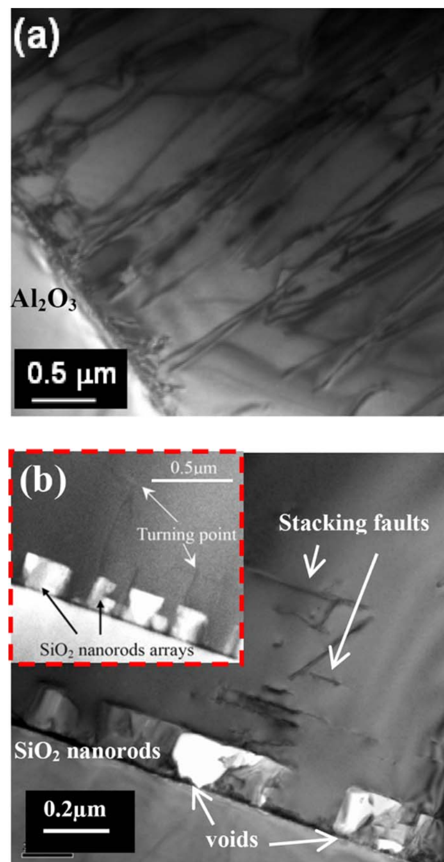

FIG. 2. (Color online) The TEM images of the GaN/sapphire interface for the GaN epilayer grown on (a) a planar sapphire substrate and (b) on a NAPSS. The inset of (b) shows the dislocation bending phenomenon with visible turning points.

3(b). Moreover, the coalescence fronts of GaN seeds provided a strain release layer where stacking faults could occur. These stacking faults were found mostly above the voids or the small GaN seeds,[13] blocking the TD propagation, denoted as Type 2. Occasionally, the blocked dislocation might also be bent to form stacking faults.[14] If the growth rate was too slow to be a GaN seed, the dislocation could be blocked by the formation of voids, as illustrated by Type 3. Finally, we believed that the residual SiO_2 between nanorods could prohibit the GaN growth and further reduce the dislocation formation from sapphire surface, as depicted by Type 4. It is also worth noting that the density of voids in the SiO_2 NAPSS was higher than that of a microscale PSS. Therefore,

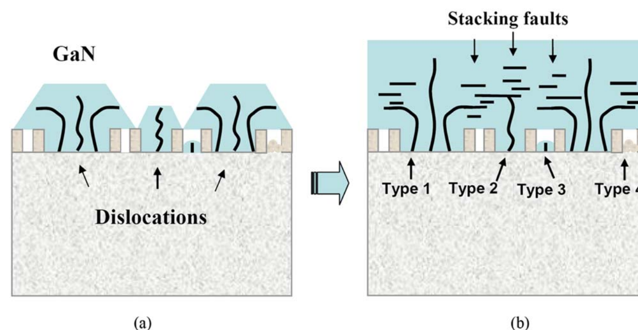

FIG. 3. (Color online) The schematics of (a) the overgrowth process and the formation of dislocations, stacking faults, and voids at the initial stage of epitaxy, and (b) four potential mechanisms accounted for the reduction of the TDD.

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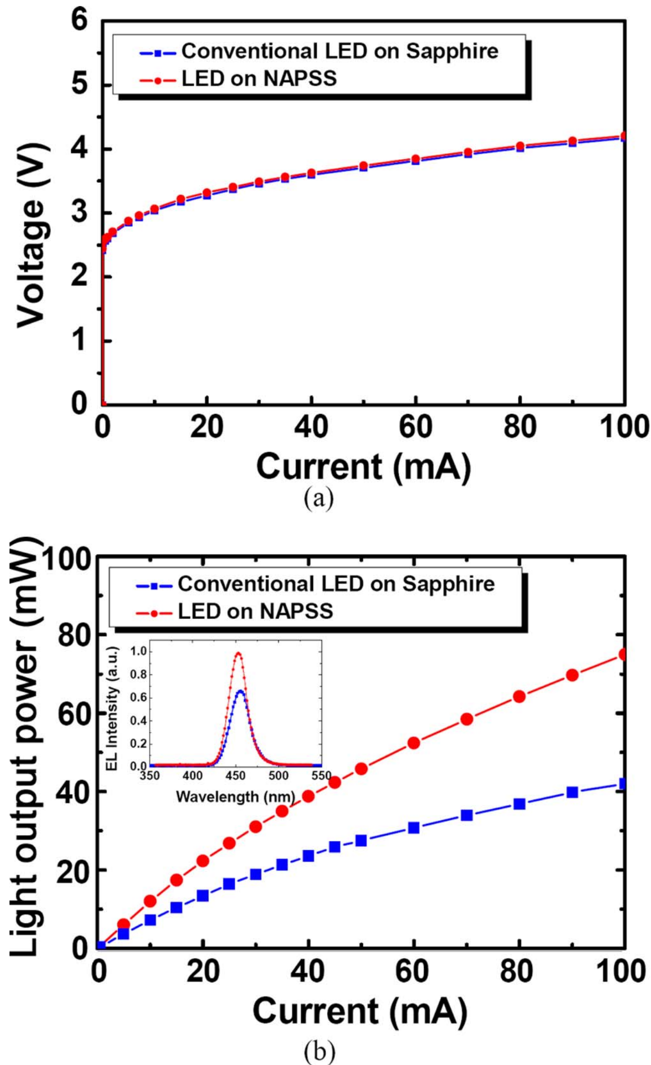

FIG. 4. (Color online) Electrical and optical properties of a NAPSS and a conventional LED: (a) the current-voltage (*I-V*) curves, where the inset shows a schematic of a NAPSS LED, and (b) the current-output power (*L-I*) curves, where the inset shows the electroluminescence spectra for both devices at a driving current of 20 mA.

we believe that the formation of stacking faults and voids were involved in the reduction and bending of dislocations.

The completed epitaxial structure then underwent a standard four-mask LED fabrication process with a chip size of $350 \times 350\ \mu m^2$ and packaged into TO-18 with epoxy resin on top. The schematic of a fabricated NAPSS LED is shown in the inset of Fig. 4(a). The current-voltage (*I-V*) characteristics of the NAPSS LED and a conventional LED with the same chip size were measured at room temperature, as shown in Fig. 4(a). The forward voltages at 20 mA were 3.27 V for the conventional LED and 3.31 V for the NAPSS LED. The nearly identical *I-V* curves indicate that the nanoscale roughness on the *p*-GaN surface had little impact on the *I-V* characteristics. Moreover, the NELO of GaN did not deteriorate the electrical properties.

Figure 4(b) shows the measured light-output power versus the forward continuous dc current (*L-I*) for the NAPSS and conventional LED. At an injection current of 20 mA, the light-output powers were approximately 22 and 14 mW for the NAPSS and the conventional LEDs, respectively. The output power of the NAPSS LED was enhanced by a factor of 52% compared to that of the conventional LED. The inset shows the normalized electroluminescence spectra for both devices at an injection current of 20 mA. A minor wavelength blueshift of ~2 nm was observed for the NAPSS LED, attributed to the partial strain release by adopting the NELO scheme.[15] The EQE of the NAPSS LED was calculated to be ~40.2%, which is an increase of 56% when compared to that of the conventional LED, ~25.7%. We believe that the 56% enhancement in EQE originated from the improved internal quantum efficiency and the enhanced extraction efficiency. The SiO_2 NAPSS-assisted NELO method effectively suppressed the dislocation densities of GaN-based LEDs, which increased the internal quantum efficiency. Moreover, the embedded SiO_2 nanorods in the GaN epilayer contributed to light extraction due to scattering at the interfaces of different refractive indices. Ueda *et al.*[16] reported that the output power linearly increased with the surface coverage ratio of nanosilica spheres. Therefore, the extraction efficiency was enhanced by the SiO_2 nanorod array.

In summary, this work introduced the SiO_2 NAPSS-assisted NELO method suitable for the MOCVD growth of the next-generation high-brightness blue LEDs. The NAPSS LED demonstrated an enhanced EQE and light-output power when compared to a conventional LED. The TDD reduction in GAN-based epilayers was realized by the SiO_2 NAPSS-assisted NELO method, where four potential TD reduction mechanisms were identified.

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