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Nanoscale Memristor Device as Synapse in Neuromorphic Systems

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ABSTRACT A memristor is a two-terminal electronic device whose conductance can be precisely modulated by charge or flux through it. Here we experimentally demonstrate a nanoscale silicon-based memristor device and show that a hybrid system composed of complementary metal−oxide semiconductor neurons and memristor synapses can support important synaptic functions such as spike timing dependent plasticity. Using memristors as synapses in neuromorphic circuits can potentially offer both high connectivity and high density required for efficient computing.

KEYWORDS Nanoelectronics, neuromorphic system, memristor, synaptic adaptation, spike-timing dependent plasticity

The sequential processing of fetch, decode, and execution of instructions through the classical von Neumann bottleneck of conventional digital computers has resulted in less efficient machines as their eco-systems have grown to be increasingly complex. Though the current digital computers can now possess the computing speed and complexity to emulate the brain functionality of animals like a spider, mouse, and cat,[1−4] the associated energy dissipation in the system grows exponentially along the hierarchy of animal intelligence. For example, to perform certain cortical simulations at the cat scale even at 83 times slower firing rate, the IBM team in ref 2 has to employ Blue Gene/P (BG/P), a super computer equipped with 147 456 CPUs and 144 TB of main memory. On the other hand, brains of biological creatures are configured dramatically differently from the von Neumann digital architecture. The key to the high efficiency of biological systems is the large connectivity ($\sim 10^4$ in a mammalian cortex) between neurons that offers highly parallel processing power.[5] The synaptic weight between two neurons can be precisely adjusted by the ionic flow through them and it is widely believed that the adaptation of synaptic weights enables the biological systems to learn and function.[1,4,6−9]

A synapse is essentially a two-terminal device and bears striking resemblance to an electrical device termed memristor[10,11] (memory + resistor). Similar to a biological synapse, the conductance of a memristor can be incrementally modified by controlling charge or flux through it. In this study we demonstrate the experimental implementation of synaptic functions in nanoscale silicon-based memristors. In particular we verify that STDP, an important synaptic modification rule for competitive Hebbian learning,[6−8] can be achieved in a hybrid synapse/neuron circuit composed of complementary metal−oxide semiconductor (CMOS) neurons and nanoscale memristor synapses (Figure 1a). These demonstrations provide the direct experimental support for the recently proposed memristor-based neuromorphic systems.[12,13] For example, in a crossbar hardware structure schematically shown in Figure 1b, a two-terminal memristor synapse is formed at each crosspoint and connects CMOS-based pre- and postsynaptic neurons. The hybrid memristor/CMOS circuits discussed here can be fabricated using similar techniques developed recently for memristor-based memory and logic.[14] The crossbar synapse network can potentially offer connectivity and function density comparable to those of biological systems and operate in a way analogous to biological systems rather than digital computers.[12,15] In this case, every CMOS neuron in the "pre-neuron" layer of the crossbar configuration is directly connected to every neuron in "post-neuron" layer with unique synaptic weights. A high synaptic density of $10^{10}/cm^2$ can also be potentially obtained for crossbar networks with 100 nm pitch, a feature size readily achievable with advanced lithography approaches.[16,17]

The memristor in our setup consists of a layered device structure including a cosputtered Ag and Si active layer with a properly designed Ag/Si mixture ratio gradient that leads to the formation of a Ag-rich (high conductivity) region and a Ag-poor (low conductivity) region (Figure 1a, inset) (Supporting Information). Typically, resistance switching devices regardless of switching material being used require an electroforming process during which metal ions or particles are injected into and cause semipermanent structural modifications inside the otherwise insulating storage medium. The forming process creates localized conducting paths (filaments) whose motion results in discrete, abrupt resistance switching characteristics.[18−23] By cosputtering Ag and Si, nanoscale Ag particles are incorporated into the Si medium during device fabrication and a uniform conduction

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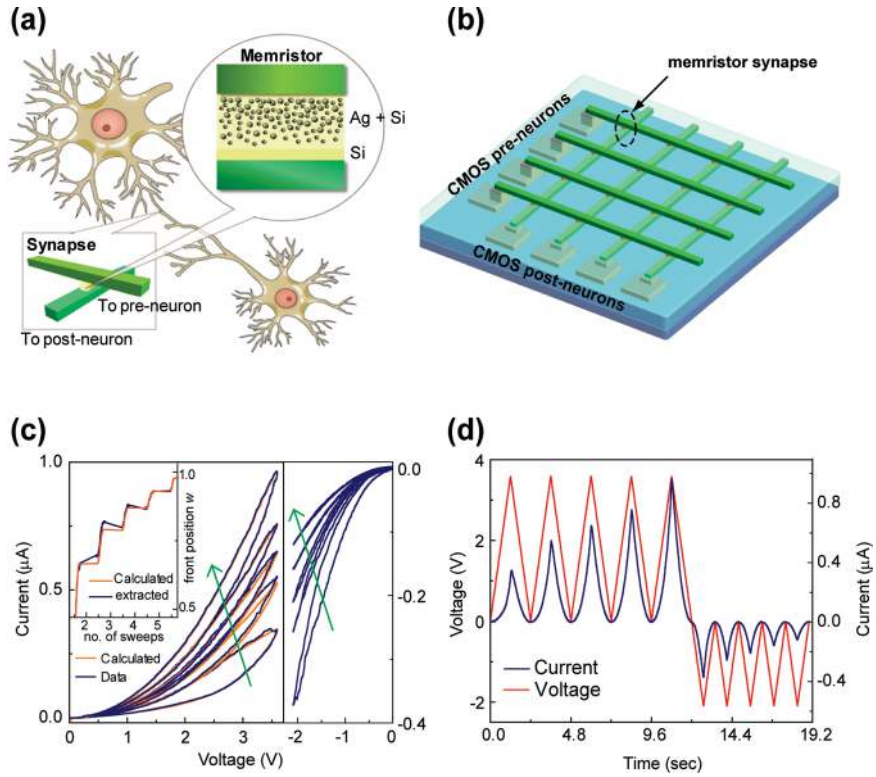

FIGURE 1. Nanoscale memristor characteristics and its application as a synapse. (a) Schematic illustration of the concept of using memristors as synapses between neurons. The insets show the schematics of the two-terminal device geometry and the layered structure of the memristor. (b) Schematic of a neuromorphic with CMOS neurons and memristor synapses in a crossbar configuration. (c) Measured (blue lines) and calculated (orange lines) $I-V$ characteristics of the memristor. Inset: calculated (orange lines) and extracted (blue lines) values of the normalized Ag front position w during positive DC sweeps. (d) The current and voltage data versus time for the device in (c) highlighting the change in current in sequential voltage sweeps.

front between the Ag-rich and Ag-poor regions can be formed. As a result, the forming process can be eliminated. In addition, under applied bias the continuous motion of the conduction front in the cosputtered memristor device replaces discrete, localized conducting filament formation[22] and results in reliable "analog" switching behaviors (Figure 1c).

Figure 1c shows the measured device current $i(t)$ (blue lines) as a function of the applied voltage across the memristor $v(t)$ for five consecutive positive voltage sweeps and five consecutive negative voltage sweeps. Distinct from devices that show abrupt conductance jumps,[18−23] here the conductance continuously increases (decreases) during the positive (negative) voltage sweeps, and the $I-V$ slope of each subsequent sweep picks up where the last sweep left off. In fact, the device $I-V$ can be well fitted by a simple memristor circuit model[11] (orange lines, Figure 1c)

$$i(t) = \frac{1}{R_{ON}w(t) + R_{OFF}(1 - w(t))}v(t) \qquad (1)$$

Here $w(t)$ stands for the normalized position of the conduction front between the Ag-rich and Ag-poor regions within the active device layer and has the value between 0 and 1. Upon the application of a positive voltage bias, Ag ions move from the Ag-rich region to the Ag-poor region and increases w, and vice versa. As w(t) approaches to 0(1), the device reaches the lowest (highest) conductance state with resistance of R_{OFF} (R_{ON}). In this model we further assumed the position $w(t)$ is a linear function of the flux-linkage $\varphi(t) = \int v(t)dt$ through the device. Equation 1 can then be rewritten as

$$i(t) = G(\varphi(t))v(t) \qquad (2)$$

This is the equation for a flux-controlled memristor[10] and $G(\varphi(t))$ is the so-called memductance. In addition, for the devices studied here bias voltages with amplitude $< V_T = 2.2$ V are not sufficient to drive the Ag ions inside the a-Si matrix and have negligible effect on the memristor resistance. The threshold effect and the value of the threshold voltage V_T have been consistently obtained in all the devices tested in this study.

The calculated current values during the voltage sweeps based on the memristor model discussed above were shown as orange lines in Figure 1c together with the measured current (blue lines). The inset to Figure 1c shows the values

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of $w(t)$ (orange lines) used to calculate the current during the five consecutive positive voltage sweeps by assuming $w(t)$ to be a linear function of the flux-linkage φ. In addition, the values of $w(t)$ can also be directly extracted from the data using eq 1 and are shown in the inset to Figure 1c as the blue lines. The relative good agreements between the calculated and the measured values in $i(t)$ and $w(t)$ verify that the device characteristics above the threshold voltage can indeed be explained by the memristor-model using eqs 1 and 2, where the front position is roughly a linear function of the flux-linkage $\varphi(t) = \int v(t)\mathrm{d}t$. However, strictly speaking the device is not a true memristor due to the threshold effect but falls in the more broadly defined memristive device category.[24] On the other hand, the threshold effect makes it possible to perform nondisturbing read of the device state by using read pulses with $V_{\mathrm{read}} < V_{\mathrm{T}}$ and can in fact be beneficial in practical applications.

The flux-controlled memristor model suggests that the device conductance (memductance) can be incrementally adjusted by tuning the duration and sequence of the applied programming voltage. Figure 2a shows the results when the device was programmed by a series of 100 identical positive (3.2 V, 300 μs) pulses followed by a series of 100 identical negative voltage pulses (−2.8 V, 300 μs). The device conductance (represented by the measured current at a small read voltage of 1 V) was measured after each programming pulse. As expected from the DC characteristics of the device, the application of positive potentiating voltage pulses (P) incrementally increases the memristor conductance, and the application of negative depressing voltage pulses (D) incrementally decreases the memristor conductance. We note that unlike results from devices with abrupt switching characteristics where the programming signals control the final device state,[22] here the flux-linkage $\varphi(t)$ during each programming pulse controls the relative change of the memristor conductance. This effect was further demonstrated in Figure 2b. Here mixed positive (P) and negative (D) voltage pulses with constant pulse height but different pulse widths were applied to the device and the change in memristor conductance ΔG were measured and recorded after each P/D pulse. A clear correlation between ΔG and the pulse width of the applied P/D signals was observed; the application of a longer positive (negative) pulse resulted in a larger increase (decrease) of memristor conductance, and vice versa.

These results suggest the memristor devices are capable to emulate the biological synapses with properly designed CMOS neuron components to provide local programming voltages with controlled pulse width and height. For example, to demonstrate advanced synaptic functions such as STDP, an important synaptic adaptation rule for competitive Hebbian learning that demands the change of synaptic weight to be a strong function of the timing of the pre/postneuron spikes,[6−8] we have implemented a CMOS neuron circuit to convert the relative timing information of the

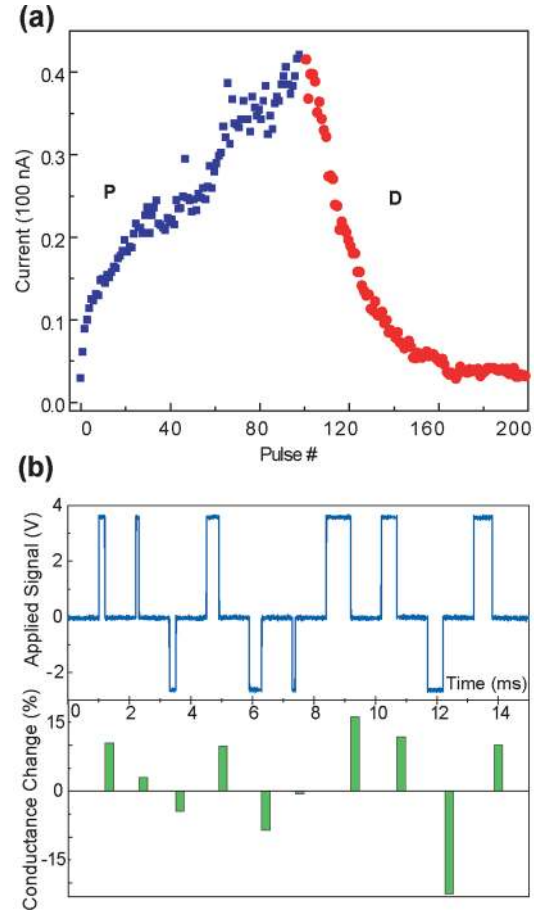

FIGURE 2. Memristor response to programming pulses. (a) The device conductance can be incrementally increased or decreased by consecutive potentiating or depressing pulses. The conductance was measured at 1 V after each pulse and the read current is plotted. P, 3.2 V, 300 μs; D, −2.8 V, 300 μs. (b) (Top) Mixed potentiating and depressing pulses with different pulse widths that are used to program the memristor. (Bottom) Measured change of the memristor conductance after the application of each pulse. The conductance change was normalized to the maximum memristor conductance.

neuron spikes into pulse width information seen by the memristor synapse (Supporting Information). Briefly, the neuron circuit consists of two CMOS based integrate-and-fire neurons[25] connected by a nanoscale memristor with active device area of 100 nm × 100 nm. The neuron circuit involves a mixed analog-digital design and employs a time division multiplexing (TDM) approach with globally synchronized time frames to convert the timing information into a pulse width.[12] Specifically, the neuron circuit generates a potentiating (depressing) pulse across the memristor synapse when the presynaptic neuron spikes before (after) the postsynaptic neuron, with the pulse width being an exponentially decaying function of the relative neuron spike timing $\Delta t = t_{\mathrm{pre}} - t_{\mathrm{post}}$, where t_{pre} (t_{post}) is the time when the presynaptic neuron (postsynaptic neuron) spikes (Supporting Information).

Figure 3a shows the measured change of the memristor synaptic weight after each neuron spiking event obtained in the hybrid CMOS-neuron/memristor-synapse circuit. When

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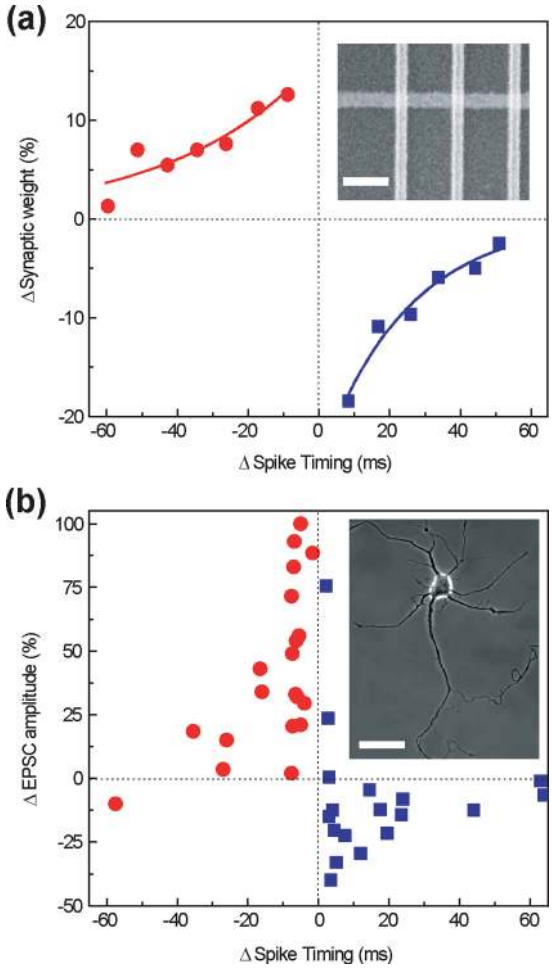

FIGURE 3. Demonstration of STDP in the memristor synapse. (a) The measured change of the memristor synaptic weight vs the relative timing Δt of the neuron spikes. The synaptic change was normalized to the maximum synaptic weight. Inset: scanning-electron microscope image of a fabricated memristor crossbar array. Scale bar: 300 nm. (b) The measured change in excitatory postsynaptic current (EPSC) of rat hippocampal neurons after repetitive correlated spiking (60 pulses at 1 Hz) vs relative spike timing. The figure was reconstructed with permission from ref 8. Inset: A phase contrast image of a hippocampal neuron. Scale bar: 50 μm. The image was adapted with permission from ref 26.

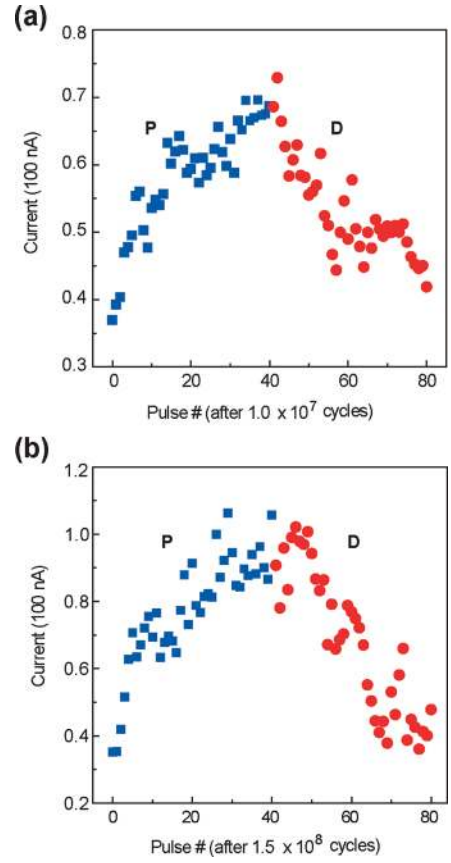

FIGURE 4. Response of the memristor device after repeated potentiating (P) and depressing (D) pulses. (a) After 1.0×10^7 P/D pulses. (b) After 1.5×10^8 P/D pulses. In each test, 3.1 V, 800 μs potentiating pulses, -2.9 V, 800 μs depressing pulses, and 1 V, 2 ms read pulses were used. After each programming pulse, the device conductance was measured by a read pulse and recorded.

the preneuron spikes before (after) the postneuron, the memristor synaptic weight increases (decreases). In addition, the change in the synaptic weight versus the spike timing difference Δt can be well fitted with exponential decay functions, verifying that STDP characteristics similar to that of biological synaptic systems (e.g., Figure 3b) can indeed be obtained in memristor synapses.[7,8]

Finally, in Figure 4 we plot P/D response of the device after continuous applications of the potentiation and depression pulses. As shown in Figure 4b, up to 1.5×10^8 times of P/D conductance modulation can be achieved before the device shows significant degradation. Assuming the synapses are updated at a rate of 1 Hz,[27,28] this endurance corresponds to ~5 years of continuous synaptic operation. These demonstrations together with the large connectivity and density offered by the two-terminal memristor synapses in the crossbar configuration (e.g., Figure 1b) make the hybrid CMOS-neuron/memristor-synapse approach promising for hardware implementation of biology-inspired neuromorphic systems.

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Supporting Information Available. Fabrication of the memristor devices. Design and characterization of the neuron circuit. Device response after 5.0×10^5 and 1.0×10^6 P/D pulses. This material is available free of charge via the Internet at http://pubs.acs.org.

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