Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel

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***Abstract*—We report the concept and demonstration of a nanoscale ultra-thin-body silicon-on-insulator (SOI) P-channel MOSFET with a $Si_{1-x}Ge_x$/Si heterostructure channel. First, a novel lateral solid-phase epitaxy process is employed to form an ultra-thin-body that suppresses the short-channel effects. Negligible threshold voltage roll-off is observed down to a channel length of 50 nm. Second, a selective silicon implant that breaks up the interfacial oxide is shown to facilitate unilateral crystallization to form a single crystalline channel. Third, the incorporation of SiGe in the channel resulted in a 70% enhancement in the drive current.**

***Index Terms*—Heterojunctions, MOSFET's, SiGe, silicon-on-insulator technology, solid-phase epitaxy, ultra-thin-body.**

I. Introduction

DEVICE scaling has been successfully applied over many CMOS technology generations, resulting in consistent improvement in both device density and performance. However, new challenges are encountered in the scaling of conventional MOSFET structures much below 100 nm. The high channel doping concentration required to suppress the short-channel effect (SCE) results in degraded mobility and enhanced junction leakage. The ultra-thin-body silicon-on-insulator (SOI) MOSFET is a promising structure that suppresses SCE without using a heavily doped channel [1], [2]. With an undoped or lightly doped channel, it also avoids the fluctuation of threshold voltage (V_{TH}) due to random fluctuations of the number of dopant atoms in the channel region of nanoscale MOSFET's [3]. Another attractive approach to improving CMOS performance exploits the strain- or band-structure-induced mobility enhancement to increase the drive current. One of the most notable effects is the enhanced hole mobility in silicon germanium (SiGe) under biaxial compressive strain [4]–[7]. In the sub-100 nm regime, a device that combines the advantages of the SiGe/Si heterostructure and an ultra-thin-body could be the device structure of choice. In this letter, we report the concept and demonstration of nanoscale ultra-thin-body SOI P-channel MOSFET's and show the enhancement in drive current due to the incorporation of SiGe in the channel.

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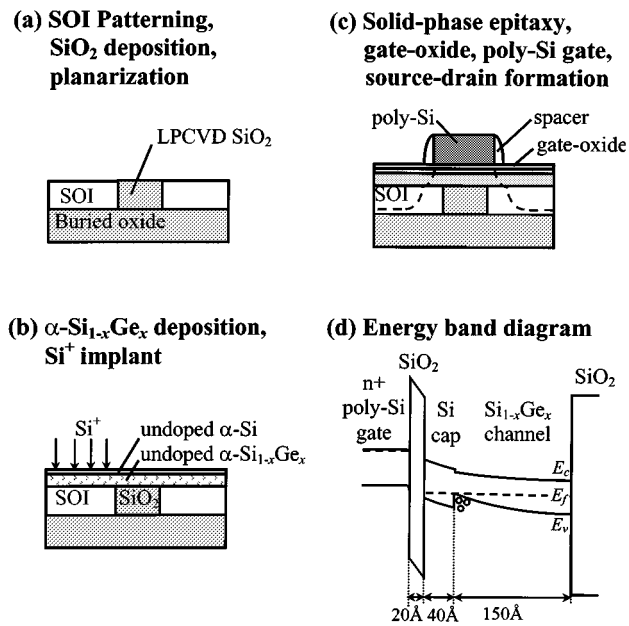

Fig. 1. Process flow for the SiGe-channel ultra-thin body solid-phase epitaxy MOSFET (SPEFET). The energy band diagram through the SiGe/Si film in Fig. 1(d) shows that the hole inversion layer is formed in the SiGe at the interface with the cap Si.

II. Device Fabrication

An ultra-thin-body SOI MOSFET has a body thickness that is less than two or even one hundred angstroms. Etch-back or oxidation-thinning processes may be incapable of producing a uniform body thickness since this is limited by the thickness uniformity of the starting thick SOI layer. To provide adequate thickness uniformity, a deposited channel film is more desirable.

MOSFET's with gate length down to 50 nm were fabricated on SmartCut™ wafers which had a 50 nm thick SOI layer and a 400 nm buried oxide. The SOI layer was etched away completely except for regions which were to become the thick source and drain islands. The trench between the source and drain islands, which is about 20 nm shorter than the channel length, was filled with SiO_2 using low-pressure chemical-vapor deposition (LPCVD) and planarized to give the structure shown in Fig. 1(a). 150 Å of undoped amorphous $Si_{1-x}Ge_x$ (graded from $x = 0$ to $x = 0.3$ from bottom to top) and 50 Å of undoped amorphous-Si (α-Si) were deposited at 425 °C using LPCVD to form a heterogeneous amorphous film connecting the source and drain islands. On the control wafers, 200 Å of undoped α-Si was deposited instead of the SiGe/Si stack to obtain a pure-Si channel. This was followed by a masked or unmasked 20 keV

Si implant with a dose of 7×10^{15} cm^{-2} to break up the interfacial oxide over the source island or over both the source and drain islands, respectively [Fig. 1(b)]. This implant facilitates the crystallization of the amorphous film with the SOI island(s) as the seed. The crystallization step, performed at 550 °C for 12 hr, results in lateral solid-phase epitaxy (SPE) growth to form the channel. The range of the lateral SPE is about 0.25 μm. After 20 Å gate oxide growth and *in-situ* n+ poly-silicon gate deposition, the gate was patterned using electron- beam lithography, and the self-aligned source and drain regions formed by ion implantation [Fig. 1(c)]. Finally, contact-hole etch, metal deposition, and metal patterning steps were performed to complete the device. This device structure is called the SPE MOSFET (SPEFET) [2]. The energy-band diagram of the SiGe-channel SPEFET is shown in Fig. 1(d). The top Si cap layer has a thickness of 40 Å after gate oxide growth. It serves to provide a good Si/SiO_2 interface quality. Nearly all of the band-gap difference between $Si_{0.7}Ge_{0.3}$ and Si appears at the valence band. As a result, the majority of the holes in P-SPEFET's are confined in the SiGe-channel, not at the Si/SiO_2 interface.

III. Characterization and Discussion of Results

In Fig. 2, the drain current of the SiGe-channel and the Si-channel P-SPEFET's are compared. These devices had SPE seeding at the source side only. An enhancement of 70% in the current drive is observed at $V_{\rm DS} = -1.5$ V, $V_{\rm GS} - V_{\rm TH} = -1.2$ V in the SiGe P-SPEFET's. We believe this is due to the lower effective mass of holes in $Si_{0.7}Ge_{0.3}$ which could account for a 20% enhancement and probably the existence of biaxial compressive strain in the channel which lifts the degeneracy of the light-hole (LH) and heavy-hole (HH) bands at the Γ point, leading to an even lower in-plane effective mass of the topmost HH band [4], [5]. One speculation on how strain could be incorporated in the SiGe-channel is that the elongated lattice constant of SiGe in the vertical direction gets transferred laterally to the channel region during the SPE growth. Comparable drive currents for the SiGe-channel and Si-channel N-SPEFET's are observed, and this is expected since the peak electron concentration in the SiGe-channel N-SPEFET biased into inversion is in the unstrained Si cap layer where electron mobility is not enhanced. $I_{\rm DS}$ is low probably due to a large series resistance and further process optimization is needed.

With an unmasked Si implant, the SPE growth proceeds from both ends of the channel and the two growth fronts meet near the middle of the channel, resulting in a low angle grain boundary. With the implant masked such that native oxide is broken up only on one side, crystallization proceeds from one side only, so that the grain boundary in the channel is eliminated at the cost of an additional lithography step. In Fig. 3, the effects of one- and two-sided crystallization on the $I_{\rm DS}$-$V_{\rm DS}$ characteristics of the SiGe-channel P-SPEFET's are shown. The elimination of the grain boundary is seen to give about 80% improvement in the drive current at $V_{\rm DS} = -1.5$ V, $V_{\rm GS} - V_{\rm TH} = -1.2$ V. The $I_{\rm DS}$-$V_{\rm GS}$ characteristics are plotted in Fig. 4 to show the good turn-off behavior of the devices that used one-sided crystallization. Fig. 5 illustrates the excellent short-channel effect of the ultra-thin-body devices. Fig. 4 and 5 also show that the grain boundary not only increases the threshold voltage and subthreshold swing probably due to the high trap-state density at the grain boundary, but also causes a wider distribution of the $V_{\rm TH}$ values. Fig. 5 also shows that the Si-channel device has 0.2

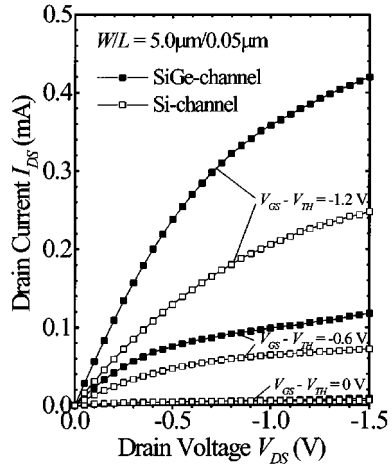

Fig. 2. SiGe P-SPEFET has 70% larger $I_{\rm DS}$ than the Si SPEFET due to the higher hole mobility in the SiGe channel.

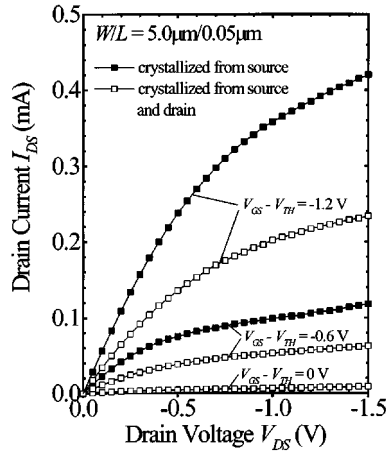

Fig. 3. $I_{\rm DS}$ is 80% higher in the SiGe P-SPEFET with the channel laterally crystallized from the source than from both the source and drain.

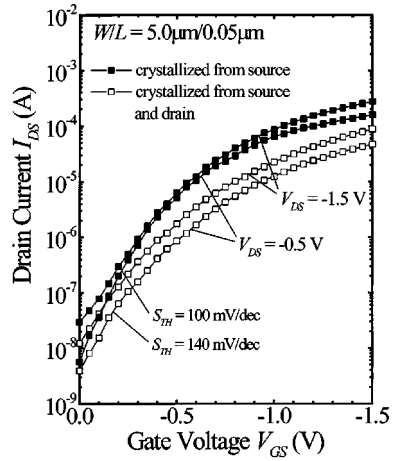

Fig. 4. SiGe P-SPEFET with SPE seeding at the source only shows better turn-off characteristics.

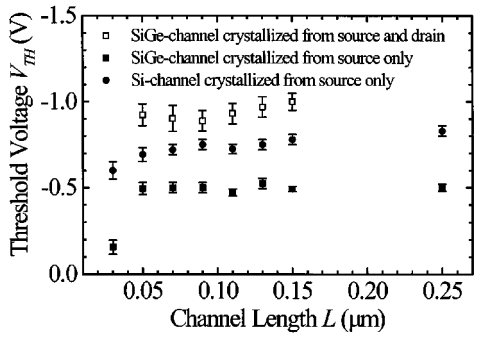

Fig. 5. All ultra-thin-body SiGe SPEFET's show little V_{TH} roll-off down to $L = 0.05$ μm. Both the existence of a grain boundary in the channels due to seeding at source and drain and the larger band-gap in Si-channel device yield high V_{TH} as expected.

V higher V_{TH} than the SiGe-channel device. This is consistent with the valence band offset between Si and $Si_{0.7}Ge_{0.3}$.

IV. Conclusion

In conclusion, we have demonstrated the shortest channel-length (50 nm) SiGe-channel heterostructure MOSFET reported to date. The device has a novel structure that employs an undoped ultra-thin-body on a SOI substrate to suppress the short-channel effects. The thin body is fabricated by lateral SPE which also provides a convenient way to produce the SiGe/Si heterostructure. A 70% enhancement in the drive current is observed due to the introduction of $Si_{0.7}Ge_{0.3}$ in the channel. A masked interfacial oxide break-up implant is shown to facilitate unilateral crystallization to eliminate the grain boundary from the channel.

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