Nanosecond Delay Floating High Voltage Level Shifters in a 0.35 μm HV-CMOS Technology

Yashodhan Moghe, Torsten Lehmann, *Senior Member, IEEE*, and Tim Piessens, *Member, IEEE*

***Abstract*—We present novel circuits for high-voltage digital level shifting with zero static power consumption. The conventional topology is analysed, showing the strong dependence of speed and dynamic power on circuit area. Novel techniques are shown to circumvent this and speed up the operation of the conventional level-shifter architecture by a factor of 5–10 typically and 30–190 in the worst case. In addition, these circuits use 50% less silicon area and exhibit a factor of 20–80 lower dynamic power consumption typically. Design guidelines and equations are given to make the design robust over process corners, ensuring good production yield. The circuits were fabricated in a 0.35 μm high-voltage CMOS process and verified. Due to power and IO speed limitation on the test chip, a special ring oscillator and divider structure was used to measure inherent circuit speed.**

***Index Terms*—CMOS, DMOS, fast, floating, high speed, high voltage, high-speed, high-voltage, HV, HV CMOS, HV-CMOS, HVCMOS, level shifter, level-shifter, low power, low-power, reduced area, ultra fast, ultra-fast.**

I. Introduction

MODERN CMOS triple-well processes offer HV extensions via special DMOS or drain-extended MOS (hereafter simply referred to as DMOS) transistors and N-wells that can float up to high voltages above the chip substrate. It is common practice to place low voltage (LV) circuitry in these floating wells and communicate between the various voltage domains via DMOS cascodes, particularly for digital control signals. Various techniques have been described in the literature [1]–[12]. While these designs are useful for their applications, they have disadvantages, as shown in Table II:

1) Low switching speed [1], [2]: This is due to the high gate and drain capacitances of DMOS transistors or the delay through a LV transistor stack
2) Large silicon area [1], [2], : This is due to the inability to share floating N-wells among PDMOS transistors or the large area of a LV transistor stack
3) Static power consumption [3]–[9]: Not suitable for battery-powered (especially implantable) applications
4) Dynamic control signals [4], [10]: This increases system complexity, especially for arrays of level shifters
5) High voltage capacitors [11], [12]: In many processes, HV capacitors can be constructed only with normal routing metals (overlap or finger arrangement), requiring large area to obtain reasonable capacitance values

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Y. Moghe is with the Silanna Group, Sydney Olympic Park, Australia (e-mail: yash.moghe@silanna.com).

T. Lehmann is with the School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, Australia (e-mail: tlehmann@unsw.edu.au).

T. Piessens is with ICsense, B-3001 Leuven, Belgium (e-mail: tim.piessens@icsense.com).

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TABLE I
SIMULATED AND MEASURED RESULTS

Temp=25°C	Performance Parameter				
V_{DDH}=10V	Delay			Dynamic Power	
V_{SSH}=7.5V	(ns)			(μW/MHz)	
V_{DDL}=3.3V	typ	max	meas	typ	max
Basic	28.4	1048	—	900	8k
Clamp	30.0	128.9	—	98	160
Latch	34.0	132.2	—	60	86
Fast	12.0	22.8	10.7	58	64
Ultra-Fast	2.9	5.6	3.0	42	44

Temp=25°C	Performance Parameter				
V_{DDH}=10V	Delay			Dynamic Power	
V_{SSH}=6.7V	(ns)			(μW/MHz)	
V_{DDL}=3.3V	typ	max	meas	typ	max
Basic	11.8	100.2	—	3880	36k
Clamp	12.3	33.1	—	86	128
Latch	14.9	37.6	—	62	72
Fast	7.7	13.3	8.6	62	68
Ultra-Fast	2.2	3.5	2.4	48	50

The novel techniques in this paper avoid the above drawbacks while simultaneously improving silicon area, speed and dynamic power consumption. The techniques described are additive, in that they build on each other, resulting in a performance increase each time. We focus on implementations that require only thin-oxide DMOS transistors (high drain-source and drain-gate voltage but low gate-source voltage) as these work efficiently over a wide range of supply voltages; and furthermore, thick-oxide DMOS transistors are not always available. Nevertheless, many of these techniques are generic and easily ported to thick-oxide DMOS designs.

These techniques are robust and specifically account for wide process variations (process corners), ensuring high production yield. The circuits, along with special test circuitry, were fabricated on a 0.35 μm HV CMOS process and tested.

II. Conventional HV Level Shifting

While many variations on HV level shifting circuits exist in the literature, we focus on those that draw no static supply current and don't require HV capacitors. The classic design transforms the well-known low voltage level shifter [Fig. 1(a)] to a HV equivalent using DMOS cascodes [2] [Fig. 1(b)]. In

TABLE II
COMPARISON WITH PREVIOUS WORK BY OTHERS

Prior Work	Year	Tech Type	Tech Node L (μm)	Delay D (ns)	Voltage V (V)	D/(LV) (ns/(μm.V))	Disadvantages compared to this work
Declerq et al. [3]	1993	CMOS	2	80	50	0.8	Static power consumption
Doutreloigne et al. [4]	1999	HV CMOS	0.7	15	20	1.07	Static power, external dynamic controls
Pan et al. [1]	2003	HV SOI	0.35	20	18	3.2	Low speed, large area
Park et al. [5]	2006	DMOS	1.0	50	160	0.31	Static power, HV caps
Doutreloigne et al. [10]	2006	HV CMOS	0.7	2000	100	28.6	External dynamic controls
Serneels et al. [12]	2006	CMOS	0.13	0.08	2.4	0.26	HV capacitors
Chebli et al. [11]	2007	HV CMOS	0.8	475	100	5.9	HV capacitors
Rossberg et al. [6]	2007	SOI-CMOS	-	350	400	-	Static power consumption
Buyle et al. [7]	2008	HV CMOS	0.35	2.5	25	0.29	Static power consumption
Khorasani et al. [8]	2008	HV CMOS	0.8	-	300	-	Static power consumption
Choi et al. [2]	2009	SOI	-	-	100	-	Low speed, large area
Khorasani et al. [9]	2009	HV CMOS	0.8	-	150	-	Static power, low speed, large area
Present work	2010	HV CMOS	0.35	2.4	10	0.69	-

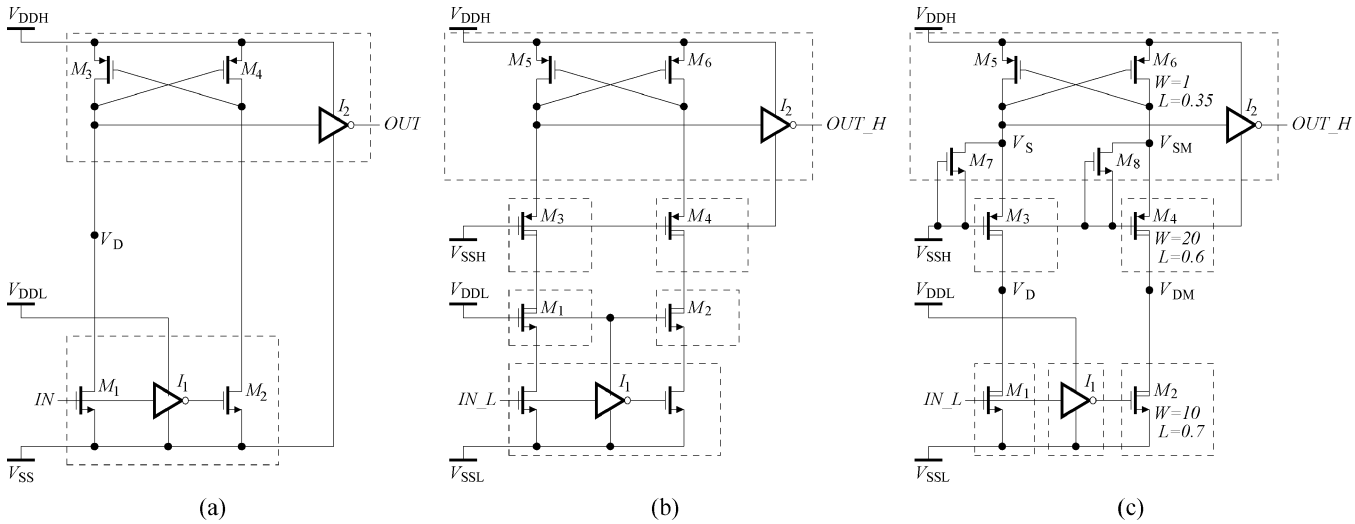

Fig. 1. Basic level shifting: (a) low-voltage prototype; (b) transformed to HV; (c) with simple modifications. Device dimensions given in microns. Dashed boxes indicate separate N-wells. All devices are placed in N-wells. nMOS transistors are placed in P-wells inside N-wells (not directly in the P-substrate).

Fig. 1(b), the NDMOS cascode transistors M1/M2 (with gates connected to V_{DDL}) protect the LV pull-down transistors. Similarly, the PDMOS transistors M3/M4 (with gates connected to V_{SSH}) protect the floating LV circuitry sitting between the V_{SSH} and V_{DDH} rails. Dashed boxes indicate separate N-wells. On most HV CMOS processes, NDMOS transistors must each have their own N-well (the drain terminal).

Even for this basic circuit, improvements can be made as shown in Fig. 1(c). The NDMOS transistors are used directly as pull-downs rather than as cascodes, saving some area. Two additional low-voltage nMOS transistors M7/M8 are also added to the floating circuitry to prevent the sources of the PDMOS transistors being pulled more than a diode drop below V_{SSH}. Otherwise, even though a PDMOS transistor may be off, leakage can pull its source down by several volts, weakening or destroying the gate oxide. Khorasani *et al.* [9] used resistor pull-ups to achieve the same effect, but with the disadvantage of dissipating static power.

A. Device Sizing for DC Operation

In this section, we derive design equations for DC operation for the LV and HV circuits in Fig. 1 to show the difficulty in the LV-to-HV transformation. To explicitly avoid negative quantities in the algebra, we use the symbols V_{tn} and $|V_{tp}|$ to denote N-channel and P-channel threshold voltages respectively. Furthermore, for brevity we use $K' = \mu C_{ox}$, with a subscript indicating N-channel or P-channel.

For the LV prototype in Fig. 1(a), consider the case where V_D is high. In this state, the gates of M1 and M3 are both at V_{SS}. To flip the state of the level shifter, M1 needs to be sized relative to M3 such that when the gate of M1 is set to V_{DDL} and the gate of M3 is still at V_{SS}, the common drain voltage V_D can be pulled down to at least $|V_{tp}|$ below V_{DDH} – otherwise the latched state cannot be flipped quickly. By symmetry, M2 and M4 are sized the same way. Under these conditions, M1 is in the active region (assuming similar threshold voltages for P and N channel transistors and $V_{DDL} < V_{DDH}$), while M3 is in the triode region. We assume M3 is in the linear triode region to conservatively overestimate its strength.

The currents through M1 and M3 are given by:

$$I_{D1} = \frac{1}{2} K_n' \left(\frac{W}{L}\right)_n (V_{DDL} - V_{tn})^2$$

$$I_{D3} = K_p' \left(\frac{W}{L}\right)_p (V_{DDH} - |V_{tp}|)|V_{tp}|.$$

Since M1 and M3 pass the same current, we equate the two equations to derive the following design equation:

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = 2\frac{K'_p}{K'_n}\frac{(V_{DDH} - |V_{tp}|)|V_{tp}|}{(V_{DDL} - V_{tn})^2}. \quad (1)$$

For good yield, the NMOS/PMOS ratio is set for the slow N/fast P corner with maximum V_{DDH} and minimum V_{DDL}.

For the HV transformed case in Fig. 1(c), the situation is quite different. As M1 turns on, V_D is pulled down, and since M3 is on, V_S follows. However, as V_S drops, the gate drive on M3 decreases, making the pulldown weaker. Therefore, it can be seen that the ratio of M3 to M5 is the critical design parameter. Again, M2, M4 and M6 are sized to make the circuit symmetrical. In the following equations, we set $V_{DD} = V_{DDH} - V_{SSH}$ for algebraic brevity and solve for the case where $V_S = V_{DDH} - |V_{tp}|$.

As for the LV case, M5 is conservatively taken to be in the linear triode region and the current through it is given by

$$I_{D5} = K'_p\left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)|V_{tp}|.$$

If $V_D < V_{SSH}$, which is easily achieved with a minimum size M1, then M3 is in the active region with current:

$$I_{D3} = \frac{1}{2}K'_{pd}\left(\frac{W}{L}\right)_{pd} (V_{DD} - |V_{tp}| - |V_{tpd}|)^2$$

where the additional subscript d is used to indicate DMOS. Equating I_{D3} and I_{D5} gives the following design equation:

$$\frac{\left(\frac{W}{L}\right)_{pd}}{\left(\frac{W}{L}\right)_p} = 2\frac{K'_p}{K'_{pd}}\frac{(V_{DD} - |V_{tp}|)|V_{tp}|}{(V_{DD} - |V_{tp}| - |V_{tpd}|)^2}. \quad (2)$$

Firstly, from the denominator of (2), the floating voltage domain $V_{DDH} - V_{SSH}$ must be greater than $|V_{tp}| + |V_{tpd}|$. Otherwise, M3 works in the subthreshold region during pulldown, which makes for a very large ratio in (2). In simulation with $V_{DDH} - V_{SSH}$ equal to 1.4 V (approximately two threshold voltages), device ratios in excess of 100 were required for correct DC operation of the level shifter, confirming the above calculation. Secondly, for good production yield, the sizing should be done for the slow P corner (strong/weak N is irrelevant here, but relevant in later sections).

The difficulty in going from the LV case to the HV case is apparent when the sizing ratios in (1) and (2) are evaluated. For design purposes, $V_{DDL} - V_{SSL} = V_{DDH} - V_{SSH} = 2.2$ V was used (approximately three threshold voltages), and all device dimensions given in this paper are for these conditions. For many 0.35 μm CMOS processes (including this one), the ratio K'_p/K'_n is nominally equal to 1/3, mainly due to the ratio of hole to electron mobility, but in the fast P/slow N corner this increases to 1/2. In the fast P/slow N corner, the values for $|V_{tp}|$ and V_{tn} are approximately equal to 0.5 V and 0.7 V respectively for this process. Under these conditions, (1) dictates a device sizing ratio $(W/L)_n/(W/L)_p = 0.38$.

For the HV case, the critical device sizing ratio is much higher. In general, $|V_{tp}|$ and $|V_{tpd}|$ track each other, and in the slow P corner are both approximately equal to 0.8 V for this process. The ratio K'_p/K'_{pd} for most HV processes typically ranges from 2 to 5 and this is set by the tradeoff between on-resistance and breakdown voltage for DMOS transistors. The DMOS transistors we used had a breakdown voltage of 14 V, with a K'_p/K'_{pd} ratio of 2. Under these conditions, (2) dictates a device sizing ratio $(W/L)_{pd}/(W/L)_p = 12.4$ for M3/M5. This corresponds to the dimensions in this paper. In simulation in the slow P corner, we found that DC operation of the circuit was compromised below $V_{DDH} - V_{SSH} = 2$ V, which confirms the above calculation.

M1 is also scaled relative to M5 according to the following equation (which is very similar to (1)):

$$\frac{\left(\frac{W}{L}\right)_{nd}}{\left(\frac{W}{L}\right)_p} = 2\frac{K'_p}{K'_{nd}}\frac{(V_{DD} - |V_{tp}|)|V_{tp}|}{(V_{DDL} - V_{tnd})^2}. \quad (3)$$

Again, the scaling is done for the slow N/fast P corner. For the technology we used, the ratio $(W/L)_{nd}/(W/L)_p$ for M1/M5 was equal to 0.75. Note that this is higher than the case for the LV level shifter due to the lower ratio of K'_{nd}/K'_p for the NDMOS case. As shown in the next section, a minimum sized M1 is more than sufficient.

B. Dynamic Performance Calculations

The delay through the basic HV level shifter is composed of the transient behaviour on the four circuit nodes V_D, V_S, V_{DM} and V_{SM} shown in Fig. 1(c). Fig. 2 shows a top view and wafer cross section of the devices M1, M3, and M5. The various gate and junction capacitances are shown, to aid in understanding the transient behaviour of the circuit. The diagram is not to scale. Consider the case when IN_L is initially low. To switch the level shifter, the following sequence takes place:

1) IN_L goes high, charging up the gate capacitance C_{g-nd} of M1. The inverter I1 similarly discharges the gate capacitance of M2
2) The node V_D begins to drop rapidly as shown in Fig. 4. Nodes V_D and V_{DM} have the largest parasitic capacitance, as explained below, however M1 is switched on very strongly in the active region and discharges the capacitance on V_D quickly. The node V_{DM} is in a high-impedance state but remains steady due to the capacitance on the node.
3) Node V_S quickly follows V_D down until it reaches a voltage at least $|V_{tp}|$ below V_{DDH}, as determined by the relative sizing of M3 and M5. We denote the time delay thus far T_1. At this time, the node OUT_H experiences a large step increase.
4) Node V_{SM} charges up to the same voltage as V_S and we denote this time delay T_2
5) Node V_{DM} charges up slowly and linearly as shown in Fig. 4 due to the combination of large parasitic capacitance and low current through the weakly switched on devices M4 and M6 that are both in the active region. We denote this time delay T_3
6) Once V_{DM} charges up to the same voltage as V_{SM}, they both charge up towards the V_{DDH} rail. As this happens, node V_S drops further down and the positive transition on OUT_H completes. We denote this time delay T_4.

The total delay through the level shifter is composed of the sum $T_1 + T_2 + T_3 + T_4$. T_1 is quite small because although the parasitic capacitance on node V_D is large, the pulldown strength

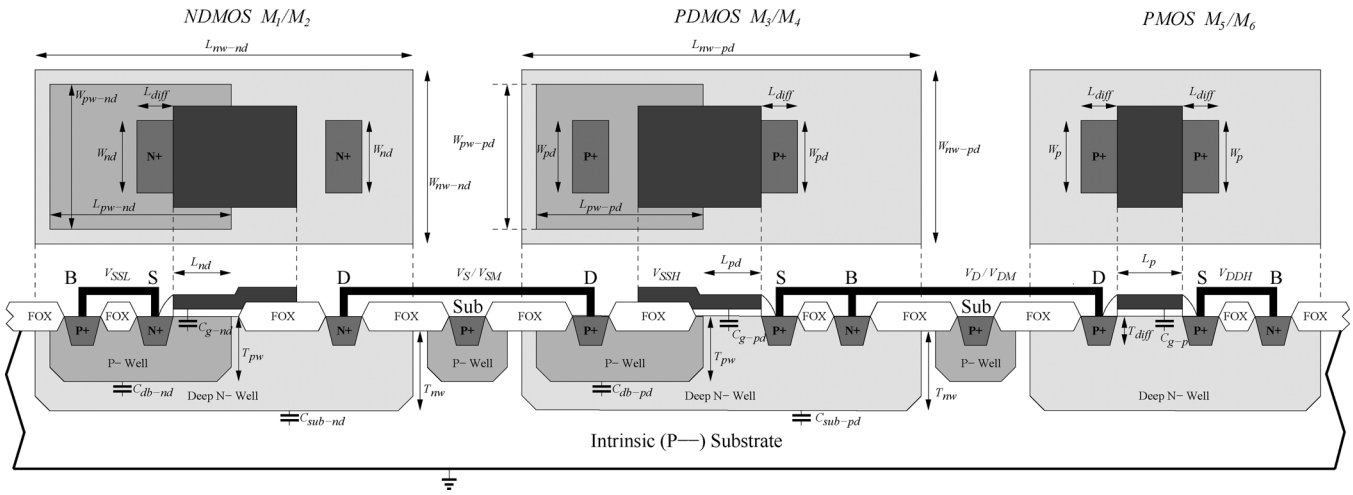

Fig. 2. Top view and cross section of important devices in basic HV level-shifter with critical dimensions marked. Diagram not to scale.

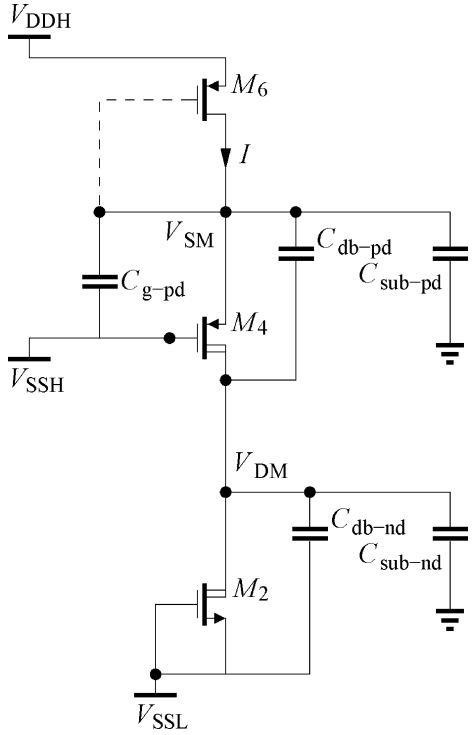

Fig. 3. Equivalent circuit during time T_3. Dashed line indicates virtual connection.

of M1 and M3 is high, resulting in a fast transient. T_2 is also small because the required voltage swing on node V_{SM} is small and can be accomplished quickly. T_3 is large due to the combination of high parasitic capacitance on node V_{DM} and the low pullup capability of M6. T_4 can also be large because M3 is only able to pull V_S quickly to within a threshold voltage of V_{SSH}. Thereafter, only subthreshold current can discharge the node further. T_1, T_2, T_3, T_4 are shown in Fig. 4.

We now give a derivation of the T_3 parameter to show how it changes with device width and the values of V_{DDH} and V_{SSH}. We do not give a derivation of T_4 since we show later in Section III how to minimise it by various techniques.

T_3 is the time that it takes node V_{DM} to charge from V_{SSL} to above V_{SSH} – that is, nearly through the entire V_{DDH} voltage. During this time, nodes V_S and V_{SM} are equal by reason of circuit symmetry. M6 thus acts like a diode-connected transistor in the active region. M4 is also in the active region. The currents through M4 and M6 are given by

$$I_{D4} = \frac{1}{2}K'_{pd}\left(\frac{W}{L}\right)_{pd}(V_{SM} - V_{SSH} - |V_{tpd}|)^2 \tag{4}$$

$$I_{D6} = \frac{1}{2}K'_{p}\left(\frac{W}{L}\right)_{p}(V_{DDH} - V_{SM} - |V_{tp}|)^2. \tag{5}$$

For algebraic simplicity, we make the substitution $V = V_{SM} - V_{SSH}$ and $V_{DD} = V_{DDH} - V_{SSH}$. That is, we consider V_{SSH} to be the local ground potential and specify voltages relative to that. Equating currents through M4 and M6 gives

$$\frac{\left(\frac{W}{L}\right)_{pd}}{\left(\frac{W}{L}\right)_{p}}\frac{K'_{pd}}{K'_{p}} = \frac{(V_{DD} - V - |V_{tp}|)^2}{(V - |V_{tpd}|)^2}. \tag{6}$$

However, from (2), we know

$$\frac{\left(\frac{W}{L}\right)_{pd}}{\left(\frac{W}{L}\right)_{p}}\frac{K'_{pd}}{K'_{p}} = 2\frac{(V_{DD-\min} - |V_{tp-\max}|)|V_{tp-\max}|}{(V_{DD-\min} - |V_{tp-\max}| - |V_{tpd-\max}|)^2}$$

where $|V_{tp-\max}|$ and $|V_{tpd-\max}|$ represent the threshold voltages for pMOS and PDMOS respectively in the slow P process corner. Also, as explained earlier, $|V_{tp-\max}| \approx |V_{tpd-\max}|$ and $|V_{tp}| \approx |V_{tpd}|$ (PMOS and PDMOS transistors track each other across process corners) and $V_{DD-\min} \approx 3|V_{tp-\max}|$. Substituting these into (6) and solving for V, we get

$$V \approx \frac{1}{3}(V_{DD} + |V_{tpd}|). \tag{7}$$

Substituting this back into (4) gives

$$I \approx \frac{1}{6}K'_{pd}\left(\frac{W}{L}\right)_{pd}(V_{DD} - 2|V_{tpd}|)^2. \tag{8}$$

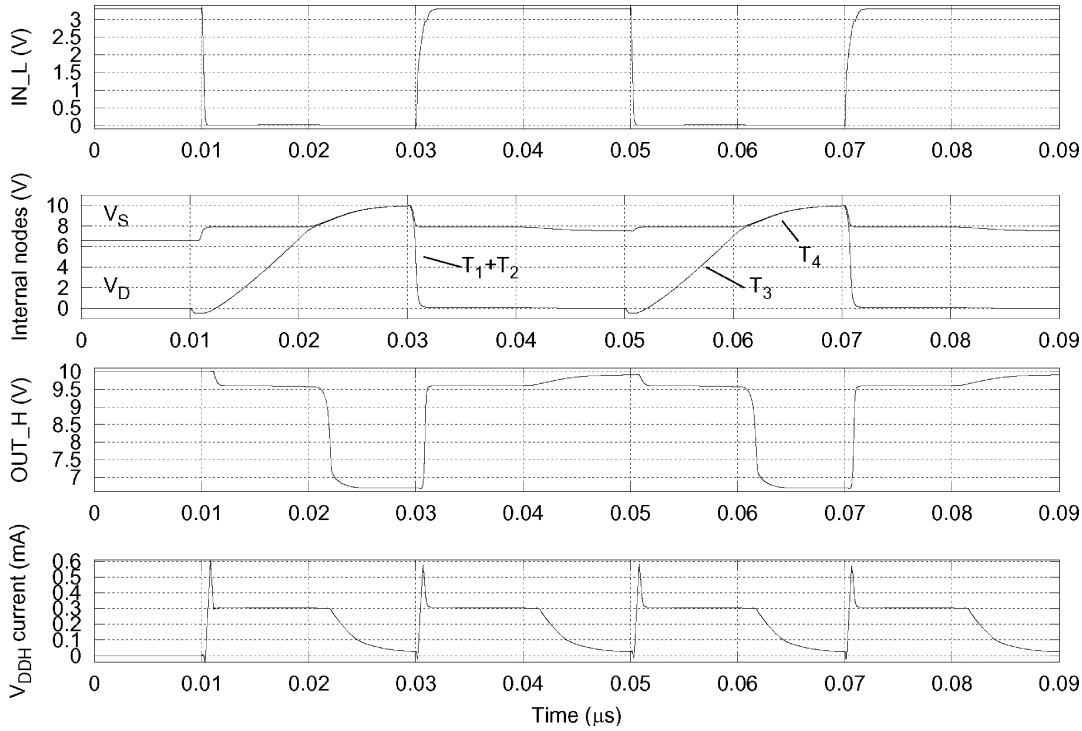

Fig. 4. Transient operation of basic HV level shifter. Delays T_1-T_4 (Section II-B) indicated.

To understand the speed at which node V_{DM} charges up, we examine the dynamic circuit consisting of ideal transistors and major parasitic capacitances shown in Fig. 3. The dashed line shows the virtual diode connection of M6. In reality, the instantaneous currents through M4 and M6 are not the same due to the presence of C_{db-pd}. The current required to discharge C_{db-pd} during the T_3 transient actually flows through M4, thus increasing the V_{SM} voltage and making the virtual diode connection of M6 not strictly valid. However, we verified in simulation that the error in current associated with making the diode connection assumption is less than 10%, and is thus acceptable in order to simplify the analysis.

Node V_{SM} is a low-impedance node due to the virtual diode connection assumption, and hence C_{g-pd} and C_{sub-pd} play no part in the dynamic response. Capacitances C_{sub-nd}, C_{db-nd} and C_{db-pd} experience the same voltage change at node V_{DM}, which needs to be supplied by the current I in (8).

From Fig. 2, the value of C_{db-nd} is given by

$$C_{db-nd} = C_{j-pw}(W_{nd} + W_{ex-pwnd})(L_{pw-nd} + 2T_{pw}) + 2C_{j-pw}L_{pw-nd}T_{pw}$$

where C_{j-pw} is the junction capacitance per square micron of the P-well/N-well interface and $W_{ex-pwnd}$ is the constant dimension $W_{pw-nd} - W_{nd}$ (twice the overhang of the P-well width beyond the NDMOS width). L_{pw-nd} is constant since L_{nd} is always chosen to be minimum. T_{pw} and T_{nw} are the depths of P-wells and N-wells respectively. Therefore, C_{db-nd} can be rewritten as

$$C = A_{pw-nd}W_{nd} + B_{pw-nd} \tag{9}$$

where A_{pw-nd} and B_{pw-nd} are constants defined as

$$\begin{aligned} A_{pw-nd} &= C_{j-pw}(L_{pw-nd} + 2T_{pw}) \\ B_{pw-nd} &= C_{j-pw}W_{ex-pwnd}(L_{pw-nd} + 2T_{pw}) \\ &\quad + 2C_{j-pw}L_{pw-nd}T_{pw}. \end{aligned}$$

Similarly, C_{sub-nd} and C_{db-pd} can be written as

$$C_{sub-nd} = A_{nw-nd}W_{nd} + B_{nw-nd} \tag{10}$$

$$C_{db-pd} = A_{pw-pd}W_{pd} + B_{pw-pd} \tag{11}$$

where the constants are similarly defined as:

$$\begin{aligned} A_{nw-nd} &= C_{j-nw}(L_{nw-nd} + 2T_{nw}) \\ B_{nw-nd} &= C_{j-nw}W_{ex-nwnd}(L_{nw-nd} + 2T_{nw}) \\ &\quad + 2C_{j-nw}L_{nw-nd}T_{nw} \\ A_{pw-pd} &= C_{j-pw}(L_{pw-pd} + 2T_{pw}) \\ B_{pw-pd} &= C_{j-pw}W_{ex-pwpd}(L_{pw-pd} + 2T_{pw}) \\ &\quad + 2C_{j-pw}L_{pw-pd}T_{pw}. \end{aligned}$$

The total capacitance is the sum of the three above:

$$\begin{aligned} C_{tot} &= C_{db-pd} + C_{sub-nd} + C_{db-nd} \\ &= A_{pw-pd}W_{pd} + W_{nd}(A_{nw-nd} + A_{pw-nd}) \\ &\quad + B_{pw-nd} + B_{nw-nd} + B_{pw-pd} \\ &= K_1W_{pd} + K_2W_{nd} + K_3. \end{aligned} \tag{12}$$

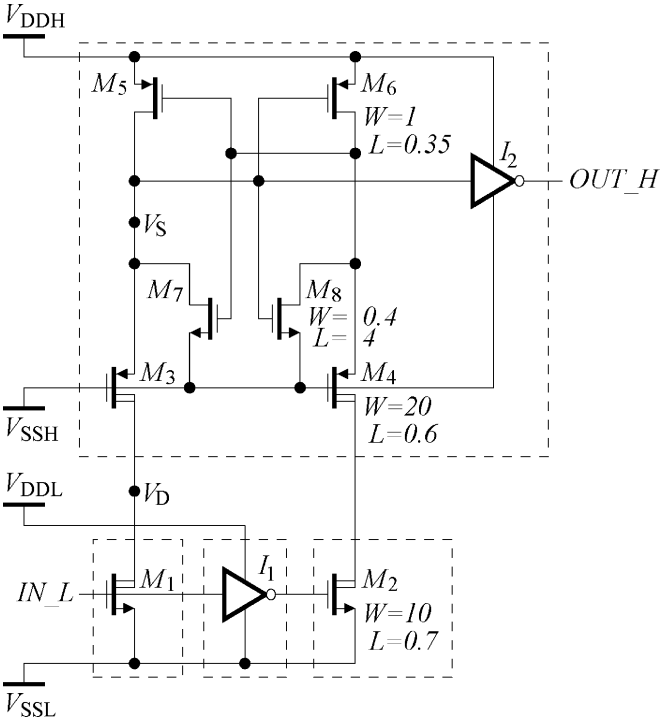

Fig. 5. Active clamping. Dimensions in microns. Separate dashed N-wells.

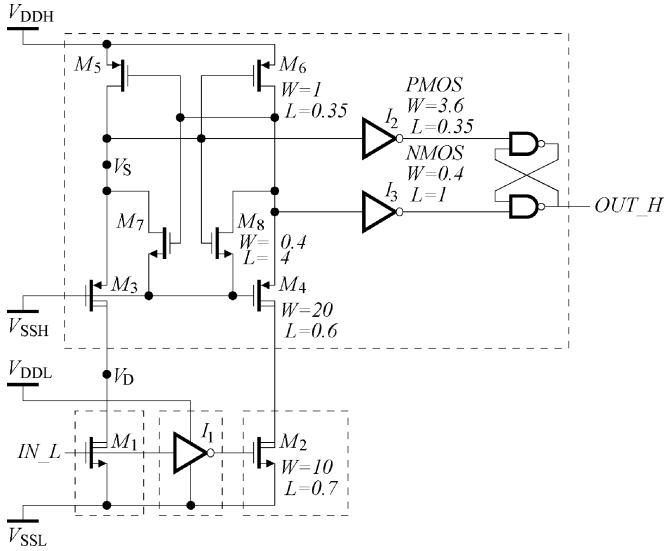

Fig. 6. Addition of latch. Dimensions in microns. Separate dashed N-wells.

The time T_3 taken to charge up node V_{DM} to approximately V_{DDH} is then calculated from (8) and (12) according to the capacitor equation $\Delta T = C\Delta V/I$:

$$T_3 = \frac{6V_{DDH}L_{pd}}{K'_{pd}(V_{DD} - 2|V_{tpd}|)^2}(K_1 + K_2\frac{W_{nd}}{W_{pd}} + \frac{K_3}{W_{pd}}). \quad (13)$$

It should be noted that the delay is a linear function of V_{DDH}, and this behaviour can be seen in the measured delay plot for the fast mode level shifter shown in Fig. 13. It is also highly sensitive to $V_{DD} = V_{DDH} - V_{SSH}$ and $|V_{tpd}|$ (and $|V_{tp}|$). Finally, it is apparent that scaling W_{pd} (and all other device dimensions correspondingly) reduces the delay. In the next section, we use the insight gained from the above equation to size the devices appropriately.

C. Device Sizing for Dynamic Operation

In Section II-A, we showed how to select the relative W/L ratios for M1, M3 and M5 to guarantee correct DC operation. In Section II-B, we extended this to derive an expression for the main delay component T_3 in the level shifter. There remains now the task of choosing the actual W/L ratios for each device. This decision is based on minimising layout area and maximising speed of operation.

By examining (13), we see that when scaling W_{pd} (and all other device dimensions correspondingly), there are three distinct regimes in the delay curve. Firstly, when W_{nd} is minimum and W_{pd} is close to minimum, the $((K_2W_{nd} + K_3)/W_{pd})$ term dominates and the delay decreases almost proportionally to the increase in W_{pd}. As W_{pd} is increased toward the limit specified by (3), the $(K_1 + K_2W_{nd}/W_{pd})$ term reaches a constant value and sets a lower limit to the delay through the level shifter. As M1, M3 and M5 are further scaled up, diminishing returns are achieved due to this limit.

For the basic HV level shifter, the general design algorithm to achieve a desired speed is as follows:

1) Choose minimum size allowable for M3 and select M5 accordingly using (2). All device lengths are kept to minimum. The minimum M1 allowed in the technology is usually far larger than that stipulated by (3)
2) If speed is not sufficient, scale up M3 and M5 together until it is, but only up to the limit set by (3) for the minimum sized M1
3) If speed is still insufficient, scale M1, M3 and M5 together until required speed is achieved, noting that there is an upper limit which cannot be exceeded

The above approach is inefficient because both the circuit area and dynamic power increase proportionally to the speed increase. The techniques we present in Section III are novel in that they allow small sized DMOS transistors to be used, while increasing speed and decreasing power and area.

D. Conventional Circuit Performance Summary

The conventional technique has several disadvantages. Firstly, each PDMOS transistor must be in a separate well. Ideally, the PDMOS bulks should be tied to V_{DDH} , allowing them to share the floating well. However, because the source can drift below V_{SSH}, the bulk must be able to follow it, otherwise the source-bulk junction could exceed the technology limit. The extra transistors M7/M8 in Fig. 1(c) help alleviate this problem by acting as diodes, but under that arrangement, the high-side voltage domain $V_{DDH} - V_{SSH}$ needs to be made a diode drop smaller than the maximum voltage tolerance of the low-voltage transistors in the technology, which can be a disadvantage. Because each PDMOS transistor is in a separate well, the size of the level shifter is large. Especially for arrays of level shifters, this is a serious disadvantage.

Another disadvantage of the basic level shifter is very low switching speed. As shown in sections Sections II-A–II-C, one branch of the level shifter switches fast (the NDMOS and

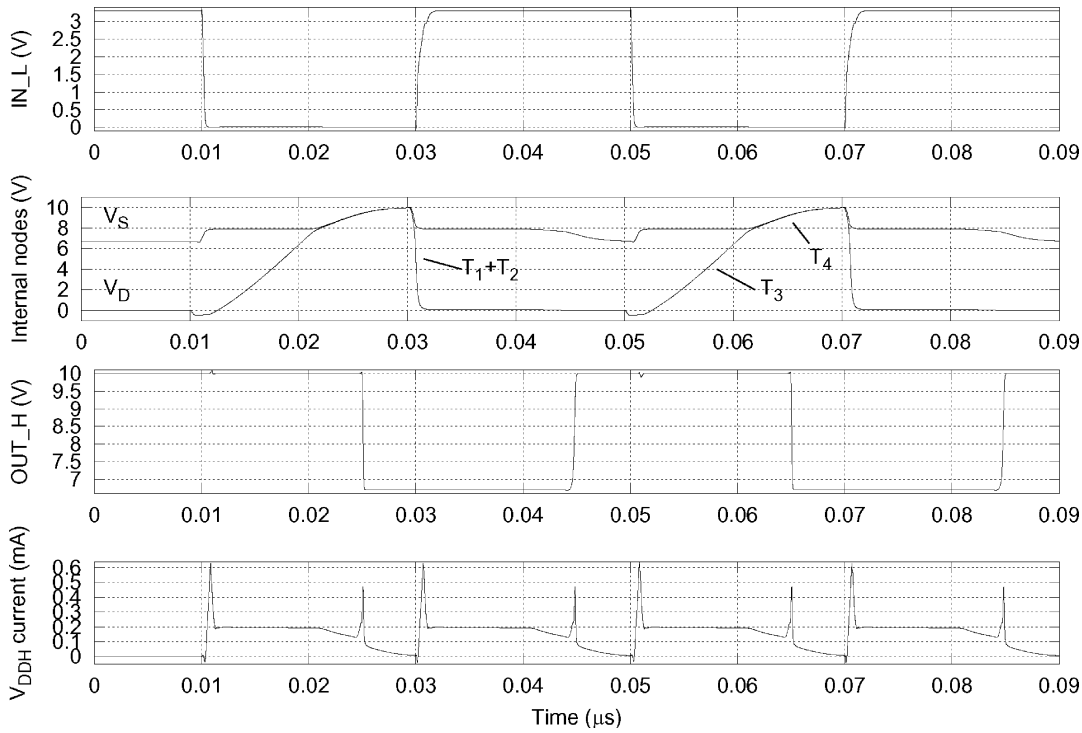

Fig. 7. Transient operation of latching HV level shifter. Delays T_1-T_4 (Section II-B) indicated.

PDMOS pull down quickly), but the other one takes a long time to pull up due to the weak PMOS. As shown in Table I, delays of over 1 μs are seen in simulation over process corners. This is far more than the 1–2 ns of delay typically seen in the LV prototype level-shifter, even accounting for much higher V_{DDH}.

Coupled with the slow switching speed is very high power consumption. As noted above, the PDMOS is only able to pull its source voltage to within a threshold of V_{SSH} quickly, and thereafter subthreshold current pulls the source voltage down the rest of the way. To restore full digital switching levels, an output inverter must be used. The inverter dissipates crowbar current long after the switching event, as much as several microseconds over process corners. If the circuit normally switches more often than every few microseconds, then it effectively always dissipates static power. The extra current during and after switching flows from V_{DDH}, which is the worst point for power consumption. Simulations over corners showed currents of up to 100 μA flowing statically. With V_{DDH} at 10 V (a typical level for implantable neurostimulator applications) and V_{SSH} generated by a linear regulator down to V_{SSL} (typical for most systems), this equals 1 mW of static power, which is unacceptable given that there may be tens or hundreds of such level shifters on the chip. Even without the static current flow, it can be seen from Table I that typical dynamic power consumption of the basic HV level shifter is 0.9–3.9 mW/MHz, which is also unacceptable for battery powered or implantable systems. For other HV applications (automotive, MEMS, power switching), with V_{DDH} of 50 V or more, power consumption would be correspondingly higher.

The final disadvantage of this circuit is highly asymmetrical switching. As explained above, the two branches in the level-shifter switch at very different speeds. Hence, the output of the circuit switches quickly in one direction but very slowly in the other. A plot of the circuit operation is shown in Fig. 4.

III. Design Improvements

In this section, we present a series of additive design improvements that can be applied to speed up the basic circuit and reduce area and power consumption.

A. Improvement I – Clamping

A simple improvement can be made to the basic design as shown in Fig. 5. Here the diode connected transistors M7/M8 from the basic circuit in Fig. 1(c) are reconnected to actively pull down the source voltages of the PDMOS transistors to V_{SSH}. The transistors M5/M7 and M6/M8 thus effectively form a pair of latching inverters with the PDMOS transistors M3/M4 used to change the latched state. Because the PDMOS cannot initially pull its source voltage down to V_{SSH}, the nMOS transistor needs to be made much weaker than the pMOS transistor. Otherwise the latch would never change state. This is especially true in the strong N, weak P process corner. The device sizes we used for $V_{DDH} - V_{SSH} = 2.2$ V are shown in Fig. 5. Note that the W/L ratio of M6 is about 30 times larger than that of M8. Taking the ratio $K'_n/K'_p = 3$ into account, this makes M8 10 times weaker than M6, which sets the switching threshold of the inverter M6/M8 to around $V_{DDH} - |V_{tp}|$. This matches the device sizing decision made in Section II-A whereby the source voltage of the PDMOS is pulled down to at least $V_{DDH} - |V_{tp}|$ initially. This improvement is not novel and has been used by others [12], [13]. However, we present a full analysis of, and design guidelines for, the technique for the first time.

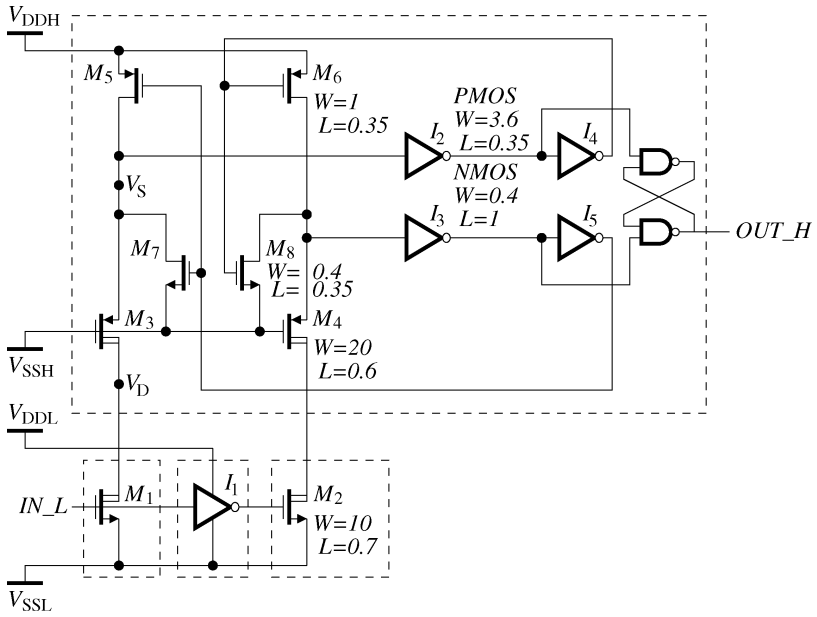

Fig. 8. Fast mode. Dimensions in microns. Separate dashed N-wells.

This technique has a number of advantages, the most important being silicon area reduction and elimination of crowbar current after the switching event. Since the source voltages of the PDMOS transistors are limited strictly within V_{DDH} and V_{SSH} (they cannot drift a diode voltage below V_{SSH} as before), the PDMOS transistors can be placed in the same N-well as the floating circuitry (PDMOS bulks connected to V_{DDH}). This reduces the number of N-wells required for each level shifter from 6 to 4, resulting in an area saving of 30–40% depending on technology. If level shifters are arrayed, then the V_{DDH} and V_{DDL} N-wells can be shared, effectively bringing the number of extra N-wells each circuit adds down to 2 (for the two NDMOS transistors). In this way, an area saving of 50–60% can be made for an array of level shifters.

The circuit also speeds up significantly in some process corners (shown in Table I) as the nMOS transistors help to pull the source voltages of the PDMOS transistors down to V_{SSH}. Essentially, this minimises the T_4 component of the delay as shown in Section II-B. This also eliminates the post-switching crowbar current in the output inverter. In fact, the output inverter can be eliminated, although this is not recommended as it will limit the drive capability of the circuit.

The low-power feature makes this circuit attractive to battery-powered applications. While this circuit is a significant improvement over the original in terms of area and power, it is still slow and has the asymmetrical switching characteristic. These aspects are dealt with in the following sections.

Interestingly, in the typical process corner, the circuit slows down somewhat compared to the basic HV level shifter. This is because the bulks of the PDMOS transistors M3 and M5 are no longer connected to their sources, but to a higher voltage V_{DDH}. This raises the threshold voltages of the PDMOS transistors due to the body effect. However, the small decrease in the typical corner is well worth the speedup in the worst case corners, as well as the area and power saving.

B. Improvement II – Latching

The asymmetrical switching of the previous circuit is a disadvantage as it adds skew to digital signals. This disadvantage is overcome by the addition of custom inverters and a NAND gate latch as shown in Fig. 6. The inverters I_2 and I_3 are sized to be sensitive to the initial dip in the source voltage of the PDMOS transistors (strong pMOS and weak nMOS transistors). Again, the W/L ratio of the pMOS and nMOS have been sized to place the inverter switching threshold at roughly $V_{DDH}-|V_{tp}|$, but this time the pMOS has been made minimum length to save space and speed up the circuit. The inverters present clean transitions to the inputs of the latch. The latch itself delays switching at the outputs until both branches of the level shifter have changed state.

This improvement makes the output switching symmetrical. Instead of distorting the digital signal, a simple delay is introduced. This behaviour can be seen in the simulation plot in Fig. 7. This feature is very useful where signal timing across voltage domains is important, for example in neurostimulators where charge balance between sourcing (from V_{DDH}) and sinking (to V_{SSL}) current is required [14]. The area penalty of the inverters and latch is less than 5% since the area is dominated by the DMOS transistors. There is also a slight slowdown over corners due to the extra delay through the latch.

C. Improvement III – Fast Operation

In this section we describe how to dramatically improve the switching speed of the level shifter. The circuit is shown in Fig. 8. Here the simple cross-coupling of the level shifter has been augmented by the insertion of two cascaded inverters in each path. This effectively buffers and adds gain to the PDMOS source voltage transitions, significantly increasing the gate drive voltage on the pMOS pullup. As shown in Table I, this grants a significant speed increase over the clamping and latching level-

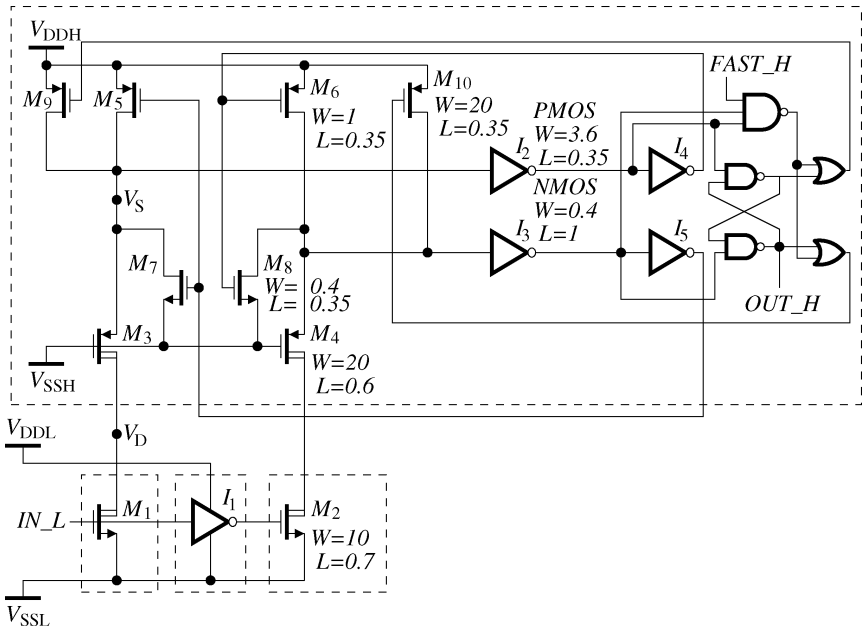

Fig. 9. Ultra-fast mode. Dimensions in microns. Separate dashed N-wells.

shifters. Note that the first inverter is sized to be sensitive to the initial dip in the PDMOS source voltage, as in the previous section. The second inverter is a normal minimum sized symmetrical inverter. Even though there are two extra inverters switching in this circuit compared to the previous section, the faster switching speed keeps the dynamic power consumption down (crowbar current flows for a shorter time). As shown in Table I, in some corners the power consumption is reduced by up to 25% compared to the previous section.

Since the nMOS pulldowns on the PDMOS sources are no longer directly cross-coupled, they can be made minimum length, saving layout area. Thus, the overall size of the level shifter doesn't change much compared to the last section. The output NAND latch is maintained to keep the transitions symmetrical. It is also used in the next section to make the level-shifter switch even faster.

D. Improvement IV – Ultra-Fast Operation

The speed limiting step in the previous circuit is the pullup action of the pMOS transistor. Although the gate of the pMOS transistor is driven by a full-scale digital signal (due to the buffer), the pMOS transistor is still weak compared to the PDMOS transistor. This limits how much the PDMOS source voltage can be pulled up initially, which in turn limits the rate at which the drain voltage of the NDMOS transistor can be charged up to V_{DDH}. Until the drain voltage of the NDMOS charges up close to V_{DDH} (and the PDMOS current drops close to zero), the positive transition on the PDMOS source voltage cannot finish. As explained earlier, it is not possible to make the pMOS transistor stronger as this would prevent the PDMOS transistor from pulling its source voltage down in the first place. To overcome this, the strength of the pMOS transistor needs to be augmented transiently during the pullup phase. The circuit to do this is shown in Fig. 9.

It is similar to the circuit in the previous section, with some additions. Large minimum length pMOS transistors M9/M10 have been placed in parallel with the normal weak ones M5/M6. The gates of these assisting transistors are driven by a combinatorial circuit whose inputs are the outputs of the NAND latch and the current state of the level shifter. The gate of an assisting transistor is pulled low only while the PDMOS source voltages are both low and the appropriate latch output is low. This is precisely the time interval when the level shifter is in the process of switching. Only one of the assisting pMOS transistors fires during any given switching interval. The assisting pMOS transistor pulls up the source voltage of the DMOS much higher during the switching interval and speeds up the charging of the NDMOS drain. As shown in Table I, this boosts speed beyond the fast mode described in Section III-C. Compared to the original level shifter, this circuit shows a speed increase of a factor of 5–10 in the typical process corner and a factor of 30–190 in the slowest corner.

Despite the higher transistor count, dynamic power consumption is reduced by 33% compared to the previous section due to the ultra-fast transitions. Although this design contains an element of dynamic control (the assist transistors switch on transiently), this is internally generated, thus simplifying system design. Importantly, the dynamic element adapts optimally to process corner, reducing the delay spread over corners. An area penalty of 5–10% is incurred due to the extra circuitry.

The circuit has a potential erroneous startup state where both assisting pMOS transistors are switched on. If it gets into this state it cannot switch as the PDMOS transistor cannot overcome the strong pMOS assist transistor. To overcome this, a startup circuit has been provided in the form of a FAST_H signal which is held low (at V_{SSH}) at startup. This gates the operation of the assisting pMOS transistors via the 3-input NAND gate, turning the circuit into that shown in the previous section. In a practical system design, the FAST_H signal is best implemented

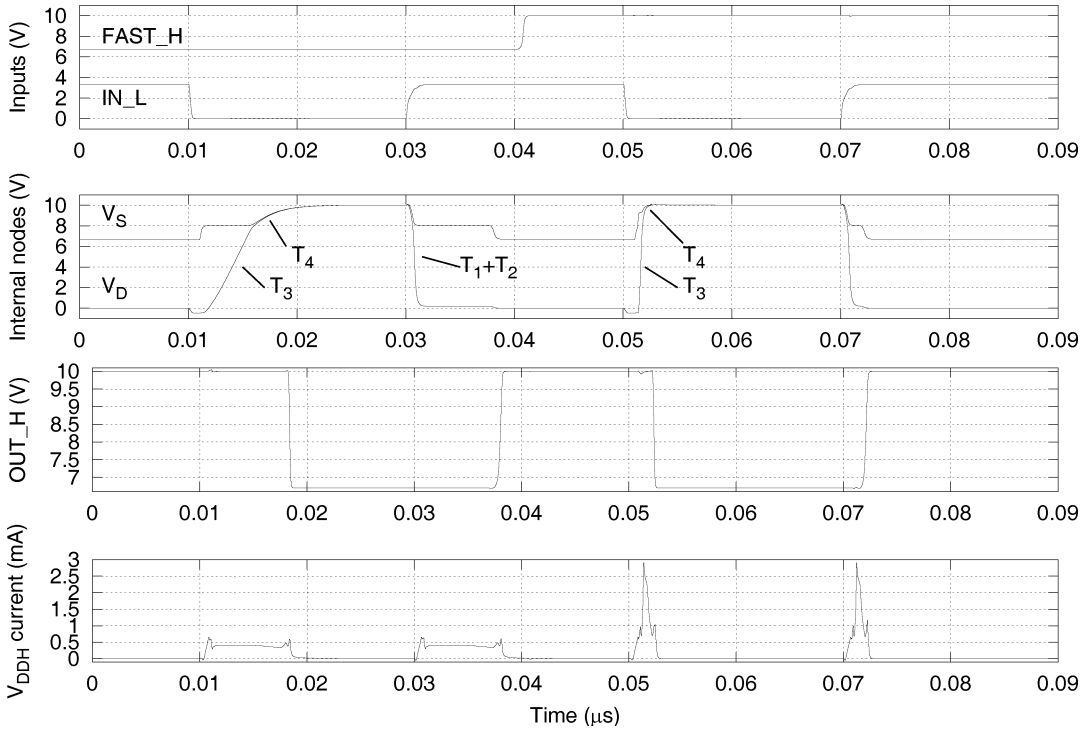

Fig. 10. Transient operation of fast and ultra-fast HV level shifter. Delays T_1-T_4 (Section II-B) indicated. T_3 and T_4 much smaller in ultra-fast mode.

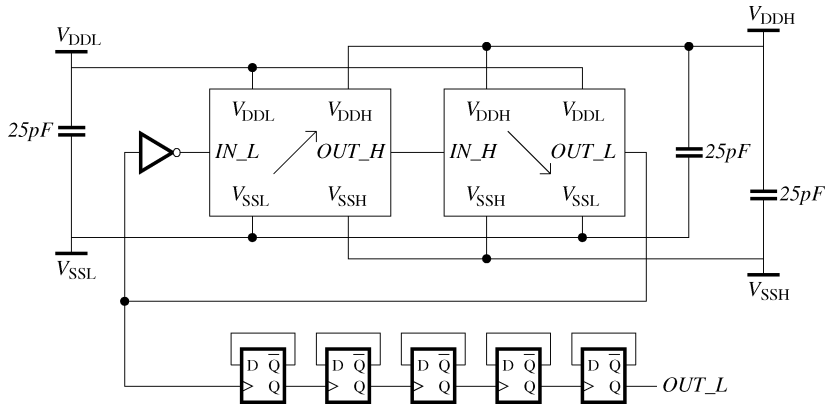

Fig. 11. Ring oscillator and divider.

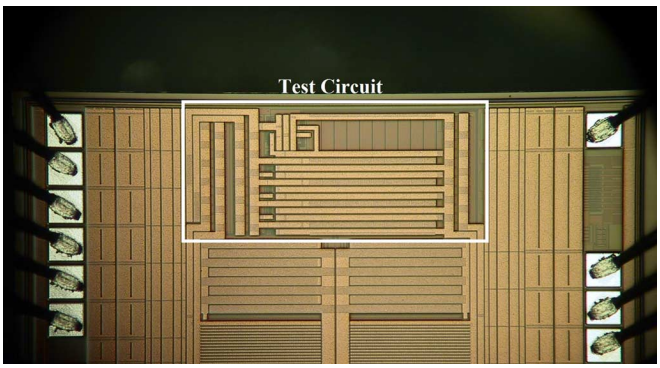

Fig. 12. Photograph of chip with test circuit highlighted.

as a global signal generated by a single level shifter without the ultra-fast mode (and thus no startup issue) and distributed around the chip. This signal is held low at system startup to allow all level shifters to get into the correct state and subsequently set high to enable the ultra-fast mode.

A simulation plot of the circuit working is seen in Fig. 10, showing the operation of both the fast and ultra-fast modes.

IV. Test Circuitry and Results

The circuits described above are fast and run at high voltages. The ultra-fast level shifter in particular has a delay of 2–4 ns. It was not possible to bring the inputs and outputs directly to chip IOs for stimulus and measurement as the speed of the IO drivers themselves would have limited the test frequencies that could be used. Even if the IO speed were sufficient, the power dissipation involved in driving HV IOs at the required frequency would be in the 200–400 mW range, causing thermal dissipation problems for the test chip.

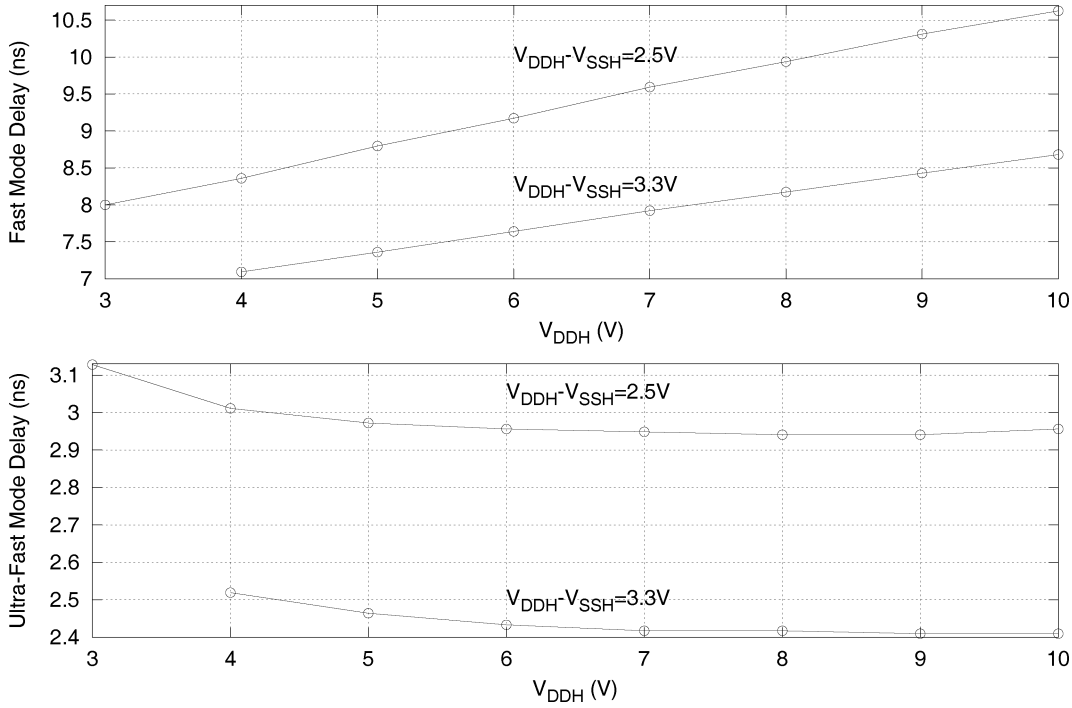

Fig. 13. Measured HV level shifter delay at different supply levels.

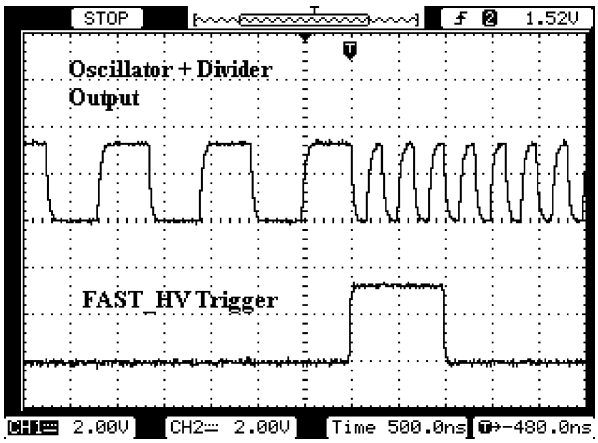

Fig. 14. Oscilloscope capture of oscillator and divider output.

Instead, we created an on-chip ring oscillator structure using an up-shifter and down-shifter in a loop. The low-voltage output of the ring oscillator was put through a flip-flop chain, dividing the oscillator frequency by 32. Since the up and down level shifters undergo two transitions each during a single oscillation, the average delay of the level-shifters was inferred by dividing the period of the output signal by 128 (32×4). The test circuit is shown in Fig. 11. The down-shifter is simply the dual of the up-shifter with the pMOS and PDMOS transistors interchanged with nMOS and NDMOS transistors (and vice versa) and the voltage domains interchanged by essentially turning the schematic upside down. The devices were sized (using the dual of (2)) to give delays similar to the up-shifter. A photo-micrograph of the test circuitry is shown in Fig. 12. Most of the area of the test circuitry (85%) is taken up by on-chip supply decoupling capacitors to keep the supplies steady. This was necessary due to the high inductance (> 2 nH) on the power and ground bondwires.

We only had enough room for a single test circuit on the chip. Since the ultra-fast circuit incorporates the fast circuit (via the FAST_H signal), we were able to test both on silicon, but not the other level shifters. Dynamic power consumption could not be measured due to the confounding effect of the IO drivers, whose power consumption was far higher than that of the core circuit. With separate pins for the IO drivers we could have distinguished the IO power from the core power; but we could not do this due to space limitations on the chip.

In Table I, simulated (typ, max) and measured delay and simulated dynamic power (typ, max) are given for $V_{DDH} = 10$ V and for two different values of $V_{DDH} - V_{SSH}$, namely 2.5 V and 3.3 V. V_{DDL} was fixed at 3.3 V to make the test chip compatible with FPGA signalling levels on the test board. As explained in the previous sections, the more complex circuits are increasingly faster and have decreasing dynamic power consumption. The ultra-fast level shifter in particular has very little spread in performance over corners, and this is due to the adaptive nature of the internal transient boost.

An extensive set of measurements of the delays through the fast and ultra-fast HV level shifters is shown in Fig. 13. V_{DDH} was swept over a large range for two values of $V_{DDH} - V_{SSH}$, with V_{DDL} fixed at 3.3 V. In the fast mode, the delay changes linearly with V_{DDH} as expected. In the ultra-fast mode, the speed is boosted until the delay is essentially flat, as determined by inherent transistor speeds. If V_{DDH} were raised even further, the linear delay behaviour would once again be seen, but for this to occur, V_{DDH} needs to be raised beyond the safe operating region for the technology. For processes with higher voltage DMOS transistors (20 V to 200 V or more), the linear dependence of delay on V_{DDH} would be seen.

An oscilloscope capture of the operation of the ring oscillator and divider is shown in Fig. 14. The top trace shows the divider output. The positive edge of the pulse on the bottom trace switches the HV level shifters in the ring oscillator from the fast mode to the ultra-fast mode.

Table II shows a comparison of this work to other previous work. Where available, the technology node L, voltage V and delay D of the level shifter has been recorded, and combined into a figure of merit $D/(LV)$ – the lower the figure of merit the better. Prior works that equal or better the figure of merit of this work all exhibit static power consumption and/or make use of HV capacitors. As stated earlier, it was a design goal of this work to avoid both of these.

V. Conclusion

We presented a comprehensive analysis of the conventional high voltage level shifter, showing the dependence of power and speed on circuit area. We then showed an additive series of novel techniques for simultaneously improving switching speed, silicon area and power consumption as well as eliminating the asymmetrical switching characteristic. These techniques are robust to process variations and have been verified on silicon. In Table I, it can be seen that for high V_{DDH} (10 V) and low $V_{DDH} - V_{SSH}$ (2.5 V), the delay through the ultra-fast level shifter increases by a factor of 10 typically and 190 in the worst case corner compared to the basic level-shifter. Under the same conditions, typical and worst case dynamic power consumptions are reduced by factors of 20 and 180 respectively. For a higher value of $V_{DDH} - V_{SSH}$ (3.3 V), the speed increase is lower but still significant, being a factor of 5 typically and 30 in the worst case corner. However, the improvement in dynamic power consumption is much higher, being a factor of 80 typically and 720 in the worst case. Silicon area is reduced by 50% overall. Static power consumption is eliminated and no HV capacitors are required. These techniques are generally applicable, but especially so in battery powered and implantable applications.

Acknowledgment

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Yashodhan Moghe received the Bachelors degree in electrical engineering and the Masters degree in biomedical engineering from the University of New South Wales (UNSW), Sydney, Australia, in 2001.

From 2001 to 2008, he was Analog ASIC Designer and then Senior Analog ASIC Designer at Cochlear Ltd., Lane Cove, Australia, where he worked on low-power analog and mixed-signal designs, including the world's first totally implantable cochlear implant. He is currently Design Manager at Silanna Group, Sydney Olympic Park, Australia, where he works on various commercial and research-based design and technology projects on Silicon-on-Sapphire (SoS) technology.

In 2006 he started a part-time Ph.D. in microelectronics at UNSW. His Ph.D. research, for which he holds a patent, focuses on novel circuits and systems to improve the electrical safety of multi-channel neurostimulator implants. His Ph.D. work is funded by Cochlear.

Torsten Lehmann (SM'06) received the M.Sc. and Ph.D. degrees in electrical engineering from the Technical University of Denmark, Lyngby, Denmark, in 1991 and 1995, respectively, for work on self-learning VLSI neural networks.

He spent two years as a Research Fellow funded by the European Union at the University of Edinburgh, Scotland, U.K., where he worked with biologically inspired artificial neural systems. From 1997 to 2000, he was an Assistant Professor in electronics at the Technical University of Denmark, working with low-power low-noise low-voltage analog and mixed analog-digital integrated circuits. He worked briefly as an ASIC design engineer with Microtronics A/S, Denmark. From 2001 to 2003 he was Principal Engineer with Cochlear Ltd., Australia, where he was involved in the design of the world's first fully implantable cochlear implant. Currently, he is a Senior Lecturer in microelectronics at the University of New South Wales, Sydney, Australia. His main research interests are in solid-state circuits and systems (analog and digital), biomedical electronics and ultra-low-temperature electronics.

Tim Piessens was born in Bornem, Belgium, in 1975. He received the Masters degree in electrical engineering and the Ph.D. degree in electronics from the Katholieke Universiteit Leuven (K. U. Leuven), Heverlee, Belgium, in 1998 and 2003, respectively.

From 1998 to 2003, he worked as a Research Assistant at the ESAT-MICAS Laboratory, K. U. Leuven, on the development of highly efficient line drivers for xDSL systems. In 2004, he co-founded the company ICsense, which is a fabless microelectronics company specializing in integrated sensor interface systems.