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NBTI and Leakage Aware Sleep Transistor Design for Reliable and Energy Efficient Power Gating

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***Abstract*—In this paper we show that power gating techniques become more effective during their lifetime, since the aging of sleep transistors (STs) due to negative bias temperature instability (NBTI) drastically reduces leakage power. Based on this property, we propose an NBTI and leakage aware ST design method for reliable and energy efficient power gating. Through SPICE simulations, we show lifetime extension up to 19.9x and average leakage power reduction up to 14.4% compared to standard STs design approach without additional area overhead. Finally, when a maximum 10-year lifetime target is considered, we show that the proposed method allows multiple beneficial options compared to a standard STs design method: either to improve circuit operating frequency up to 9.53% or to reduce ST area overhead up to 18.4%.**

I. Introduction

Reliability reduction of electronic systems in the very deep submicron (VDSM) era is one of the most critical concerns for IC designers [2]. Particularly, negative bias temperature-instability (NBTI) effect on pMOS transistors is recognized as the primary parametric failure mechanism for modern ICs [4], [12], [17]. NBTI causes a considerable increase in threshold voltage (V_{th}) when pMOS transistors are biased in strong inversion, that is during their ON state [5]. This effect increases dramatically at higher operating temperature and supply voltage [7]. These conditions are typically experienced by ICs during standard burn-in test [16], which can cause significant NBTI degradation (V_{th} increase) of the devices even for short burn-in duration (tens of hours) [7].

Along with reliability, power consumption has become a major issue for modern ICs. VDSM technologies enable the integration of billions of gates on a small die, leading to a power density and total power dissipation that is at the limits of what packaging and cooling can support [9]. Moreover, as technology shrinks, leakage power is increasing dramatically, to the point where it can be nearly as large as dynamic power [9]. One effective approach to tackle leakage power is power gating [14]. It utilizes transistors as power switches to disconnect logic blocks from supply voltage during periods of inactivity. Power switches, also referred to as *sleep transistors* (*STs*) are implemented either as header or footer switches. A header switch uses a high V_{th} pMOS transistor to control V_{dd}, while a footer switch uses a high V_{th} nMOS transistor to control V_{ss}. The use of high V_{th} transistor allows designers to further reduce leakage power, as it decreases exponentially with transistor V_{th}. Both header and footer STs can be used in a power gating design. However, footer STs are more costly to design, requiring a triple well CMOS process [9]. Therefore, header STs are more commonly used in commercial power-gated circuits, and will be considered in this paper.

Header STs degrade because of NBTI like any other pMOS transistor. Particularly, since STs are always ON (under stress) when the power-gated circuit is operating, they suffer from an even higher degradation compared to functional transistors [6], [18]. As a result, since STs are on the critical path, their degradation will reduce circuit performance and lifetime, thus causing long-term reliability issues [18]. While standard power gating approaches [8]–[10], [15] ignore the detrimental effect of NBTI on STs, a few countermeasures have been proposed to tackle NBTI effect on power-gated circuits [6], [18]. They mainly rely on ST network oversizing and adaptive body bias [6], [11], which allow designers to extend circuit lifetime and increase its long-term reliability at the cost of more area and increased design complexity.

In this paper, to the best of our knowledge, we show for the first time that ST aging due to NBTI can considerably benefit leakage power saving. As a result, the effectiveness of power gating in terms of leakage reduction increases with ST aging. By SPICE electrical simulations performed considering two case studies (10 FO4 cascaded inverters and the *b02* benchmark from the *itc99* benchmark suite) implemented by a 32nm, Metal Gate, High-K, Strained-Si CMOS technology [1], we show that leakage power may reduce by more than $5\times$ during the first month of operation, by more than $10\times$ during the first year, and up to $20\times$ in 10 years of circuit operation. This leads to an over-reduction of leakage power during circuit lifetime with respect to the value expected by standard NBTI-unaware power gating techniques. Based on this feature, we propose an NBTI and leakage aware ST design method for reliable and energy efficient power gating. It relies on the identification of an ST threshold voltage suitably lower than that of standard high V_{th} STs, accounting for the NBTI degradation induced during burn-in test. This way, part of the unexpected leakage power over-reduction is spent to counteract the detrimental effects of ST aging on circuit long-term reliability. Through SPICE simulations of ISCAS85 benchmarks, we show that the proposed ST design approach enables a circuit lifetime extension up to $19.9\times$ and an average leakage power reduction (per year of lifetime) up to 14.4% compared to standard ST design approach. It is worth noting that these improvements are achieved without any area overhead, thus reducing the cost over alternative

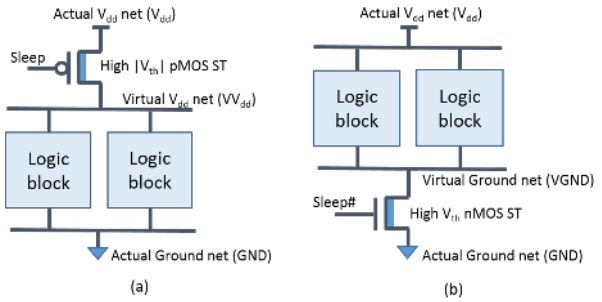

Fig. 1. Power-gating approaches: (a) header pMOS ST; (b) footer nMOS ST.

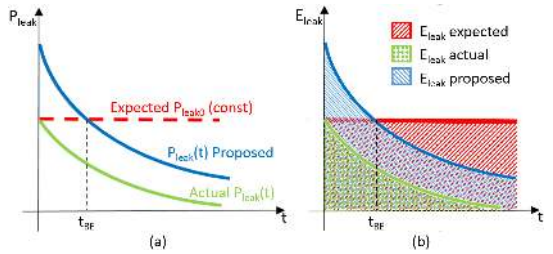

Fig. 2. Expected and actual profile for standard and proposed ST design: (a) leakage power profile; (b) leakage energy profile.

techniques in [6], [18]. Furthermore, if a maximum 10-year lifetime target is considered, the proposed method provides multiple beneficial options to designers: either to improve circuit operating frequency up to 9.53% or to reduce ST area overhead up to 18.4%.

The rest of the paper is organized as follows. In Sec. II we present same basics on NBTI and power gating approaches, and we discuss motivation and basic idea of the proposed ST design approach. In Sec. III we assess the NBTI impact on STs, considering a standard high V_{th} ST design. In Sec. IV we discuss the proposed methodology, and in Sec. V we present SPICE simulation results to validate it. Finally, in Sec. VI we draw some conclusions.

II. Background and Motivation

Negative BTI causes a threshold voltage increase in pMOS transistors, denoted by ΔV_{th}, when they are ON ($V_{GS} = V_{dd}$, stress phase) [5]. NBTI-induced degradation is partially recovered when pMOS transistors are polarized in their OFF state ($V_{GS} = 0$, recovery phase). The reaction-diffusion model in [5] allows designers to estimate threshold voltage increase as a function of technology parameters, operating conditions and time. Since threshold voltage degradation does not depend on the frequency of the input signal, but only on the total amount of the stress time, in [17] a simple analytical model has been proposed that allows designers to estimate long term threshold voltage shift. It is given by:

$$\Delta V_{th} = K\alpha^n t^n \tag{1}$$

The parameter t is the operating time, while α is the fraction of the operating time during which a pMOS transistor is under a stress condition. It is $0 \leq \alpha \leq 1$, where $\alpha = 0$ if the pMOS transistor is always OFF, while $\alpha = 1$ if it is always ON. The value of the exponent $n = 1/6$ is a fitting parameter; the parameter K lumps all the technological and environmental parameters and, as reported in [17], it is $3.9 \times 10^{-3} Vs^{-n}$.

Power gating is one of the most effective leakage power reduction techniques for VDSM technologies. It relies on selectively powering down certain blocks in the chip that are not being used by inserting a header pMOS sleep transistor (ST) in series with the pull-up logics (Fig. 1(a)), or a footer nMOS ST in series pull-down logics (Fig. 1(b)). This way, an intermediate virtual power supply (denoted by virtual V_{dd}) or virtual ground (denoted by virtual GND) is created.

A header ST uses a high V_{th} (in absolute value) pMOS transistor to connect actual and virtual V_{dd}, while a footer ST uses a high V_{th} nMOS transistor to connect actual and virtual GND. Footer STs are typically used in voltage scaling approaches [9]. Particularly, since they exhibit a lower on-resistance than pMOS transistors, they can be designed smaller in order to provide the same current. Nevertheless, header pMOS STs exhibit a better leakage characteristic than nMOS, so they can be preferred in designs where leakage constraints are stringent. Additionally, nMOS footer STs are more costly to design, since they require a triple well CMOS process [9]. Conversely, in the case of pMOS STs the n-well is readily available for bias tapping in the standard CMOS process, making their use preferred in commercial power-gated circuit.

In standard power gating approaches [8]–[10], [15] high V_{th} header STs are designed (sized) in order to achieve the desired trade-off in terms of IR drop and leakage power, without considering NBTI degradation. Therefore they identify an expected leakage power consumption as a target, which remains constant for the whole circuit lifetime. This expected value is represented in Fig. 2(a) as a dashed red line. However, as we will show in the next section, leakage power decreases as STs age. To assess this trend over time, it should be considered that leakage current has two main contributors [9]: subthreshold current and gate current. Subthreshold current contribution dominates, since gate current can be well controlled by the use of high-k dielectrics. Therefore, when an ST is OFF, its leakage current I_{leak} turns out to be [9]: $I_{leak} \propto (W/L)exp[(-qV_{th})/(nkT)]$ where W and L are the ST channel width and length, respectively, k is the Boltzmann constant, T the temperature, and n is a parameter that depends on the device fabrication. Since the main NBTI effect is to increase V_{th} as shown in (1), we expect that actual leakage power ($P_{leak} = V_{dd} \times I_{leak}$) considerably decreases as STs age (Fig. 2(a), solid green line), with a much faster reduction during the early circuit lifetime. As a result, an over-reduction of leakage power with respect to the expected value is experienced.

We propose to spend part of the (unexpected) leakage power over-reduction to counteract the NBTI effects on STs (IR drop increase and consequent circuit lifetime reduction). As it will be shown in detail in Sec. IV, this is accomplished by designing STs with a lower V_{th} compared to the standard high V_{th} STs. In fact, STs with lower V_{th} will exhibit a lower resistivity, thus a lower IR drop, allowing designers to

extend circuit lifetime and increase long-term reliability. The leakage power profile of the proposed approach is qualitatively depicted in Fig. 2(a) (blue solid line). Due to the lower initial V_{th}, a higher leakage power at the very early stage of lifetime is exhibited. Nevertheless, it rapidly drops as STs age, reaching the break-even with the expected value at t_{BE}. For $t \geq t_{BE}$, the leakage power of the proposed ST design becomes even lower than expected. The same holds for the leakage energy consumed by the circuit during its lifetime (Fig. 2(b)).

The proper (initial) ST V_{th} value can be determined accounting for the effect of burn-in test. In fact, stress conditions usually applied during burn-in (high temperature and voltage) can induce a significant NBTI degradation (V_{th} increase). As a result, the leakage power of power gated circuits decreases considerably during burn-in test. Therefore, the initial ST V_{th} can be selected so that the break even point in Fig. 2(a) is reached at the end of burn-in test, further decreasing the leakage energy required during the ST effective lifetime ($t > t_{BE}$ in Fig. 2(b)).

III. Analysis of NBTI Impact on Sleep Transistors

In order to assess the impact of NBTI on power-gated circuits, we considered the power gating approach in Fig. 1(a) applied to two logic blocks: the *b02* benchmark from the *itc99* benchmark suite, and a circuit composed by 10 FO4 cascaded inverters. They have been implemented by a 32nm Metal Gate, High-K Strained-Si CMOS technology [1], with a supply voltage $V_{dd} = 1V$. Particularly, the high V_{th} model has been adopted to implement the pMOS STs, while logic gates have been designed using the low V_{th} model.

To highlight the effect of ST degradation, in our simulations we have not considered the aging of logic transistors. Nevertheless, as introduced in Sec. I, the degradation of STs dominates over that of standard logic [6], since they are under a stress condition for 100% of time during which a power-gated circuit is operating. Similarly to [13], [19], the V_{th} degradation (ΔV_{th}) has been estimated by means of the model in (1) fitted with the experimental results reported in [19] for the 32nm Metal Gate, High-K CMOS technology. The estimated ΔV_{th} values obtained for each considered operating time interval have been utilized to customize the SPICE device model and simulate STs with the proper NBTI degradation.

STs have been sized in order to introduce an IR drop equal to $0.1V_{dd}$ at the beginning of their operating time (hereafter denoted as $t0$). This is a constraint usually assumed by standard power gating approaches neglecting the effect of NBTI [6], [8]–[10], [15]. The obtained values of the ST equivalent aspect ratios $S = (W/L)_{eq}$ are: $S_{b02} = 102$; $S_{NOT} = 35$. Moreover, we have assumed that STs are under a stress condition (ON) for 60% of the operating time ($\alpha = 0.6$ in (1)).

A. NBTI Impact on IR Drop and Circuit Lifetime

When a power-gated circuit is not idle, STs are ON and operate in triode region. Therefore, the equivalent resistance of an active ST transistor can be expressed as:

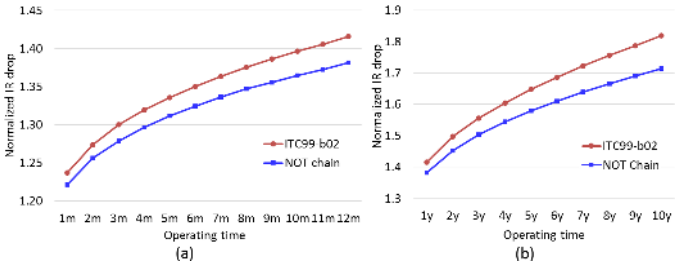

Fig. 3. Profile of the normalized IR drop over time (normalization factors: $IR_{b02}(t0) = IR_{NOT}(t0) = 100mV$) for an operating time of: (a) 1 month - 12 months; (b) 1 year - 10 years.

$$R_{ST} \propto [(W/L)\,\mu_p C_{ox}\,(V_{dd} - V_{th})]^{-1} \tag{2}$$

As a pMOS ST ages and its V_{th} (absolute value) increases, its equivalent resistance increases as well, and so does the IR drop between its source (actual V_{dd} in Fig.1(a)) and drain (virtual V_{dd} in Fig.1(a)) when the current drained by the power-gated circuit flows through it. In order to evaluate the IR drop profile accounting for ST aging, the current drained by the power-gated circuit has been evaluated by means of SPICE simulations as the worst case active current drained at $t0$. The obtained results are shown in Fig. 3(a)(b) for an operating time ranging from 1 to 12 months and from 1 to 10 years, respectively. The IR drop values have been normalized over the value exhibited by the two circuits at $t0$ (0.1V). As can be seen, the IR drop increase exceeds 20% after only 1 month of operation for both considered circuits, approximates 40% after one year, and after 10 years of operation it reaches 72% and 83% for *b02* benchmark and NOT chain, respectively.

As a consequence of IR drop increase with aging, the propagation delay τ of the a power-gated circuit increases as well. This can eventually lead to a delay fault, thus circuit lifetime shortening. Let us define circuit lifetime as the time required by a circuit to degrade its performance by 15% with respect to its worst case propagation delay τ_{wc} at $t0$. In fact, we can consider that a 15% time margin is added to the worst case propagation delay when determining the clock period in order to account for a degradation induced by PVT variations [6]. Denoted by t_{LT} the lifetime of a circuit, it is evaluated so that $\tau_{wc}(t_{LT}) = 1.15 \cdot \tau_{wc}(t0)$. The simulation results for the normalized propagation delay for the two considered circuits are shown in Fig. 4, which reports the delay profiles as a function of circuit lifetime. For each circuit, the normalization factor is the respective τ_{wc} at $t0$. We can see that the propagation delay degrades by more than 6% after the first month of operation, it exceeds more than 10% degradation after 1 year for both circuits, and in 10 years it reaches 20.6% for the NOT chain and 27.2% for the *b02* benchmark. As for lifetime, which has been estimated as previously discussed (Fig.4(b)), it is approximately 2.15 years for the *b02* benchmark, and 3.95 years for the NOT chain.

B. NBTI Impact on Leakage Power

The goal of power gating is to reduce leakage power. Therefore, it is of utmost importance to assess the impact of ST

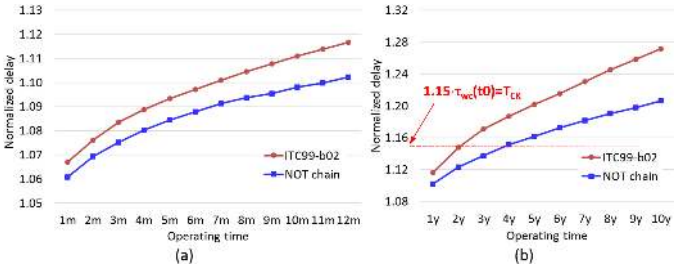

Fig. 4. Profile of the normalized propagation delay over time (normalization factors: $\tau_{wc.b02}(t0) = 59.63ps$; $\tau_{wc.NOT}(t0) = 118.3ps$) for an operating time of: (a) 1 month - 12 months; (b) 1 year - 10 years.

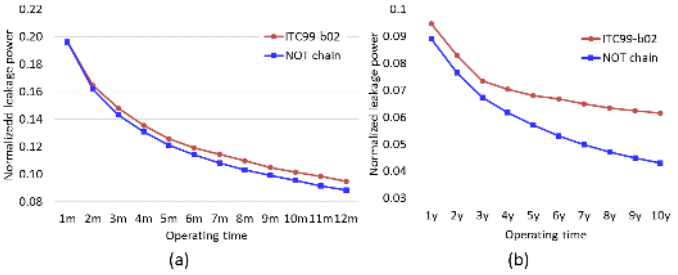

Fig. 5. Profile of the normalized leakage power over time (normalization factors: EP_{leak0}(b02)=62.1pW, EP_{leak0}(NOT)=32.2pW) for an operating time of: (a) 1 month - 12 months; (b) 1 year - 10 years.

aging on power gating effectiveness. For the considered two case studies, when a standard power gating approach using high V_{th} STs is applied, leakage power drops to $62.1pW$ (*b02* benchmark) and $32.2pW$ (NOT chain), with a reduction exceeding 95% with respect to a design without power gating. These two latter values represent the values of the leakage power that designers expect to consume if a standard power gating design flow not accounting for NBTI is considered. We will refer to these values as *expected leakage power at t0*, and we will denote them as $EP_{leak0}(b02)$ and $EP_{leak0}(NOT)$.

Instead, as discussed in the previous section, we expect that leakage power considerably decreases as STs age. This is confirmed by the obtained simulation results shown in Figs.5(a)(b). The leakage power for each of the two considered case-studies has been normalized over the respective EP_{leak0}. After only 1 month of operation, the leakage power drops to less than 20% of that at $t0$ for both circuits. It further reduces to less than 10% after 1 year, and after 10 years of operation leakage power collapses to 4.3% of the EP_{leak0} for NOT chain, and to a value slightly higher than 6.2% of the EP_{leak0} for the *b02* benchmark. Therefore, the obtained SPICE simulation results confirm that the effectiveness of power gating in reducing leakage power increases considerably as STs age.

IV. Proposed Approach for ST Design

Leakage power reduction well below the expected value (EP_{leak0}) due to ST aging has been so far ignored by power gating techniques. We propose to renounce part of this leakage power over-reduction in order to counteract the detrimental effect of ST aging on IR drop and propagation delay, thus improving circuit lifetime and long-term reliability.

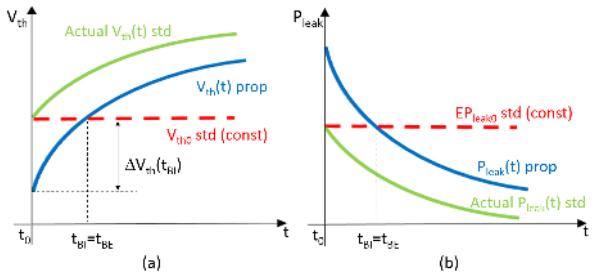

Fig. 6. Schematic representation of the proposed method to determine ST V_{th} optimal value: (a) qualitative V_{th} trend over time for the proposed (prop) and standard (std) ST design, and (b) correspondent leakage power trend.

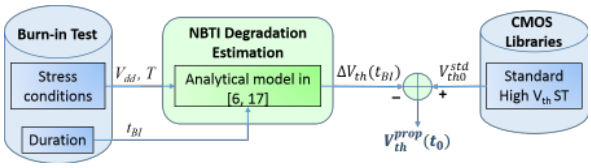

Fig. 7. Flow of the proposed ST V_{th} determination approach.

As introduced in Sec. II, this can be achieved by designing STs with a lower (initial) V_{th}, thus reducing ST resistance, either by re-designing the power switching fabric (device level approach, suitable for the development of future ST fabrics), or by applying a proper forward body bias to available ST fabrics (circuit level approach).

The proper ST V_{th} value can be determined accounting for burn-in test. The stress conditions usually applied during burn-in (high temperature and voltage) induce a significant NBTI degradation (V_{th} increase) [7], [16]. The method to determine the ST V_{th} for the proposed design approach can be qualitatively explained through Fig. 6. Let us denote by t_{BI} the burn-in duration (the initial time instant is set to 0), by $V_{th}^{prop}(t0)$ the initial threshold voltage value of the proposed STs, and by V_{th0}^{std} the initial threshold voltage value of a standard high V_{th} ST. The ST threshold voltage $V_{th}^{prop}(t0)$ is selected so that, as a consequence of NBTI degradation, V_{th}^{prop} reaches V_{th0}^{std} (break-even point) at the end of the burn-in test (at $t_{BI} = t_{BE}$ in Fig. 6(a)). In fact, it is:

$$\begin{aligned} &P_{leak}^{prop}(t_{BI}) = EP_{leak0} \iff \\ &\iff V_{th}^{prop}(t_{BI}) = V_{th0}^{std} \end{aligned} \tag{3}$$

This way, the leakage power exhibited by a circuit during its effective lifetime ($t > t_{BE}$ in Fig. 6(b)) turns out to be considerably lower than expected. The flow of the proposed method is represented in Fig. 7. The threshold voltage degradation during burn-in test, denoted by $\Delta V_{th}(t_{BI})$, can be properly estimated given burn-in stress conditions (temperature and voltage) and duration by means of the model in [7], [17] (whose simplified formulation is given in (1)). The threshold voltage V_{th0}^{std} is extracted from the used CMOS library. The (initial) threshold voltage of the ST for the proposed design approach is then computed as: $V_{th}^{prop}(t0) = V_{th0}^{std} - \Delta V_{th}(t_{BI})$.

Different stress conditions and duration may characterize burn-in test. Let us consider possible values reported in [3]:

- Stress conditions: $T = 105°$C, $V_{dd} = 1.3$V;

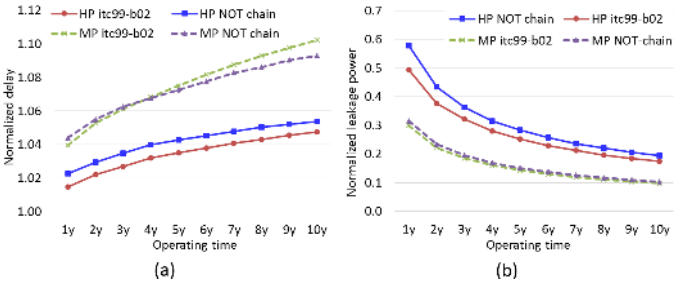

Fig. 8. Profile over time of (a) normalized propagation delay (normalization factors: $\tau_{wc.b02}(t0) = 59.63ps$; $\tau_{wc.NOT}(t0) = 118.3ps$) and (b) normalized power leakage (normalization factors: EP_{leak0}(b02)=62.1pW, EP_{leak0}(NOT)=32.2pW).

TABLE I
LIFETIME (LT) INCREASE AND AVERAGE LEAKAGE POWER VARIATION OVER A STANDARD DESIGN ($\Delta = [(HP, MP) - Std]/Std$)

Circuit	Std design		HP design		MP design	
	LT	$P^{av}_{leak}(pW)$	LT ext.	ΔP^{av}_{leak}	LT ext.	ΔP^{av}_{leak}
b02 bench.	2.15y	18.4	25.1×	-20.1%	10.2×	-22.8%
NOT chain	3.95y	6.3	20.2×	-9.5%	8.3×	-12.6%

- Possible duration: $t_{BI1} = 10h$; $t_{BI2} = 100h$.

The following values of V_{th} degradation are obtained: $\Delta V_{th}(t_{B1}) \simeq 47mV$, $\Delta V_{th}(t_{B2}) \simeq 70mV$. The two corresponding V_{th} values are ($V^{std}_{th0} = 0.581mV$ for the considered device model [1]): $V^{prop}_{th1}(t0) = 0.534V$, hereafter referred to as MP (medium performance) ST design; $V^{prop}_{th2}(t0) = 0.511V$, hereafter referred to as HP (high performance) ST design.

V. VALIDATION RESULTS

The proposed ST design approach has been validated by means of SPICE simulations. To this end, the same simulation set-up as that described in Sec. III has been considered. In Fig. 8(a) we report the results for the propagation delay of the two considered case studies for lifetime in the range 1-10 years. The delay values are normalized over the respective values at $t0$ for the high V_{th} ST designs. The equivalent aspect ratios of the STs are those determined in Sec. III: $S_{ST.b02} = 102$ and $S_{ST.NOT} = 35$. As can be seen, the normalized delay is in the range 1.09-1.11 for the MP designs, while it is between 1.03 and 1.04 for the HP designs. Therefore, for all considered operating time interval, the normalized propagation delay is considerably lower than time reference utilized to estimate circuit lifetime (1.15), as discussed in the Sec. III. Fig.8(b) shows the leakage power trend over time for the two considered circuits, normalized over the respective value of EP_{leak0}. We can see that, after only 1 year of operation, the leakage power consumption is considerably lower than the value estimated without considering NBTI effect, reaching 31% of EP_{leak0} for MP design, and 40%-50% of EP_{leak0} for HP design. After 10 years of operation, the leakage power drops to 10% of EP_{leak0} for MP design, and to less than 20% of EP_{leak0} for HP design.

In Table I we report the lifetime increase ('LT ext.') compared to a standard (Std) approach. It ranges from 10.2× (8.3×) for the *b02* benchmark (NOT chain) adopting an

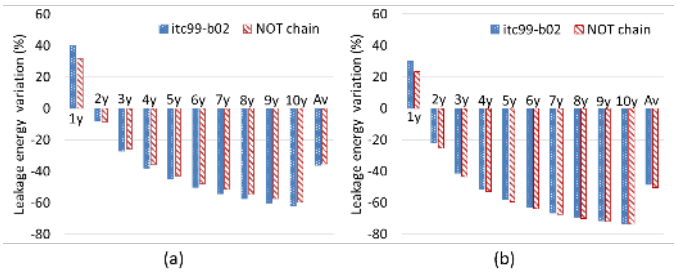

Fig. 9. Leakage energy variation over time of the proposed (a) HP ST design and (b) MP ST design, over the standard ST design.

MP ST design, to 25.1× (20.2×) for the HP ST design. Differently from previous solutions in [6], [18] based on ST oversizing possibly combined with adaptive body bias, the increase of circuit LT and long-term reliability can be pursued with no area overhead with respect to standard power gating techniques. The relative variation of the average leakage power is also reported. For each ST design (Std, HP, MP) the average leakage power has been computed as the value of the total leakage energy consumed by circuit over the achieved maximum LT. For both MP and HP ST design, a considerable reduction of the average leakage power is exhibited, ranging from 9.5% to 22.8%.

The energy efficiency of the proposed ST design approach has been assessed also by evaluating the leakage energy variation with respect to the value expected by a standard (NBTI-unaware) power gating technique, for a circuit LT up to 10 years. The leakage energy consumption for $t < t_{BE}$ (Fig. 2) has been also accounted for. The obtained results are depicted in Fig. 9(a)(b) for the HP and MP ST design, respectively. During the considered 10 year LT, the average reduction ranges from of 35.3% (NOT chain with HP ST) to 50.5% (NOT chain with MP ST). It should be noted that, exhibiting a lower resistance, the proposed STs will also enable a reduction of energy dissipated due to Joule effect during their ON state, thus reducing thermal issues.

The improvement reported in Table I would lead to a circuit lifetime exceeding 30 years. However, for many applications it is not of interest to extend the circuit lifetime for such a long period. Therefore, let us consider 10 years as maximum target lifetime, which represents a 4.92× extension for the *b02* benchmark, and 2.45× extension for the NOT chain with respect to the standard power-gating approach, as evaluated in Sec. III. The identification of a lifetime target enables to either increase the operating frequencies, thus improving performance, or reduce the equivalent size of the STs, thus reducing ST area overhead compared to a standard power gating approach. Let us first suppose to keep the size of the STs fixed at the values considered so far ($S_{ST.b02} = 102$, $S_{ST.NOT} = 35$). Table II reports the obtained results for the operating frequency increase. As can be seen, the operating frequency for the HP ST design can be increased by 10.5% (9.78%), for the *b02* benchmark (NOT chain) with respect to a standard ST design. With an MP ST design, 4.23% (4.93%) frequency increase for the *b02* benchmark (NOT chain) can

TABLE II
OPERATING FREQUENCY INCREASE FOR 10 YEAR LT

Circuit	Std design	HP design@10y		MP design@10y		LT ext.
	T_{CK}	T_{CK}	Δf_{CK}	T_{CK}	Δf_{CK}	
b02 bench.	68.6ps	61.4	10.3%	65.7ps	4.23%	4.92×
NOT chain	136.0ps	122.7ps	9.63%	129.3ps	4.93%	2.45×

TABLE III
ST AREA REDUCTION FOR 10 YEAR LT

Circuit	Std design	HP design@10y		MP design@10y		LT ext.
	S_{eq}	S_{eq}	ΔA_{ST}	S_{eq}	ΔA_{ST}	
b02 bench.	102	81	20.6%	93	8.8%	4.92×
NOT chain	70	55	21.4%	63	10%	2.45×

be achieved. Alternatively, a reduction of the equivalent ST size can be pursued. In this case, the clock periods for the two considered circuits are the same as those calculated in Sec. III. The obtained results are reported in Table III. The HP design enables 20.6% (21.4%) ST area reduction for the *b02* benchmark (NOT chain), while the MP design offers 8.8% (10%) ST area reduction. An analogous reduction of leakage power is exhibited.

We further validated the proposed ST design considering benchmarks *c432*, *c499* and *c1355* from ISCAS85 benchmark suite. The obtained SPICE simulation results confirmed those for *b02* benchmark and NOT chain. They are reported in Table IV. As can be seen, an average $19.9\times$ ($9.2\times$) LT extension for the HP (MP) design can be achieved, with a 12.2% (14.4%) average leakage power reduction. These results, obtained with no additional ST area, represent an improvement with respect to those reported [6], [18] (obtained for different technologies and different power gating strategies), which also imply an increase of ST area overhead with respect to a standard power gating technique. Moreover, if a 10 year LT target is considered, either an average 9.53% (4.4%) increase of operating frequency, or a 18.4% (8.1%) ST area reduction with respect to a standard power gating approach can be achieved.

VI. CONCLUSIONS

We showed that, as sleep transistors (STs) degrade, their leakage power drastically decreases, making power gating techniques more effective over time. Based on this feature, we proposed a new ST design approach for reliable and energy efficient power gating which offers better cost-reliability trade-offs compared to standard approaches based on ST oversize. Through SPICE simulations, we showed a lifetime (thus long-term reliability) improvement up to $19.9\times$ and average leakage power reduction up to 14.4% compared to standard STs design approach, with no additional area overhead. Moreover, if a maximum target lifetime of 10 years is considered, our proposed ST design approach enables either to improve circuit operating frequency up to 9.53% or to reduce ST area overhead up to 18.4%.

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TABLE IV
LT EXTENSION AND AVERAGE P_{leak} VARIATION OVER A STANDARD ST DESIGN, AND POSSIBLE FREQUENCY/AREA OPTIMIZATION FOR LT=10Y

Circuit	HP		MP		HP@10y		MP@10y	
	LT ext	ΔP_{leak}^{av}	LT ext	ΔP_{leak}^{av}	Δf_{CK}	ΔA_{ST}	Δf_{CK}	ΔA_{ST}
c432	19.1×	-12.1%	9.5×	-15.2%	9.7%	-18.9%	5.1%	-8.8%
c499	21.4×	-14.4%	9.8×	-16.3%	9.5%	-17.4%	3.5%	-8.2%
c1355	20.2×	-10.1%	8.3×	-11.7%	9.4%	-19.0%	4.5%	-7.3%
avg	19.9×	-12.2%	9.2×	-14.4%	9.53%	-18.4%	4.4%	8.1%

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