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Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices

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One of the most important degradation effects observed in MNOS memory transistors is a negative shift of the threshold window. This negative shift is caused by a strong increase of the density of Si-SiO_2 surface traps. This effect has been proposed to be caused by the same effect that is observed in MOS devices subjected to negative-bias stress (NBS). In this paper, a detailed study of the increase of the number of surface traps in MOS structures after NBS at temperatures (25–125°C) and fields (400–700 MV/m) comparable to those used in MNOS devices is presented. Two different behaviors are observed. At low fields the surface-trap density increases as $t^{1/4}$ and at high fields it increases linearly with the stress time t. The low-field behavior is temperature and field dependent and the zero-field activation energy is determined to be 0.3 eV. The high-field behavior is strongly field dependent but independent of temperature. A physical model is proposed to explain the surface-trap growth as being diffusion controlled at low fields and tunneling limited at high fields. A comparison with MNOS degradation is made and it was found to be related to the $t^{1/4}$ behavior mentioned above.

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I. INTRODUCTION

The use of the MNOS nonvolatile memory device as a read/write memory is limited to a certain number of write/erase cycles (~10^6–10^{12} cycles).[1,2] Frequent write/erase cycles introduce changes in device properties due to the high oxide field (700–1600 MV/m). The two most important degradation effects observed in p-channel MNOS transistors are a negative shift of the threshold window (up to 10 V) and a decrease in the retention time. The negative shift of the threshold window is caused by a large increase in the density of the Si-SiO_2 surface traps.[1–3]

It is well known that surface traps are created at the Si-SiO_2 interface of an MOS capacitor when negative bias is applied to the gate at elevated temperatures.[4,5] This negative-bias stress (NBS) effect has been proposed to be the same effect that causes the degradation of MNOS devices repeatedly operated at high write/erase gate voltages.[1]

The NBS effect at elevated temperature (250–300°C) was examined by Deal *et al.*[4] and by Goetzberger *et al.*[5] They found that both the surface-trap density N_{st} and the surface-charge density Q_{ox} increased upon negative-bias stress. The increases of N_{st} and Q_{ox} were very similar and were found to be logarithmic in time. Furthermore, the increase was nearly proportional to the applied field (0–300 MV/m) and was larger at higher temperatures.

This work extends the measurements on the NBS effect in MOS capacitors to temperatures (25–125°C) and fields (400–700 MV/m) more typical for the operation of MNOS devices. When an MOS capacitor is subjected to NBS it is not too surprising that charge may be trapped at the Si–SiO_2 interface. It is much more interesting that new surface traps are actually created during NBS. We believe that this may not happen unless the atomic structure is changed at the interface. Therefore, our measurements are focused on the surface traps. The NBS behavior of MOS capacitors is characterized through studies of the time dependence of the surface-trap formation at different stress voltages and temperatures. Two mechanisms are observed to create new surface traps during NBS. The first mechanism, which is believed to be diffusion controlled, is presented schematically and the time dependence of this type of process is shown to agree with experiments. The other mechanism, which is dominant at very high fields, is a hole tunneling process. After evaluation of the measurements, possible electrochemical reactions which could occur at the Si-SiO_2 interface are discussed. Finally, the NBS behavior of MOS capacitors is compared to the degradation behavior of MNOS capacitors which is more complex to evaluate.

II. SAMPLE PREPARATION

The NBS measurements were performed on MOS samples fabricated on ⟨100⟩ 2–3-Ω cm n-type silicon wafers. A typical high-quality MOS sample was first cleaned in H_2O_2-NH_3 and H_2O_2-HCl, and then rinsed in double-distilled water water followed by a 30-s dip in 48% HF and a final short rinse in double-distilled water. An oxide layer of about 950 Å was grown in dry oxygen in a resistance-heated furnace (1200°C, 12 min). The metal gate contacts were e-gun-evaporated aluminum contacts in order to reduce the Na^+ ion content. The electrodes are circular dots with a 700-μm diameter (area 3.85×10^{-7} m^2). Radiation damage was annealed in forming gas (10% H_2, 90% N_2) for 10 min at 500°C.

For comparison of the NBS effect in MOS samples with the degradation effect in MNOS memory devices, MNOS capacitors were fabricated and exposed to high-field stress. The fabrication process of these MNOS samples has been described elsewhere.[6]

The MNOS samples were fabricated on ⟨100⟩ 0.8–1.2-Ω cm n-type silicon wafers. These were cleaned the same way as above but dipped for 2 min in 48% HF before a 30-s rinse in double-distilled water. At this stage the thickness of the residual oxide was 8–10 Å according to ellipsometer measurements. A thin oxide

layer (about 20 Å) was then grown in dry oxygen in a resistance-heated furnace at a temperature of about 600 °C for 15 min. The oxide thickness was again measured by ellipsometer, after which the slice was placed in the nitride reactor. The nitride layer was deposited at 725 °C and was then annealed in argon at 900 °C for 15 min. The metal gates on the MNOS devices were 250×500-μm (1.25×10^{-7} m^2) Cr-Au dots.

III. MEASUREMENTS AND EVALUATION OF NEGATIVE-BIAS STRESS

Negative-bias stress (NBS) of an MOS capacitor generally means that a negative voltage is applied to the metal gate for a certain time at a certain stress temperature in the range from room temperature (RT = 25 °C) up to 300 °C. In our experiments the temperature was limited to the range 25—125 °C which is typical for the operation of MOS devices. The voltage range was 40—66 V corresponding to 400—700 MV/m on our 950-Å samples. After stress, the sample is cooled to room temperature with the gate floating. Changes in the interface properties are measured with the C-V technique, which includes recording of a high-frequency and a quasistatic low-frequency capacitance curve.

A standard experimental setup for stress and C-V measurements was used. The MOS capacitor was placed on a nickel pedestal which was resistively heated to the stress temperature. Good electrical and thermal contact to the back side was provided by a thin layer of In-Ga which is liquid at RT. The stress voltage was applied to the metal gate through a thin gold wire probe. After stress the sample was cooled to RT and the high-frequency (1 MHz) capacitance was measured with a Boonton 72B Capacitance Bridge. The low-frequency quasistatic C-V curve was measured with a Keithley 610C Electrometer using the slow-ramp technique (sweep rate ~60 mV/s).[7,8]

From the measured C-V plots, the surface-trap density N_{st} may be calculated from the following relationship[7]:

$$N_{st}=\frac{C_{ox}}{qA}N_r, \tag{1}$$

where

$$N_r=\frac{C_{LF}/C_{ox}}{1-C_{LF}/C_{ox}}-\frac{C_{HF}/C_{ox}}{1-C_{HF}/C_{ox}}, \tag{2}$$

C_{ox} is the oxide capacitance, q is the electronic charge, A is the MOS-capacitor area, N_r is the relative surface-trap density, C_{LF} is the quasistatic capacitance, and C_{HF} is the 1-MHz capacitance.

If the C-V plots are recorded on a normalized scale, the relative surface-trap density N_r is easily calculated and the values of N_r are sufficient in order to study the changes of the surface-trap density. The smallest measureable value of N_r is about 0.04. With an oxide thickness of 950 Å, $C_{ox}/qA=2.2\times10^{11}$ cm^{-2}eV^{-1}, which means that surface-trap densities $>10^{10}$ cm^{-2}eV^{-1} may be determined with this method.

A typical set of C-V curves recorded with increasing accumulated stress time as parameter is shown in Fig. 1. Normally, only the relative surface-trap density at midband was evaluated from such curves. The changes in the midband relative surface-trap density during negative-bias stress is discussed in more detail in Secs. IV—IX.

Selected measurements were fully evaluated using a Wang 600 to calculate the energy distribution of the surface-state density. The energy range is limited on one side by the flatband condition, and on the other side by the onset of inversion. Near flatband, the high-frequency capacitance curve is influenced by the surface traps since their time constants become too short. The surface potential was calculated through integration of the low-frequency curve as described by Berglund.[9] The undetermined additive constant was determined through calculation of the ideal midband capacitance. This determination agreed very well with the one obtained when the integrated energy range was adjusted symmetrically to the middle of the energy band. The inversion and flatband points were easily determined since they lie ± 0.3 eV from midband (for a doping concentration of 1.5×10^{15} cm^{-3}).

The surface potential is most accurately determined from the C-V plots measured before stress. Since the relationship between the surface potential and the high-frequency capacitance is independent of the number of surface traps, it is not necessary to integrate the low-frequency curve after each stress cycle. A full evaluation of the stress results shown in Fig. 1, following these guidelines, is presented in Fig. 2. The increase in the surface-trap density as a result of negative-bias stress is shown in the energy range from flatband to inversion.

IV. BEHAVIOR OF SURFACE TRAPS

The time dependence of the surface-trap generation during negative-bias stress was studied at different stress voltages and temperatures. As mentioned above, our attention was focused on the relative surface-trap

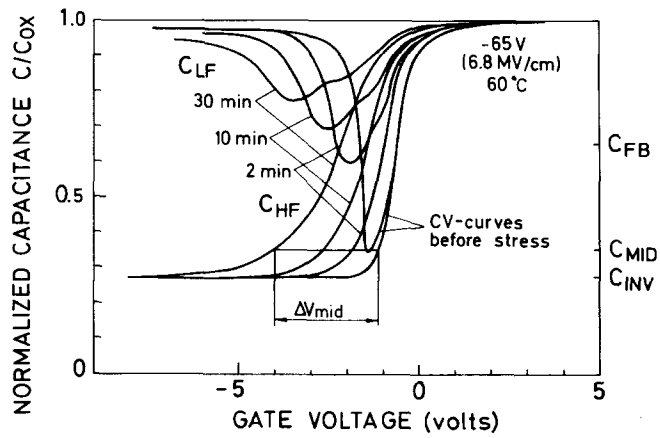


FIG. 1. A typical set of C-V curves recorded with increasing accumulated stress time as parameter. The right-most curve pair is recorded before stress and indicates low surface-trap density. As stress time increased (curves are recorded after 2, 10, and 30 min of NBS) the quasistatic (C_{LF}) and the 1-MHz (C_{HF}) C-V curves diverge and indicate an increasing surface-trap density.

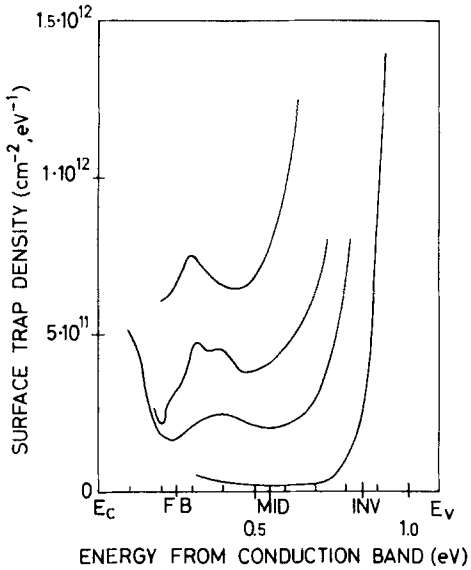


FIG. 2. A full evaluation of the stress results in Fig. 1 showing the energy distribution of the surface-trap density and its increase after NBS with stress time as parameter.

density at midband, which made data evaluation fast and simple.

The most extensive stress measurements were performed on the same high-quality MOS sample. For this sample the stress field was in the range 4—7 MV/cm, where the upper limit was set by destructive breakdown of the MOS structure. Measurements were made at three different stress temperatures 25, 60, and 125 °C. Some results are shown in Fig. 3. Each curve was obtained from a separate capacitor on the same sample (oxide thickness 950 Å).

When the NBS effect was examined by Deal *et al.*, they studied the increase of the fixed oxide charge. They found that this increase generally was accompanied by an equal amount of growth in the number of surface traps. As mentioned above, our measurements are focused on the number of surface traps, but they confirm the observation[4,5] that there is an equal growth

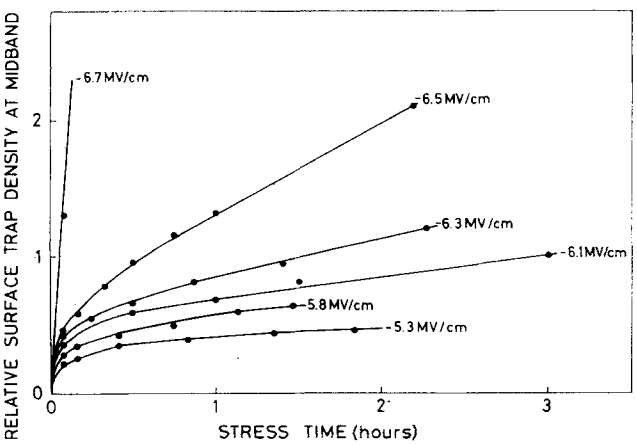


FIG. 3. Relative surface-trap density at midband and its increase with stress time for different NBS fields at room temperature (25 °C) (d_{ox} = 950 Å).

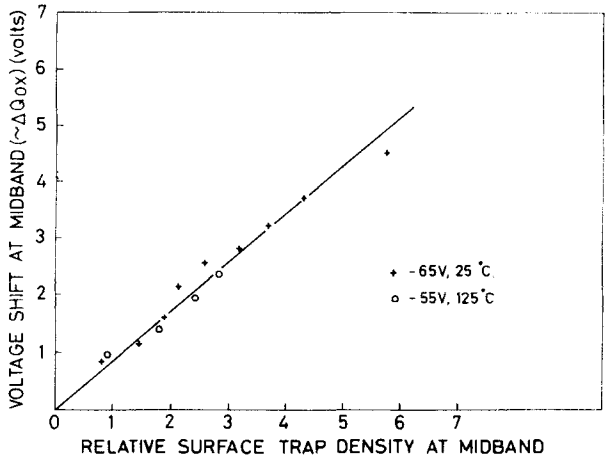


FIG. 4. The increase of the oxide charge measured as the shift of the C-V curve at midband, plotted against the relative surface-trap density at midband. The same relationship is observed after NBS at both 125 °C, −55 V (5.8 MV/cm) and 25 °C, −65 V (6.8 MV/cm) and indicates that there is roughly one surface trap per oxide charge.

of the fixed oxide charge and the surface-trap density independent of the NBS conditions. A typical plot of the growth of the fixed oxide charge, measured as the midband voltage shift, versus the midband surface-trap density is shown in Fig. 4. This plot shows the same relationship independent of NBS fields and temperatures.

The surface traps that are created during NBS can be removed by annealing. If a capacitor which has been exposed to NBS at a certain stress temperature remains at that temperature with the gate grounded, the number of surface traps slowly decreases to a new level of surface-trap density. If the annealing temperature is then increased, the number of surface traps further decreases to a new level as depicted in Fig. 5.

After NBS, even with very short stress times, some capacitors showed a strongly increased leakage current during recording of the quasistatic C-V curve. This phenomenon occurred following stress at very high voltage, particularly at room temperature. However, if such a capacitor was left with the gate voltage sweep-

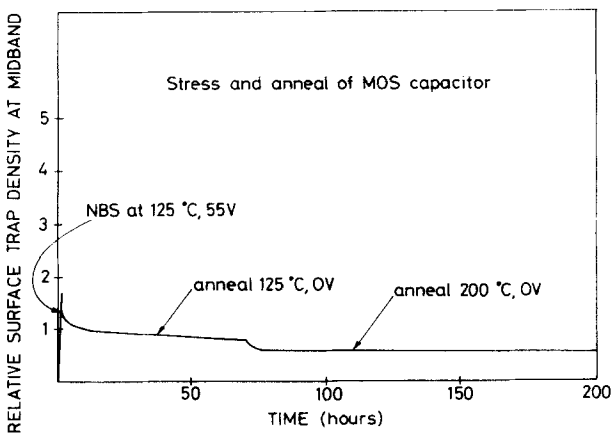


FIG. 5. The behavior of an MOS capacitor that is stressed at 125 °C, −55 V for a short time and thereafter annealed at 125 and 200 °C. The relative surface-trap density is shown against time.

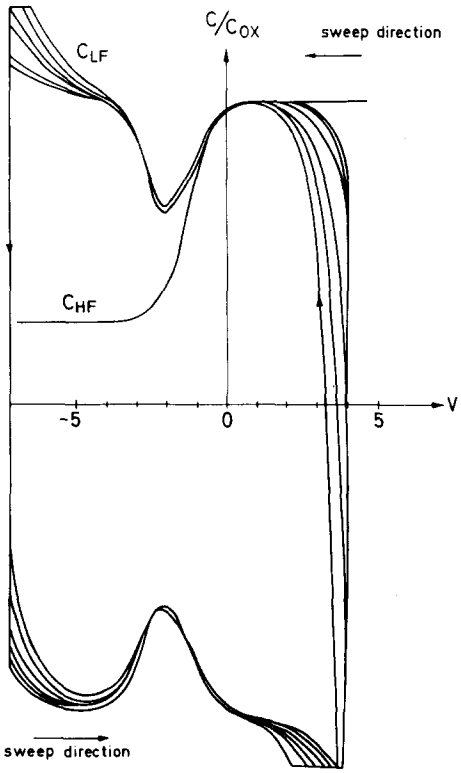


FIG. 6. Quasistatic *C-V* curves recorded after 10 min of NBS with −65 V at 25 °C. These recordings are a few of the set of curves that were recorded continuously during 1 h after stress. They show a leakage current that is decreasing with time. Is this a hydrogen-ion leakage current?

ing back and forth while the quasistatic C-V curve was continuously recorded, the leakage current slowly disappeared, as shown in Fig. 6. This leakage current may be an ion drift current, possibly by hydrogen ions.

V. DISCUSSION OF MEASUREMENTS

To our knowledge, no model for surface-trap generation has been published. Surface traps are usually believed to be either induced by charge trapped at the interface, or due to broken chemical bonds. Since the charge model is very vague in explaining surface traps in the middle of the bandgap, we believe that surface traps cannot be formed unless the atomic structure is changed at the interface. Therefore we propose a chemical model for formation of surface traps.

Goetzberger *et al.*[5] found that the surface-trap density increased as the logarithm of time at 250 and 300 °C. Their reason for choosing a logarithmic plot is according to Walden's[10] theory of charge trapping in an insulator. However, Walden is mathematically treating electron (or hole) injection to traps located well inside the insulator and this phenomena is not directly connected with the generation of surface traps.

Based on our measurements, we believe this generation to be diffusion controlled, as discussed later. Our mathematical treatment gives a $t^{1/4}$ time dependence. This is very similar to a logarithmic behavior over a few decades, so the data of Goetzberger *et al.* also fit this time dependence.

Our measured values are plotted against $t^{1/4}$ in Fig. 7 for 25 and 125 °C with the stress field as parameter. It is clearly seen that N_{st} increases as $t^{1/4}$ at 125 °C which is in agreement with Goetzberger's high-temperature results. At room temperature the $t^{1/4}$ dependence is valid for low stress voltages. For high stress voltages it is valid only during a limited initial stress time. For stress fields larger than 6.3 MV/cm the $t^{1/4}$ dependence is no longer valid. Instead the formation of surface traps becomes linear in time.

VI. MODEL FOR NBS EFFECT

In our model we assume that the silicon interface contains a large number of defects which are electrically inactive, but may become electrically active upon stress. This activation is assumed to take place through a chemical reaction. The existence of similar electrochemical reactions has been proved by Nicollian *et al.*[11]

A scheme which explains the $t^{1/4}$ mechanism is

$$\text{(surface defect)} \rightleftharpoons \text{(surface trap)} + \text{(surface charge)}^{+} + X_{\text{interface}} + e^{-}\text{(to the silicon)} \tag{3a}$$

$$X_{\text{interface}} \overset{\text{diffusion}}{\rightleftharpoons} X_{\text{bulk}}. \tag{3b}$$

In this process a diffusing species X is formed at the interface when the surface defect is electrically activated. A surface trap and a surface charge are then left at the defect site in fixed positions close to each other. The process is field dependent since a transfer of charge takes place. It agrees with the observations that equal numbers of surface traps and surface charges are produced.

The observed $t^{1/4}$ behavior of the surface-trap density N_{st} suggests that the survival of a created surface trap is diffusion controlled. This means that a stable surface trap is only formed if the species X diffuses away from the interface into the oxide (see the Appendix).

If the process is controlled by the rate at which X diffuses away from the interface into the oxide, it may be shown (this is done in the Appendix) that the surface-trap density increases as

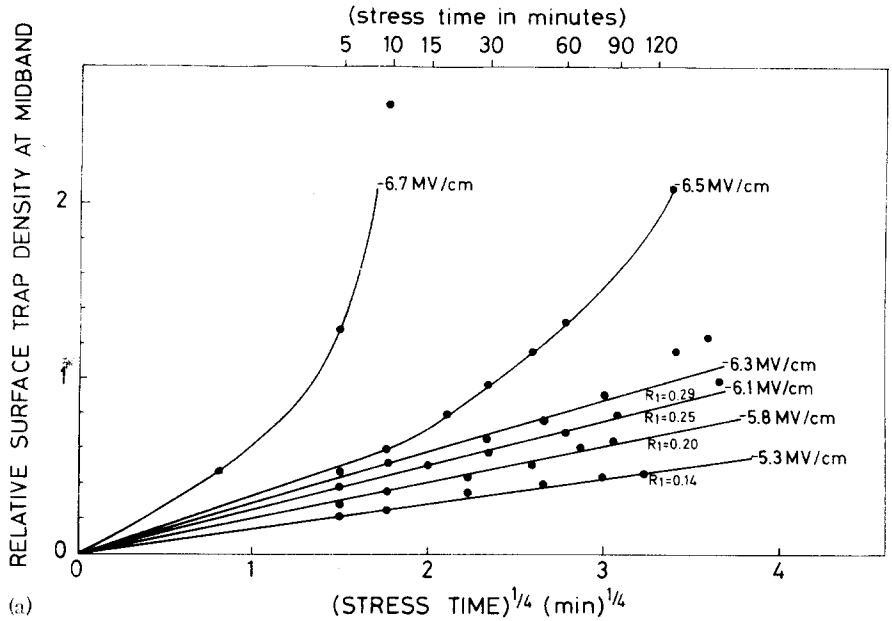
$$N_{st} = R_1 t^{1/4} \tag{4a}$$

Here, t is the stress time and R_1 is the rate constant of surface-trap formation. For the relative surface-trap density N_r we may write

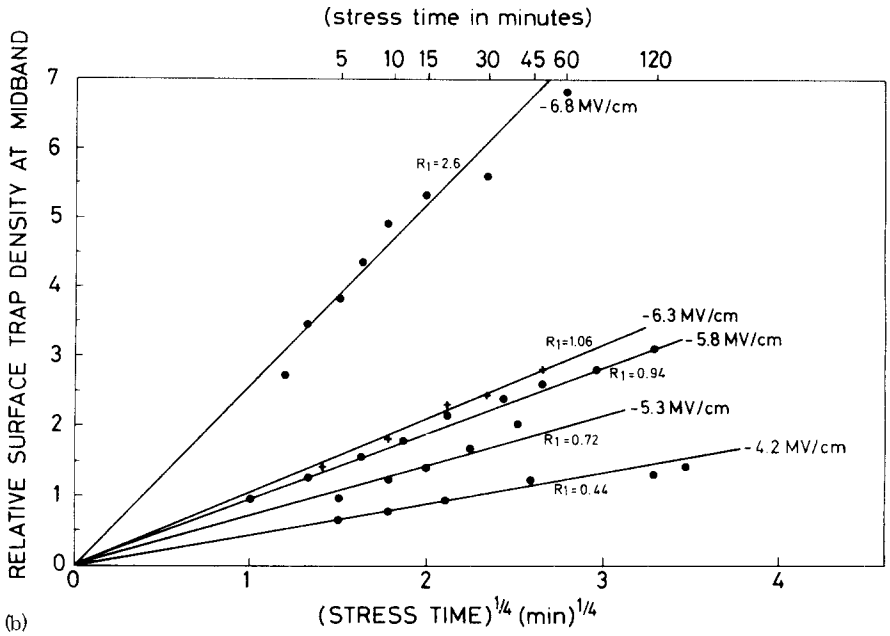
$$N_r = R_1' t^{1/4}, \tag{4b}$$

where $R_1' = (qA/C_{ox})R_1$ is the relative rate constant.

The time dependence of this process thus explains our observations at low fields. However, in this schematical process the actual defects have not yet been identified. Since infrared measurements have shown that large numbers of Si-H groups exist in the bulk SiO_2 and probably also in very large numbers at the interface,[12,13] we believe that the surface defect in scheme (3) is an $\equiv Si_s$-H group at the silicon interface. (Si_s indicates a silicon surface atom bonded to three other silicon atoms.) For the activation of this defect we



(a)



(b)

FIG. 7. Relative surface-trap density at midband plotted against (stress time)$^{1/4}$ for different NBS fields ($d_{ox} \approx 950$ Å). (a) at room-temperature (25 °C), (b) at 125 °C.

propose the following reaction which is based on a discussion by Revesz[14] on possible chemical reactions at the interface of a Si-SiO_2 system. This reaction is equivalent to process (3):

$$\underset{\text{defect}}{\equiv Si_s\text{-}H} + \equiv Si_o\text{-}O\text{-}Si_o\equiv \rightleftharpoons \underset{\substack{\text{surface}\\\text{trap}}}{\equiv Si_s^{\cdot}} + \underset{\substack{\text{oxide}\\\text{charge}}}{\equiv Si_o^{+}} + \underset{X \text{ to Si}}{\equiv Si\text{-}OH} + e^{-}\,, \qquad (5)$$

where Si_o is a silicon atom in the oxide.

When the defect is activated, the hydrogen, which is weakly bonded to the Si_s atom, reacts with the SiO_2 and forms an OH group bonded to an oxide Si_o atom, leaving one trivalent Si_o^+ in the oxide and one trivalent $Si_s^{\cdot}$ at the silicon surface. This chemical reaction is schematically represented in a two-dimensional model in Fig. 8.

The credibility of this reaction is supported by many facts. The silicon surface trivalent $Si_s^{\cdot}$ is assumed to form the surface trap, in agreement with many earlier suggestions.[14–16] The Si_o^+ is a charged trivalent oxide Si atom bonded to three oxygens. Such a defect is a good candidate for the oxide charge defect.[14,17] The silanol group Si-OH finally is known to be a relatively fast-diffusing group in SiO_2 and is normally introduced into the oxide by water decomposition.[11–13] Furthermore, the diffusion constant is known for OH in SiO_2; using the data given in Ref. 13, $D \approx 2.5\times10^{-18}$ m^2/s at 125 °C. This may be compared to the limit of validity of our theory, $D \lesssim W^2/4t = 10^{-18}$ m^2/s (see the Appendix). It is clear that OH is a good candidate for our X. We may also note that the diffusion constant of hydrogen in SiO_2 is expected to be considerably larger. A value of 10^{-13} m^2/s at 125 °C can be deduced from data in Ref. 18 (probably H_2 diffusion) and a large value of the dif-

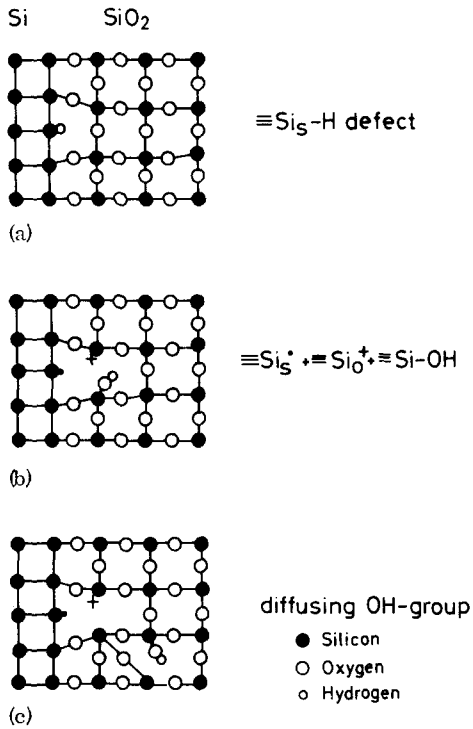


FIG. 8. Schematic two-dimensional representation of the Si-SiO_2 interface, showing (a) the ≡Si-H defect, and (b) how this defect may be electrically activated during NBS to form a surface trap, an oxide charge, and a hydroxyl group, that (c) may diffuse in the oxide and be the reaction-limiting factor. (Si_s means a silicon atom at the surface bonded to other silicon atoms, while Si_o means a silicon atom in the oxide.)

fusion constant of H is necessary to explain why the electrochemical charging effect observed by Nicollian *et al.*[11] was not diffusion limited.

According to reaction (5), the surface charge is located in the oxide a distance a from the silicon surface. Therefore we expect the enthalpy of the reaction to decrease in an electric field E_s, since an electron is transferred from the oxide-charge position into the silicon. The energy qaE_s gained by the electron is reflected in the expression for the rate constant (see the Appendix)

$$R_1' = R_{10}' \exp[-(q/kT(\phi_0 - \tfrac{1}{2}aE_s)], \tag{6}$$

where ϕ_0 is the zero-field activation energy and R_{10}' is a constant. For the NBS conditions in Fig. 7 where the $t^{1/4}$ behavior is valid, the slope of the straight line was taken as the rate constant of surface-trap formation. This rate, R_1', is plotted in Fig. 9 as a function of stress field with the stress temperature as parameter.

The field and temperature dependence found in Fig. 9 agrees very well with the diffusion theory [Eq. (6)]. From Fig. 9 we obtain $a = 3.2$ Å, and by replotting the data against $1/T$ we estimate $\phi_0 = 0.3$ eV. These values are compatible with the above model since a is expected to be about 3.1 Å, which is the Si-O-Si distance in SiO_2 (ϕ_0 is discussed in the Appendix).

VII. ANNEALING OF CREATED SURFACE TRAPS

According to the above model, the created surface traps can only be annealed out again if the species X diffuses back to the interface. Therefore, the annealing process will also be diffusion limited. According to the Appendix, we expect the surface-trap density after degradation to decrease as

$$N_{st} = R_1[t^{1/4} - (t - t_d)^{1/4}], \quad t > t_d, \tag{7}$$

where degradation is assumed to start at $t = 0$ and stop at $t = t_d$.

However, this formula assumes that each surface trap is formed when a species X diffuses away from the interface and that each of these can return to their original site. Probably it is more reasonable to assume that only a fraction γ of the formed surface traps can be annealed by this mechanism. The remaining fraction $1 - \gamma$ either corresponds to species X which have been trapped in the oxide (e.g., by chemical bonding to other oxide defects) or to surface traps that were created by other mechanisms (this will be discussed in Secs. VIII and IX). We would therefore expect N_{st} to anneal out as

$$N_{st} = \gamma R_1[t^{1/4} - (t - t_d)^{1/4}] + (1 - \gamma)R_1 t_d^{1/4}, \quad t > t_d, \tag{8}$$

where $\gamma < 1$.

When annealing for long times (and/or high temperatures) the surface-trap density N_{st} may also decrease through other mechanisms, especially by the introduction of diffusing species X or other species from the outside (either from the metal or the ambient).

The stress and anneal data in Fig. 5 was further evaluated and $R_1' = 0.85$ was found during degradation. The surface-trap density N_r during annealing is plotted against $[t^{1/4} - (t - t_d)^{1/4}]$ in Fig. 10. It is shown that only a fraction $\gamma = 0.32$ of the created surface traps was annealed out as suggested above.

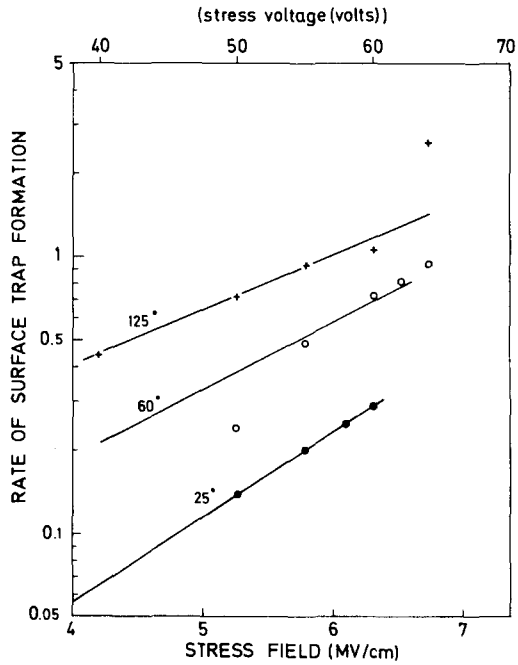


FIG. 9. The relative rate of surface-trap formation R_1' ($t^{1/4}$ region) is plotted against the NBS field for the three different NBS temperatures.

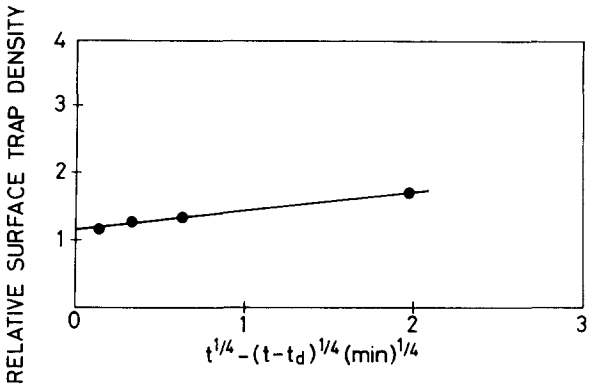


FIG. 10. The relative surface-trap density is plotted against $t^{1/4}-(t-t_d)^{1/4}$, where t_d is the stress time ($t_d = 15$ min) and t is the time elapsed since start of NBS.

VIII. DEGRADATION MECHANISMS AT HIGH FIELDS

For high stress voltages, particularly at low temperatures, N_r appears to increase linearly with time. This is clearly shown in Fig. 3. A linear rate constant R_2 was defined for the surface-trap growth in this NBS region. The rate constant R_2 appears to be independent of stress temperature but strongly dependent of stress voltage which suggests that the rate is limited by a tunneling process. Such a process may be hole tunneling from the silicon valence band into silicon dioxide hole traps (see Fig. 11).

$$(\text{oxide defect}) + h^+ \rightleftharpoons (\text{oxide defect})^+. \tag{9}$$

The charged oxide defect must then be able to create a surface trap. This is certainly possible, since it has been observed to happen during irradiation of MOS structures. Kjar and Nichols[19] have clearly shown that surface traps are created with the same rate as oxide charge during irradiation of MOS structures. Powell and Derbenwick[20] have further shown that such irradiation effects can occur as a result of hole injection only. It is therefore clear that hole trapping close to the Si-SiO_2 interface creates surface traps, although the mechanisms is not known.

In this model the trap formation rate would be proportional to the tunneling probability, that is,

$$R_2 = \frac{\partial N_{st}}{\partial t} \sim \exp(-2\chi x_t) = \exp(-E_0/E), \tag{10}$$

where χ is the imaginary wave vector for electrons in the oxide and x_t is the tunneling distance. In the actual part of the oxide forbidden band, χ is relatively independent of energy and equal to about[21] 4.95×10^9 m^{-1}.

According to Eq. (10), we have plotted $\log R_2'$ versus $1/E$ with data taken at two temperatures in Fig. 12. From the slope of the line in Fig. 12 we obtain $E_0 = 2\times10^{10}$ V/m.

From the observed field dependence of the trap formation rate we may thus estimate the trap depth. In Fig. 11 we find $X_t = (\phi_t - \phi_1)/E$, or from Eq. (10) $E_0 = 2\chi(\phi_t - \phi_1)$, which together with our experimental value of E_0 gives $\phi_t - \phi_1 = 2.0$ eV. Using $\phi_1 = 4.2$ eV, the trap depth ϕ_t is estimated to be about 6.2 eV below the oxide conduction band.

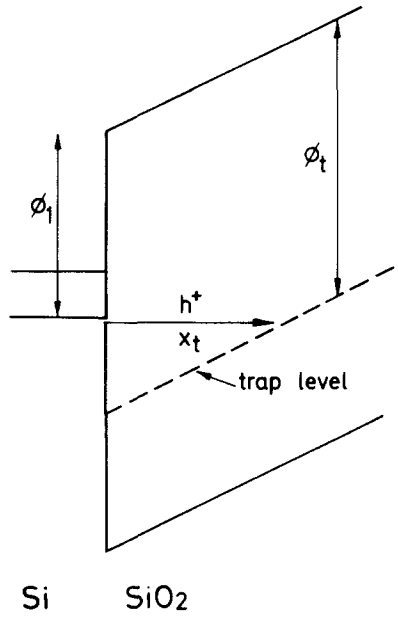


FIG. 11. Estimation of the observed hole trap level ϕ_t during NBS at high fields (t region). ϕ_1 is the Si-SiO_2 barrier height. X_t is the tunneling distance.

We thus suggest that holes are injected and trapped in the oxide and that these holes then create surface traps. How the holes create the traps in our case or in the irradiation case is not known.

The lowest field at which this effect is observed (600 MV/m) is considerably higher than the fields used in the earlier studies.[4,5] This effect has therefore not been observed by these workers. However, Nakagiri[22] has reported a rapid increase of the surface-trap density after shortly-applied fields above 700 MV/m. This increase shows a field dependence as strong as ours and

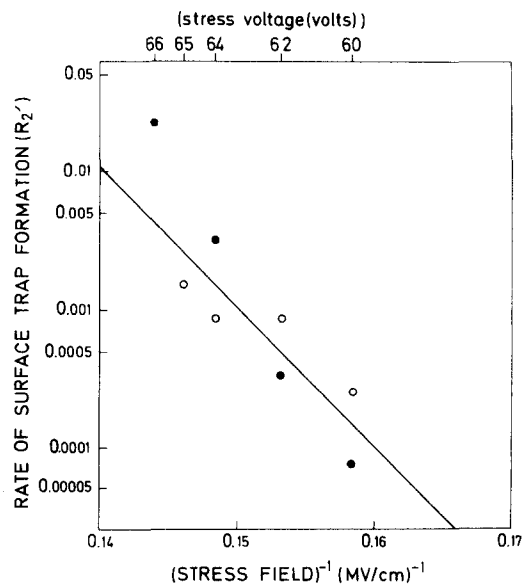


FIG. 12. The relative rate of surface-trap formation R_2' (linear region) is plotted against the inverse of the NBS field for two different NBS temperatures (25 and 60 °C).

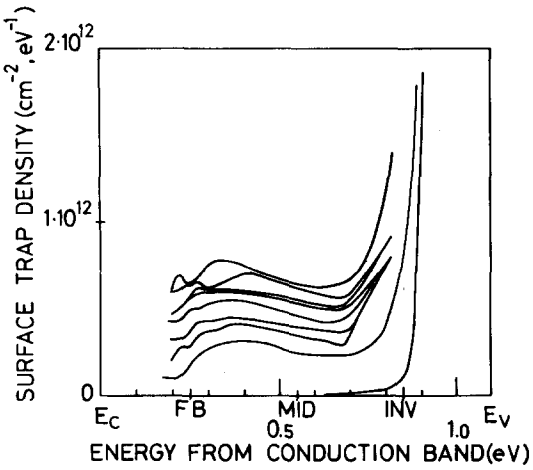


FIG. 13. A full evaluation of the increase of the surface-trap density after NBS at 125 °C, −55 V (5.8 MV/cm). These NBS conditions correspond to the $t^{1/4}$ region (stress time: 0, 3, 7, 12, 20, 35, 50, 80, and 120 min.)

was also independent of temperature from 77 to 473 K. Nakagiri observed this effect in both polarities, but somewhat higher fields were needed with positive bias. The observations of Nakagiri thus support our results.

IX. ENERGY DISTRIBUTION OF SURFACE-TRAP DENSITIES

To shorten time-consuming data evaluation, only the midband surface-trap density has been studied so far. However, much more information may be obtained if the energy distribution of the surface-trap density is calculated. These calculations are particularly pertinent since we have observed two different types of surface-trap formation with different time dependences. Also, Goetzberger *et al.*[5] observed that two independent peaks of surface-trap density emerged at different rates for different stress voltages.

The energy distribution of the surface-trap density is shown for two different NBS conditions in Figs. 13 and 14. In Fig. 13 the sample was stressed with − 55 V at 125 °C, i.e., well inside the region with the $t^{1/4}$-related rate. The number of surface traps are evenly distributed across the energy range, except for a moderate peak just below flatband. Also during stress, the number of surface traps increased evenly at all energy levels.

In Fig. 14 the sample was stressed at RT with − 64 V, i.e., the growth is linear with time. In this case uneven surface-trap distribution and growth was observed. The moderate flatband peak is still detected but it is masked by a fast-growing shoulder that "spreads" towards flatband from lower energies. It was not possible to determine whether the flatband peak possibly increased as $t^{1/4}$ because the fast-growing shoulder influenced the growth too much, even at flatband.

X. MNOS DEGRADATION

As stated in Sec. I, MNOS structures degrade upon high-field stress. This is of considerable importance since an MNOS memory device is normally operated at very high fields during the write and erase cycles. The most important form of degradation is a large threshold-voltage shift caused by an increase of the surface-trap density. In order to investigate the degradation of MNOS structures we studied the rate of surface-trap formation in samples operated repeatedly at high alternating write/erase fields. This degradation was then compared with the NBS effect of MOS devices.

There are two differences between MOS and MNOS structures that are of importance when comparing them at high-field stress. First, changes in the "fixed charge" due to stress may not be observed in MNOS devices. This is because the flatband voltage is variable, the effect that makes the MNOS device useful as a memory. The flatband voltage is determined by the charge in the insulator and by the surface-charge density. The "fixed charge" cannot be separated from the "information charge" that is injected to the memory by the erase and write pulses. However, changes in the surface-trap density may be observed as before.

Second, the stored charge affects the electric field in the insulator, particularly in the oxide at the silicon surface. This field is determined by the gate voltage and the stored charge.[23] Therefore, we are not interested in studying dc stress of MNOS structures, since the gate voltage injects charges into the insulator which considerably reduces the field at the silicon surface to an undetermined value. Instead we stress the MNOS device with an alternating write/erase square wave. Also, in this case the electric field is rather complicated,[1] but with a proper pulse length the average field is approximately determined by the gate voltage.

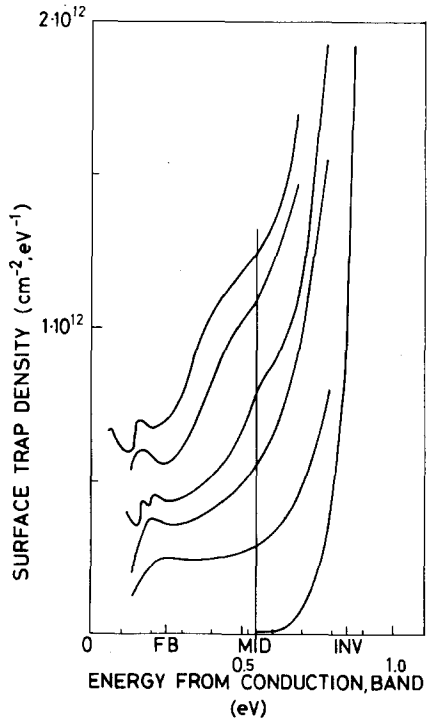


FIG. 14. A full evaluation of the increase of the surface-trap density after NBS at 25 °C, −64 V (6.7 MV/cm). NBS conditions correspond to the t region (stress time: 0, 5, 10, 15, 25, and 35 min.)

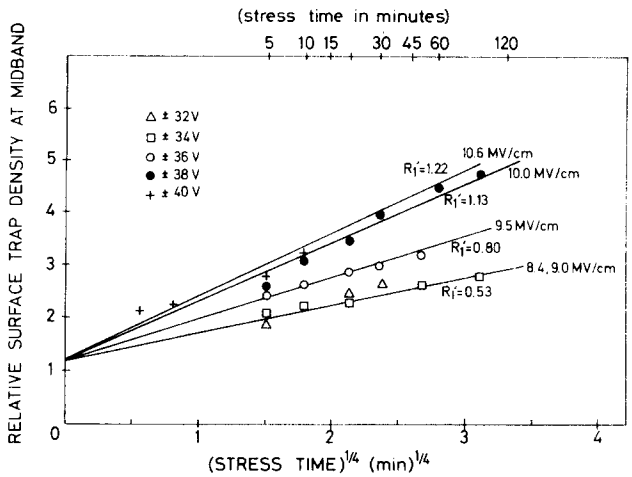


FIG. 15. Relative surface-trap density at midband plotted against (stress time)$^{1/4}$ for different write/erase pulse amplitudes at room temperature for MNOS sample CM-54.

These facts complicate the degradation measurements on MNOS samples. We see that even different write characteristics between samples will give them different degradation properties since the average oxide field will be different.

Let us discuss the measurement on one particular MNOS sample (CM-54). This sample is very similar to one of the samples (CM-55) in Ref. 6. The oxide thickness is 22 Å and the nitride thickness is 640 Å. Typical write/erase cycles are ± 32 V, 10 ms, giving a threshold window of 8 V ($V_T = \pm 4$ V). Degradation was investigated by stressing the device with a square wave with an amplitude of ± 32 to ± 40 V and a period of 20 ms corresponding to repeated 10-ms write/erase pulses. The temperature region 25—125 °C was investigated. Before recording of the C-V curves, a small voltage pulse moved the flatband voltage to 0 V in order to minimize the effect of nitride currents on the quasi-static C-V measurement. As before, changes in the relative surface-trap density at midband were studied.

The observed time dependence of the surface-trap formation exhibits a $t^{1/4}$ time dependence but not a linear dependence, as shown in Fig. 15. This indicates the same mechanism that causes the $t^{1/4}$ behavior of the MOS devices, and a further comparison may be of interest. From Fig. 15 we get a rate constant $R_1' = 1.13$ at a stress voltage of 38 V. This corresponds to an oxide field of about 1000 MV/m [taking $E_{ox} \approx (\epsilon_N/\epsilon_{ox}) \times (V_s/t_N)$]. To compare this result with the MOS results we extrapolate the curves in Fig. 9 to 1000 MV/m and obtain $R_1' \approx 3$ for the MOS device. These two values are of the same order of magnitude ($R_1 \approx 6.5 \times 10^{15}$ $m^{-2}\,eV^{-1}\,min^{-1/4}$).

By plotting $\log R_1'$ against the stress voltage we may determine the constant a in Eq. (6). Using the data in Fig. 15 we get $a = 2.7$ Å, which again is about equal the value found in MOS structures.

We thus conclude that the surface trap formation in MNOS structures is caused by the same reaction that causes the observed $t^{1/4}$ part of the NBS effect in MOS structures. We therefore expect the diffusion-controlled model proposed above to be valid also for MNOS degradation. (The model must of course be modified since part of the diffusion takes place in the silicon nitride.)

One important conclusion is then that we may use known experimental data from NBS measurements on MOS devices in order to find methods of minimizing the degradation effects in MNOS devices.

We mentioned above that measurements were performed at different temperatures. However, we were not able to evaluate the temperature dependence of R_1 because of lack of reproducibility of these measurements.

With an oxide field of 1000 MV/m one might expect the degradation of MNOS devices at room temperature to have a linear time dependence. The fact that we do not observe a linear time dependence is, however, in agreement with the proposed tunneling model. In a MNOS device the oxide is very thin and tunneling of holes from silicon into traps located in the oxide requires a certain oxide thickness as shown in Fig. 11. Tunneling to traps located in the nitride are not supposed to create surface traps. For an oxide field of 1000 MV/m, a trap depth of 6 eV would yield a tunneling distance of 20 Å which is about equal to our oxide thickness. Therefore most holes will tunnel to nitride traps and hence not create any surface traps. However, in MNOS structures with oxide thickness much larger than 20 Å we would expect the tunneling effect to be important, and such devices are thus expected to degrade faster than devices with thinner oxide layers.

It may be of interest to estimate the number of allowed write/erase cycles on our MNOS devices for comparison with other results.[1-3] Assume that we allow the increase of the surface-trap density to cause a 1-V threshold-voltage shift. This corresponds to an increase of the surface-trap density of about $\Delta N_{st} = 1.7 \times 10^{12}$ $cm^{-2}\,eV^{-1}$ or $\Delta N_r = 3$. At a 32-V stress voltage we get $\Delta N_r = 3$ after 55 000 sec (Fig. 15) which corresponds to 3×10^6 write/erase cycles. It should also be noted that we expect this number of pulses to be lower at higher temperatures.

XI. CONCLUSIONS

The process of surface-trap formation at the Si-SiO_2 interface during negative-bias stress has been studied. This is one of the most important degradation processes in MNOS memory devices during repeated write/erase cycling. This process has been characterized through studies of the surface-trap formation rate at different stress fields and temperatures. However, because of the difficulties in accurately determining the oxide field in MNOS devices we have chosen to evaluate this process through negative-bias-stress measurements on MOS devices.

Two mechanisms were observed to create new surface traps during NBS. The first mechanism appears at moderate fields and is believed to be diffusion controlled. The time dependence of such a process was shown to agree with experiments. The other mechanism is dominant at high fields (> 6.3 MV/cm) where the

formation of surface traps was shown to increase very rapidly with the applied field independent of stress temperature. This second mechanism is believed to be controlled by tunneling injection and trapping of holes but requires further clarification regarding the atomic model.

Finally, the NBS behavior of MOS capacitors was compared with the degradation behavior of MNOS capacitors and it was shown that the MNOS devices followed the diffusion-controlled mechanism discussed above.

APPENDIX

Consider a surface at $z=0$, at which a chemical reaction takes place. This reaction is schematically shown in Eq. (3). When the surface defect is electrically activated, a diffusing species leaves the defect site at which a surface trap and a surface charge are left in fixed positions close to each other.

The rate of surface-trap formation may then be written

$$\frac{\partial N_{st}}{\partial t}=A(N_D-N_{st})-BN_{st}C_{Xi}, \tag{A1}$$

where N_D is the initial concentration of surface defects, C_{Xi} is the concentration of the species X at the interface, and A and B are field-dependent rate constants. If this process is diffusion limited rather than reaction-rate limited, the surface reaction will be in quasiequilibrium, giving

$$C_{Xi}N_{st}\approx(A/B)N_D. \tag{A2}$$

Here N_D may be considered constant if we assume that the reaction is always far from saturation ($N_{st}\ll N_D$).

Diffusion control means that the rate of N_{st} growth is controlled by the diffusion of X away from the surface

$$\frac{\partial N_{st}}{\partial t}=\Psi_X; \tag{A3}$$

Ψ_X is the flow by diffusion of the species X from the interface into the oxide

$$\Psi_X=-D\frac{\partial C_X}{\partial z}, \tag{A4}$$

where D is the diffusion constant of X and $\partial C_X/\partial z$ is the concentration gradient of X in the oxide at a distance z from the interface.

The diffusion rate is given by the diffusion equation

$$\frac{\partial C_X}{\partial t}=D\frac{\partial^2 C_X}{\partial z^2}, \tag{A5}$$

where $C_X(z,t)$ is the concentration of X [$C_{Xi}=C(0,t)$]. This equation may be solved by Laplace transforms, giving the Laplace transform of the concentration of X,

$$\tilde{C}_X(z,s)=\tilde{C}_1\exp[-(s/D)^{1/2}z]+\tilde{C}_2\exp[(s/D)^{1/2}z], \tag{A6}$$

with $C_X(z,t)=0$ for $t<0$. Assuming $C_X(\infty,t)=0$, we get $C_2=0$ and $\tilde{C}_1=\tilde{C}_X(0,s)=\tilde{C}_{Xi}(s)$. Note that this assumption is valid only if the oxide may be considered infinitely thick, i.e., if $W^2/4Dt>1$ where W is the oxide thickness.

The Laplace transform of the flow of X from the surface is obtained from Eqs. (A4) and (A6) as

$$\tilde{\Psi}_X=(Ds)^{1/2}\tilde{C}_X. \tag{A7}$$

One solution to this system of equations is

$$N_{st}=R_1t^{1/4}. \tag{A8}$$

To see that this is true, we use the Laplace transform of N_{st}, which is[24] $R_1\Gamma(5/4)s^{-5/4}$, together with Eqs. (A3) and (A7) and get

$$\tilde{C}_{Xi}=R_1\Gamma(5/4)D^{-1/2}s^{-3/4}. \tag{A9}$$

The inverse Laplace transform of this gives

$$C_{Xi}=\frac{R_1\Gamma(5/4)}{(D)^{1/2}\Gamma(3/4)}t^{-1/4}. \tag{A10}$$

By finally inserting C_{Xi} from Eq. (A10) and N_{st} from Eq. (A8) into Eq. (A2) we find that the above solution in Eq. (A8) is true with

$$R_1=\left(\frac{AN_D(D)^{1/2}}{B}\right)^{1/2}\left(\frac{\Gamma(3/4)}{\Gamma(5/4)}\right)^{1/2}\approx 1.16\left(\frac{AN_D(D)^{1/2}}{B}\right)^{1/2}. \tag{A11}$$

A/B is the equilibrium constant for the process (3) and can be written

$$\frac{A}{B}=\left(\frac{A}{B}\right)_0\exp\left(-\frac{\Delta H}{kT}\right), \tag{A12}$$

where ΔH is the enthalpy of process (3). Assuming that the surface charge is located in the oxide at a distance a from the silicon surface, we will expect the enthalpy of the process to decrease with qaE_{ox} in an electric field E_{ox}. The quantity qaE_{ox} is the energy gained by an electron moving from the oxide charge position into silicon. ΔH may thus be written

$$\Delta H=q(\phi_{AB}-aE_{ox}), \tag{A13}$$

where $q\phi_{AB}$ is the zero-field value of ΔH.

The diffusion coefficient D is expected to have the following form:

$$D=D_0\exp(-q\phi_D/kT), \tag{A14}$$

where $q\phi_D$ is the activation energy for D. The rate constant R_1 now becomes

$$R_1=1.16[(A/B)_0N_D]^{1/2}\,D_0^{1/4}\times\exp\{-(q/kT)[(\tfrac{1}{2}\phi_{AB}+\tfrac{1}{4}\phi_D)-\tfrac{1}{2}aE_{ox}]\}. \tag{A15}$$

This equation predicts the field and temperature dependence of R_1 and agrees with Eq. (6) with

$$\phi_0=\tfrac{1}{2}\phi_{AB}+\tfrac{1}{4}\phi_D. \tag{A16}$$

Earlier we determined $a=3.2$ Å and $\phi_0=0.3$ eV. ϕ_D is expected to be about 0.3 eV [19] so $\phi_0=0.3$ eV is not unreasonable, making $\phi_{AB}>0$ in Eq. (A16).

If the production of X at the surface is stopped (by making $A=0$) after a certain time t_d the species X diffuses back to the surface and recombines with the defect site. This process is called annealing. If this annealing takes place at the same temperature as the

degradation, we may calculate its time dependence as a continuation of the above calculation [Eq. (A8)].

Thus, for $0 < t < t_d$, C_{Xi} is given by Eq. (A9), and, for $t > t_d$, $C_{Xi} \approx 0$ according to Eq. (A2) with $A = 0$. $\tilde{C}_{Xi}$ may therefore be written[24] as

$$\tilde{C}_{Xi} = R_1 \Gamma(5/4) D^{-1/2} s^{-3/4} [1 - \exp(-st_d)]. \quad \text{(A17)}$$

As above, we find, by using Eqs. (A3) and (A7), that

$$N_{st} = R_1 [t^{1/4} - (t - t_d)^{1/4}], \quad t > t_d. \quad \text{(A18)}$$

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