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Negative Capacitance Field Effect Transistors; Capacitance Matching and non-Hysteretic Operation

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***Abstract*—This work experimentally demonstrates negative capacitance MOSFETs in hysteretic and non-hysteretic modes of operation. A PZT capacitor is externally connected to the gate of commercial nMOSFETs fabricated in 28nm CMOS technology to explore the negative capacitance effect. In hysteretic devices, subthreshold slope as steep as 10mV/dec is achieved in the region where the ferroelectric represents an S-shape polarization. In addition, a matching condition is achieved between a PZT capacitor and the gate capacitance of MOSFETs fabricated on SOI substrates. For the first time, we achieve a non-hysteretic switch configuration in our fabricated MOSFETs, suitable for analog and digital applications, for which a reduction in the subthreshold swing is obtained down to 20mV/dec.**

I. Introduction

As CMOS technology continuing its relentless downscaling, power dissipation has become the most important roadblock for future nanoelectronic circuits and systems [1]. It is well known that the power dissipation would be lowered significantly if FETs could be operated at lower voltages [2]. An average subthreshold swing (SS) smaller than the thermal limit of MOSFET swing at room temperature would enable the scaling of the supply voltage, V_{dd}. A sub-thermal subthreshold swing ($< \ln(10)KT/q$, which is $60mV/dec$ at $T = 300K$) can be obtained by decreasing the device body factor, $m = 1+C_s/C_{ins}$, to a value smaller than 1 (where C_s and C_{ins} are the semiconductor and the gate oxide capacitances) [3], [4]. This can be achieved by using the recently proposed negative capacitance (NC) effect of ferroelectric materials to the gate stack of conventional MOSFETs [5], [6]. It has been suggested that a Metal-Ferroelectric-Semiconductor (MFS) can provide a feasible solution to step-up the semiconductor surface potential (ψ_s) above the gate voltage (V_g) which leads to a reduction in the subthreshold swing [7], [8]. The underlying idea consists of exploiting the negative capacitance region of ferroelectric materials, defined as $C_{FE} = dQ/dV_{FE}$, where Q and V_{FE} refer to the charge density and the voltage drop over the ferroelectric, respectively [9], [10]. A ferroelectric capacitor (FE) in series with a dielectric capacitor (DE) of a proper value can be biased in the negative capacitance region, providing a larger capacitance than the constituent DE capacitor [11]. In order to have a non-hysteretic NCFET, the ferroelectric NC and DE capacitor should be well matched to provide a positive total capacitance in the whole range of the operation [12], [13] while the slope of the charge line is smaller than the negative slope of the FE polarization [14], [15].

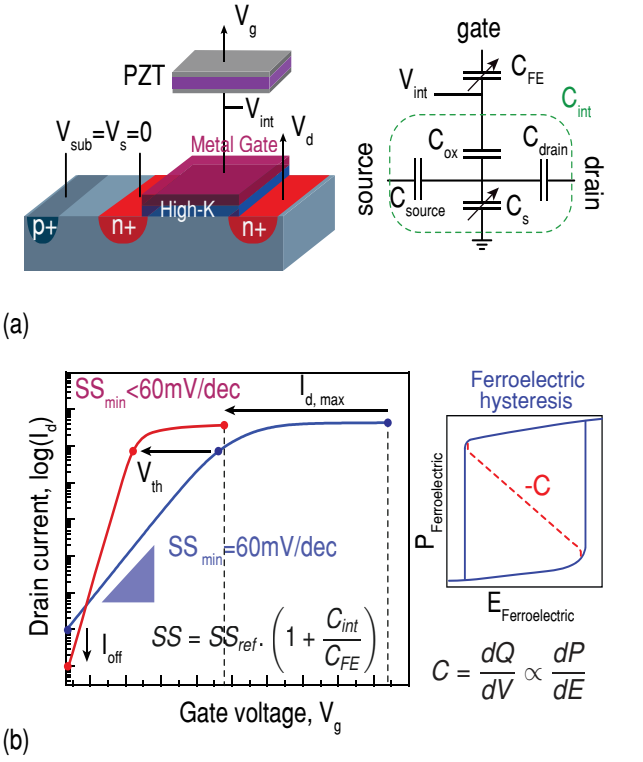

Fig. 1. The investigated experimental configuration of the NCFET (left) and the capacitance model of the structure (right). C_{int} is the total capacitance of the reference MOSFET looking into the gate (a). Transfer characteristics of a non-hysteretic NCFET versus the base MOSFET highlighting the gain of using the ferroelectric negative capacitance in terms of SS improvement and threshold voltage reduction (b).

In this context, we experimentally investigate the impact of the ferroelectric NC on DC electrical behavior of commercial MOSFETs fabricated in $28nm$ CMOS technology. A matching condition is proposed between the ferroelectric and MOS capacitances in order to obtain the non-hysteretic operation of the device. The subthreshold swing below the theoretical limit at room temperature ($60mV/dec$) over many decades of current on hysteretic NCFETs is achieved in $28nm$ bulk CMOS process. Moreover, the non-hysteretic operation of an NCFET with a matched PZT capacitor and sub-thermal swing is demonstrated.

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II. Hysteretic and Non-Hysteretic Operation: Capacitance Matching

One may consider the NCFET as a conventional transistor with an added amplifier. Considering a simple capacitance model (Fig. 1-a), the amplification factor of the NC effect can be expressed as

$$\beta = \partial V_{int}/\partial V_g = C_{FE}/(C_{FE} + C_{int}). \quad (1)$$

It should be noted that the following conditions are required to provide a sufficient amplification together with a non-hysteretic behavior in an NCFET: (i) the absolute value of the ferroelectric negative capacitance ($|C_{FE}|$) and the intrinsic gate capacitance (C_{int}) need to be relatively close, and (ii) the total capacitance should remain positive in the whole range of operation; $C_{total}^{-1} = C_{FE}^{-1} + C_{int}^{-1} > 0$. Using the amplification factor, β, the subthreshold swing of an NCFET, SS_{nc}, can be indicated as:

$$SS_{nc} = \left(\frac{\partial Log I_d}{\partial V_g}\right)^{-1} = \frac{\partial V_{int}}{\partial Log I_d} \times \frac{\partial V_g}{\partial V_{int}} = \frac{SS_{ref}}{\beta}. \quad (2)$$

In the subthreshold region, providing an effective NC by the ferroelectric leads to $\beta > 1$ and the SS will be reduced [5]. The hysteretic NCFETs and also a non-hysteretic device which fulfills above conditions will be discussed in the following sections.

III. Hysteretic NCFET

The experimental configuration of the NCFET including the capacitance model of the device is schematically depicted in Fig. 1-a, where a PZT capacitor is externally connected to the gate of a conventional MOSFET. Such external electrical connection offers the flexibility of testing tens to hundreds of PZT capacitor values and MOSFETs until the best matching is obtained. The impact of the ferroelectric negative capacitance on DC electrical performance of MOSFETs is schematically illustrated in Fig. 1-b.

High-performance commercial *n*-type MOSFETs fabricated in $28nm$ CMOS technology have been employed as the reference devices and Pb(Zr_{46},Ti_{57})O_3 (PZT) is exploited as the ferroelectric material. The PZT ferroelectric with a thickness of $50nm$ has been grown via the chemical solution deposition root on a *Pt*-coated silicon wafer [16], [17]. *Pt* top electrode is deposited at room temperature and patterned by shadow masking. The deposited PZT film has a polycrystalline structure. High-quality epitaxial ferroelectric layers are commonly considered suitable for NC devices due to their ability to form a mono-domain state characterized by a simple coercive field [18]. In this study, a repetitive bipolar voltage is applied to the ferroelectric capacitors, so that the mono-domain behavior is achieved in the polycrystalline ferroelectric material. The characterized electrical parameters of the thin film PZT (i.e. relative permittivity, coercive field, and remanent polarization) are depicted in Fig. 2. Red curve illustrates the relative permittivity (epsilon) with respect to the imposed

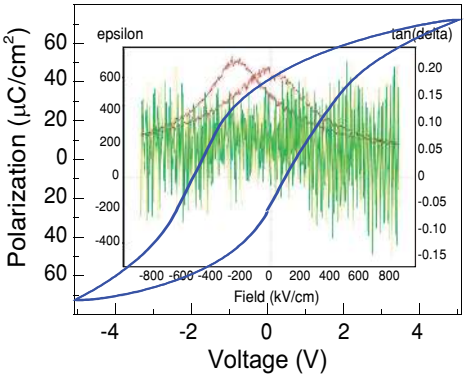

Fig. 2. The film polarization, permittivity, and the phase angle of the capacitance measurement hysteresis loops regarding the applied voltage (electric field) on the ferroelectric layer. The relative permittivity, coercive field, and remanent polarization of $220 - 240$, $260kV/cm$, and $30.2\mu C/cm^2$ have been measured.

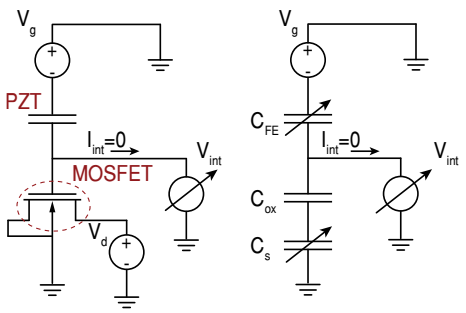

Fig. 3. Measurement setup utilized for probing the internal voltage, V_{int}, using an Agilent 4156C semiconductor analyzer. This probing has a negligible influence of the extracted SS.

electric field which varies from 220 to 240. The coercive field ($\pm 260kV/cm$) and remanent polarization ($\pm 30.2\mu C/cm^2$) of the PZT are extracted from the blue curve, devoted to the polarization-voltage hysteresis.

The experimental setup used for the electrical characterization of NCFETs is represented in Fig. 3. The internal contact is probed (V_{int}) while a voltage is applied to the top gate (a zero current is injected in the internal node). As reported in [6], this probing has a negligible impact on the measurement results of the SS.

Fig. 4 shows experimental characteristics data measured on an nMOSFET with $W = 100nm$, $L = 1\mu m$ (NCFET-a), and a $20\mu m \times 20\mu m$ PZT capacitor connected to the gate with a drain voltage of $100mV$. Fig. 4-a illustrates the hysteretic transfer characteristic of NCFET-a with an improved I_{on}/I_{off} ratio. A sub-thermal swing over 4 decades of current is illustrated in Fig. 4-b. The voltage amplification in the regions corresponding to the device subthreshold slope is depicted in Fig. 4-c. Imposing displacement vector continuity, a unique S-shape behavior in the polarization, P, is obtained and illustrated in Fig. 4-d. A negative slope of the polarization with respect

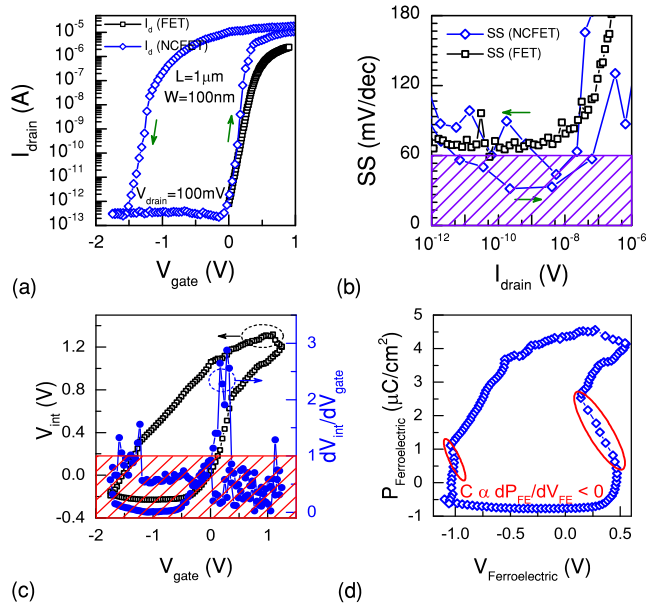

Fig. 4. Transfer characteristic of NCFET-a, where a $20\mu m \times 20\mu m$ PZT capacitor with a thickness of $50nm$ is connected to the gate of a commercial nMOSFET (a). Sub-thermal swing (b) is obtained over many decades of current due to the differential voltage amplification of NC. Amplification factor greater than 1 is achieved (c) in the regions corresponding to the negative slope of the ferroelectric polarization (d).

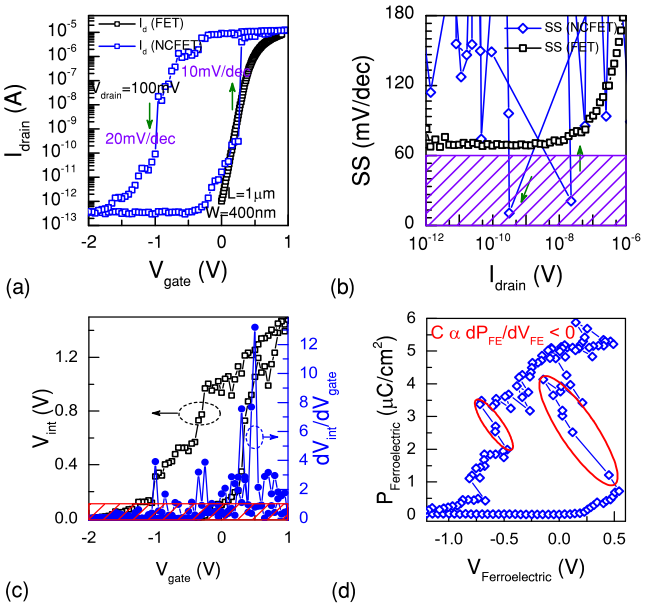

Fig. 5. The impact of the NC on DC electrical behavior of NCFET-b (b). Subthreshold slope as steep as $10mV/dec$ is demonstrated with a better matching of capacitances (b). The internal voltage represents β greater than 1 up to 12 (c). The polarization of the ferroelectric confirms the existence of NC in both positive and negative going branches (d).

to the applied electric field is observed in a certain range of the polarization, corresponding to the subthreshold region of the device.

The device operation is hysteretic due to the relatively small value of C_{int} where $C_{total}^{-1} = C_{FE}^{-1} + C_{int}^{-1} > 0$ is not fulfilled in the whole range of the gate voltage. Device characterizations of an architecture (NCFET-b) with a better matching of capacitances (higher C_{int} due to the larger gate) is illustrated in Fig. 5. Subthreshold swing of $10mV/dec$ with a $1V$ hysteresis is obtained (Fig. 5-b). The representation of the voltage amplification of this architecture is shown in Fig. 5-c with $\beta > 1$ in both branches (having a peak of above 12). The extracted P-V hysteresis of the ferroelectric capacitor clearly demonstrates the negative slope of the polarization, confirming the NC effect.

IV. Non-Hysteretic NCFET

Due to the relatively small intrinsic gate capacitance of commercial MOSFETs, the full capacitance matching between PZT capacitors and MOS capacitors is challenging.

Here, we fabricated MOSFETs on a SOI silicon wafer in relatively large dimensions which fulfill the condition for non-hysteretic NCFET. The devices are built on a p-type SOI substrate with $88nm$ of epitaxial silicon and $145nm$ BOX. A cycle of dry oxidation plus HF-based etching is used to thin down the Si layer to $30nm$, improving the gate electrostatic control. After the source and drain phosphorus implantation and annealing, the FET body is shaped using photolithography and selective plasma etching. HfO_2 with $3nm$ thickness has been deposited by ALD on an ultra thin

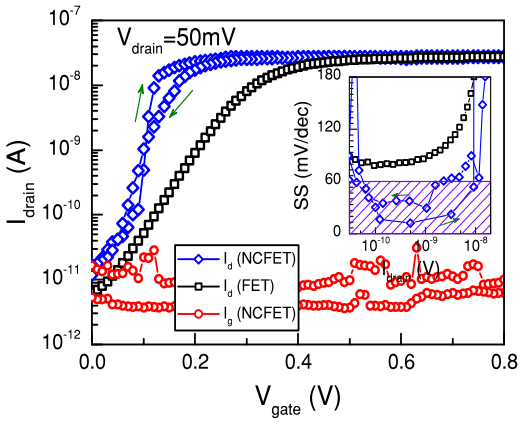

Fig. 6. $I_d - V_g$ characteristic of a non-hysteretic NCFET using a $10\mu m \times 10\mu m$ PZT capacitor comparing the reference MOSFET ($W = 19\mu m, L = 2\mu m$) with $V_{drain} = 50mV$. Sub-thermal swing down to $20mV/dec$ is obtained due to the differential amplification effect of the ferroelectric NC.

layer of SiO_2 as the gate dielectric. As reported in [19], SiO_2 is used in order to provide a proper interface with the Si channel. Photolithography is used to define the source/drain dielectric openings for electrical contact, which are then created by BHF etching. AlSi1% metal contacts have been created by sputtering and lift-off process.

In order to obtain non-hysteretic negative capacitance, A $10\mu m \times 10\mu m$ PZT capacitor is connected to the gate of a MOSFET, figured out above, with a gate length of $2\mu m$ and a gate width of $19\mu m$. Fig. 6 shows $I_d - V_g$ characteristics of the reference MOSFET and the NCFET at $50mV$ drain

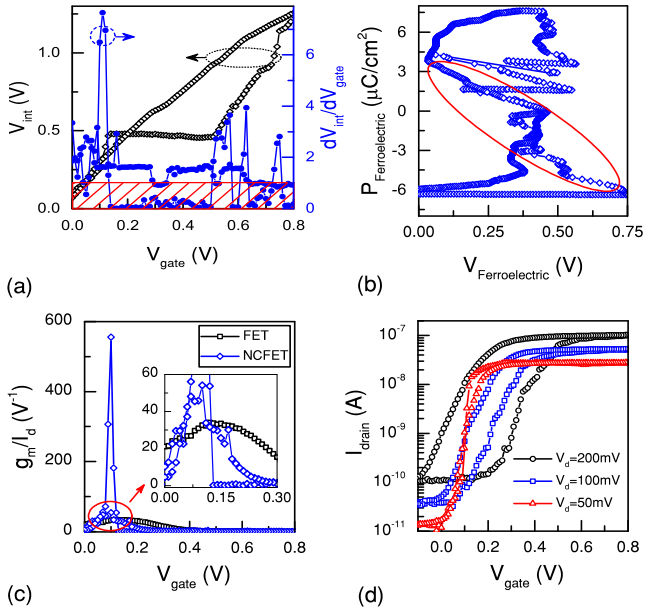

Fig. 7. Electrical characteristics of the proposed non-hysteretic NCFET. The internal voltage measurement depicts an amplification factor greater than 1 in the subthreshold region (a). The polarization of the ferroelectric demonstrates a negative slope in a wide range of the polarization (b). The calculated g_m/I_d of the NCFET represents a significant boosting in the subthreshold region of the device (c). Increasing the drain voltage results in limiting the improvement of the NC effect and increasing of the hysteresis (d).

voltage. The recorded gate leakage confirms that its level is systematically lower than I_{on} and the leakage and charge trapping mechanisms can be neglected in the reported effects. A significant improvement in the SS of the device is obtained when the ferroelectric and gate capacitances are matched so that a non-hysteretic NC operation can be achieved over the whole range of the gate voltage. A sub-thermal swing, down to $20mV/dec$, is observed due to the voltage amplification of the ferroelectric effective NC (the inset figure of Fig. 6). The internal voltage measurement represents the amplification factor up to 7 (Fig. 7-a) in the subthreshold region. Fig. 7-b reports the ferroelectric polarization showing an effective NC in a wide range of the polarization. Fig. 7-c compares g_m/I_d (g_m is the transconductance) of the NCFET with the reference MOSFET, indicating a significant improvement in the subthreshold region. The impact of the drain voltage on the NC effect is exploited in Fig. 7-d. Increasing the drain voltage performs hysteresis in the device operation and reduces the amplification factor.

V. Conclusions

The hysteretic and non-hysteretic behaviors of negative capacitance-MOSFETs are investigated in this paper. It has been experimentally proved that a significant reduction of the subthreshold swing can be obtained by the impact of the NC on field-effect transistors. A $10mV/dec$ subthreshold slope is achieved with $1V$ of hysteresis in a commercial 28nm CMOS technology. A matching condition between the ferroelectric and MOS capacitances is obtained for the non-hysteretic operation in MOSFETs fabricated on SOI substrates leading to a subthreshold swing of $20mV/dec$.

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