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Networks-in-Package; Design, Analysis and Implementation

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ABSTRACT- SiP(System-in-Package) and SoC(System-on-Chip) are familiar to us. In this paper, we firstly define advanced concepts of NoC(Network-on-Chip) and NiP (Network-in-Package). Design and implementation of NoC are explained and then, NiP used for NoC is designed and analyzed regarding of signal integrity and power integrity. The low-power packet-switched NoC with hierarchical star topology is designed and implemented for high-performance SoC platform. An NiP integrating four NoCs is fabricated in a 676-BGA-type package for large and scalable systems and the measured results of the NiP show perfect communications between NoCs.

I. Introduction

Recently, there have been strong demands for high-density packages which include multiple chips and passive components. A System-in-Package (SiP) (or SoP, that is System-on-Package) technology has been proposed as a way to overcome the density limitation of conventional single-chip package [1]. However, there is no significant difference between SiP and simply connected Multi-Chip-Module (MCM) except for their size or stacking. A concept of Networks-in-Package (NiP) is multi-chip module in a single package with packet-switched communications between Intellectual Properties (IPs) of each chip, as depicted in Fig 1. NiP is an advanced concept of SiP.

Large scale System-on-Chips with huge chip size such as embedded memory logic systems often suffer from their low yield and high cost problems. In this work, a hierarchically star-connected Networks-on-Chip (NoC) refers a designed and implemented using layered protocols and packet-switched networks, and integrated in NiP. For large scale NoC implementations, the power consumption on the network infrastructure should be minimized for reliable transmission of data with low-cost [2]. In this context, we firstly mention used chips, NoCs, and their features. Then, signal integrity and power integrity issues in design and implementation of NiP are shown.

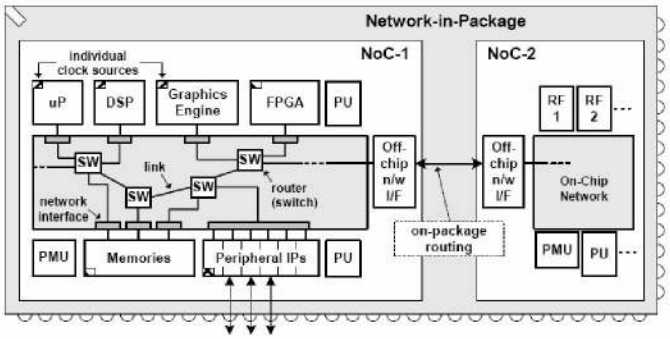


Fig.1. Networks-on-Chip and Networks-in-Package architecture

II. Design and Implementation of Networks-on-Chip

An energy-efficient Networks-on-Chip (NoC) is presented for possible applications of high-performance SoC design. It incorporates heterogeneous Intellectual Properties (IPs) such as multiple RISCs and SRAMs, a reconfigurable logic array, an off-chip gateway, and a 1.6GHz PLL. Its hierarchically-star-connected on-chip

network provides the integrated IPs, which operate at different clock frequencies, with packet-switched serial-communication infrastructure. Various low-power techniques such as small-swing signaling, partially activated crossbar, serial link coding, and clock frequency scaling are devised and applied to achieve the power-efficient on-chip communications. The 5mm×5mm chip containing all above features is fabricated by 0.18μm CMOS process, successfully measured, and demonstrated on a system evaluation board where multimedia applications run. The fabricated chip can provide 11.2GB/s aggregated bandwidth at 1.6GHz signaling frequency. The chip consumes 160mW and the on-chip network dissipates less than 51mW.

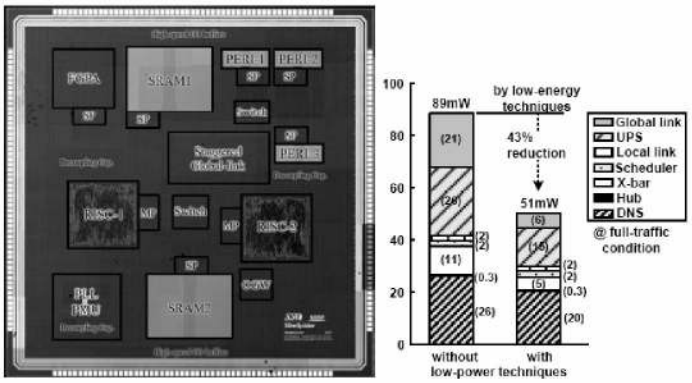
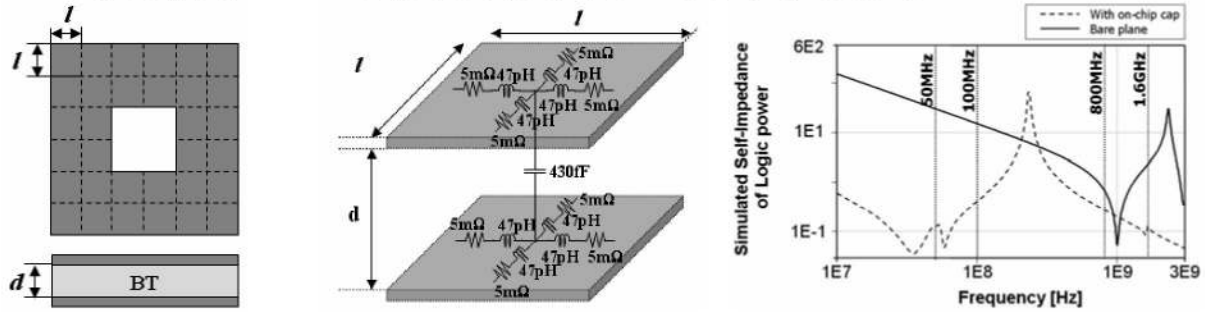


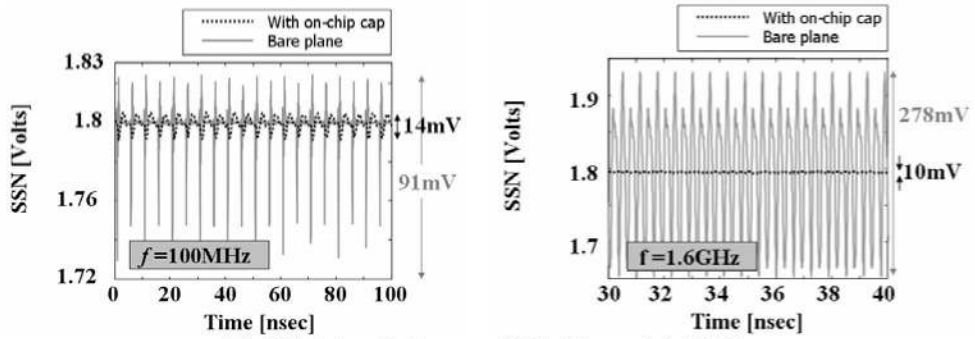
Fig.2. Die photograph and power reduction new techniques

III. Design and Analysis of Networks-in-Package (NiP) with Pre-Simulation

The NiP needs four isolated supply voltages: 1.8V for digital logic, 1.8V for analog circuits, 3.3V for I/O, and sub-0.5V for small-swing links. Each module has different operating frequencies: 50MHz for peripheral logic, 100MHz for processors, 800MHz for scheduler, and 1.6GHz for on-chip networks.



(a) TLM Model of Logic Power (b) Unit Cell of TLM Model (c) Self-Impedance of Logic Power



(d) SSN simulations at 100MHz and 1.6GHz

Fig.3. Logic Power Plane of NiP

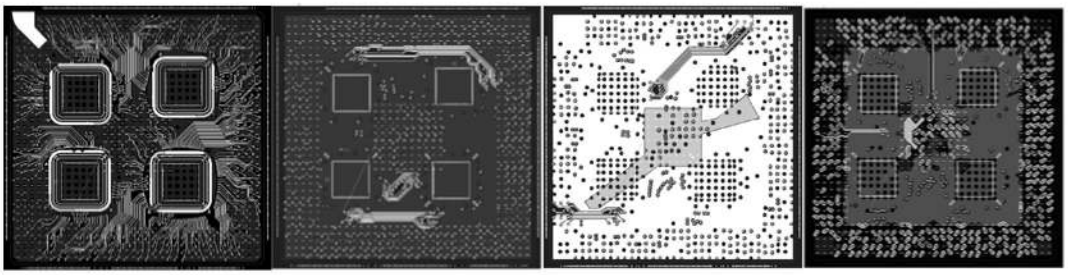
One important issue of the NiP package design is power integrity, *i.e.* a design of power and ground (P/G) distribution network (PDN). There should be no significant resonance of impedance on the P/G plane of the package at the operating frequency of NoC. In order to analyze the power integrity, we used Balanced

Transmission Line Matrix (TLM) method and Simultaneous Switching Noise (SSN) analysis [3]. Shapes of power planes to supply three isolated voltages are simulated using TLM method and determined not to have plane-resonances of self-impedances at operating frequencies of the chip, as shown in Fig. 3 (c). We also designed the number of decoupling-capacitors to be used and the values of those for each power voltage at the proper position [4]. As changing shapes of power planes and the number of off-chip decoupling-capacitors, we analyzed induced SSN between power and ground. After inserting the off-chip decoupling-capacitors and on-chip decoupling capacitors, the impedance resonance occurs at 272.1MHz, and the SSN voltages are dramatically suppressed at target frequencies, as shown in Fig.4. (d). As a result, self-impedances at the target frequencies become less than 1Ω.

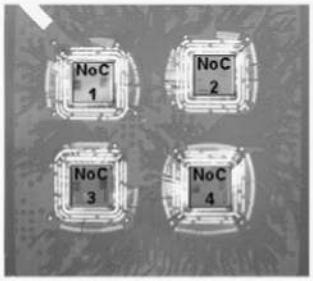
Another issue of the NiP package design is signal integrity, which is reliance on transmission of the high-frequency signals. We designed under some rules considering the signal integrity: separation between the high-frequency signals, *e.g.* 800MHz signals or 1.6GHz signals, the shortest path of high-frequency signals, the maximum number of ground balls for guarantee of return current path, and insertion of ground balls around differential signals to sustain differential mode [5].

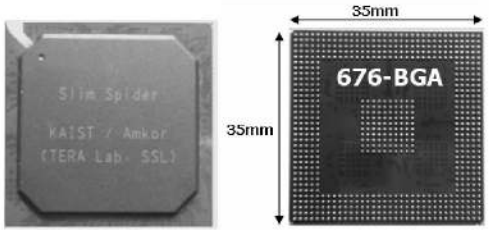
IV. Implementation and Measurement of Networks-in-Package (NiP)

The Networks-in-Package (NiP) system is constructed with four NoCs mounted on a single 676-BGA (Ball Grid Array) package as shown in Fig. 4. The NiP Package has a four-layered PCB, top/ground/power/bottom. The second layer is used as ground (or reference voltage) plane which does not have separation between analog ground and digital ground. Logic power and analog power exist in the third layer, while I/O power does in the forth layer. Photographs of implemented 35mm×35mm NiP package are depicted in Fig.4. (b) and (c).



(a) NiP Package Layout (Top/Ground/Power/Bottom)





(b) Implemented NiP Package (Before molding) (c) Implemented NiP Package (After molding)

Fig.4. NiP Photograph

Total NiP system is implemented for measurement of operation as described in Fig.5. A NiP test board contains mode-selection switches, frequency-selection switches, high-speed signal pads, reference-clock oscillator, power/ground terminals, and external I/O test pins for operating test.

Measured self-impedance curve of I/O power is plotted in Fig.6 (a). It is noted that the impedance curve has no plane-resonances at operating frequencies of the chip as we intended and it became small impedance lower than 10Ω. Fig. 6 (b) shows packet transactions between two NoCs on the NiP where the two NoCs are running at different clock frequencies, e.g. 400MHz and 274MHz. Because the NoC adopts source-synchronous signaling, the NiP enables plesiochronous communications between processing units running at different clock frequencies in different NoCs. First, NoC-1 commands "Write packet" at NoC-2 and NoC-1 again commands "Read packet at same address" at NoC-2. Then, NoC-2 responses to the "Read command" of NoC-1.

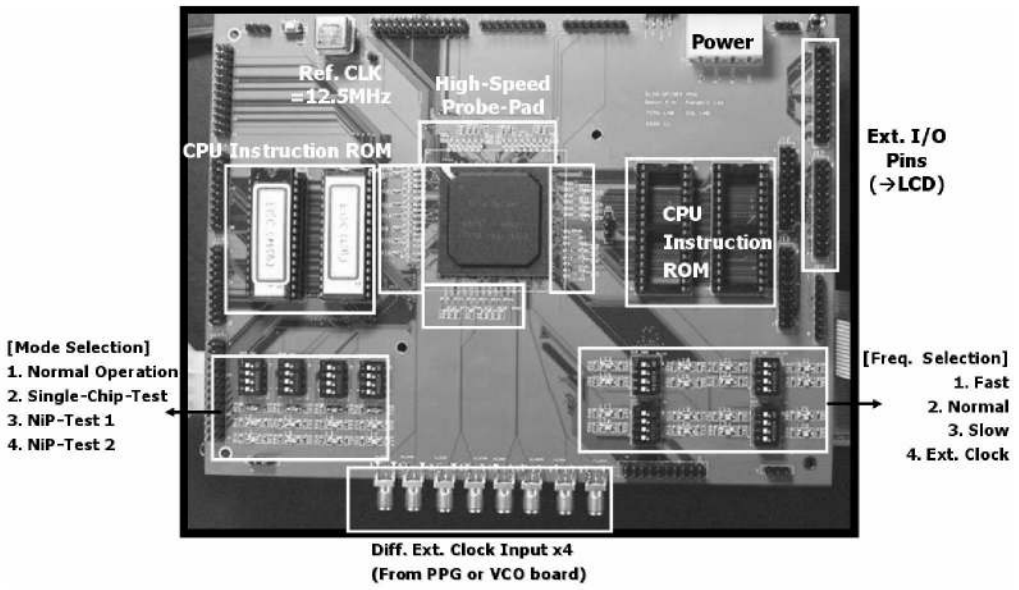
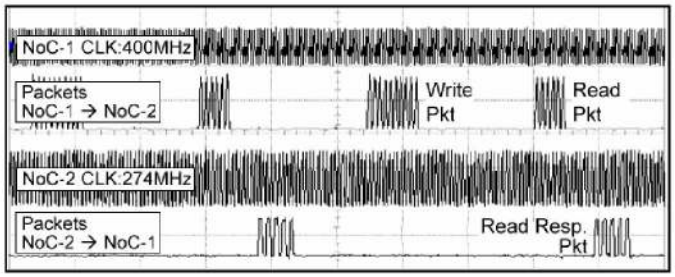


Fig.5. NiP System Implementation



(a) Measured self-Impedance of I/O power (b) Communication signals between NoC-1 and NoC-2

Fig.6. Measurement Results of NiP

V. Conclusion

Low-power packet-switched Networks-on-Package (NoC) and Networks-in-Package (NiP) with hierarchical star topology are designed and implemented for high-performance large and scalable system. The NoC contains several processors for chip operation, off-chip gateway for off-chip network interface, and on-chip networks connecting those processing units. Source-synchronous signaling enables plesiochronous communications between processing units in different NoCs running at different clock frequencies. The Networks-in-Package (NiP) system is constructed with four NoCs mounted on a single 676-BGA (Ball Grid Array) package sized 35mm by 35mm. Considering signal integrity and power integrity, separated powers and significant signals of the NiP are designed and analyzed by TLM method and SSN analysis. The implemented NiP shows perfect operations of each NoC and communications between NoCs.

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