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New advancements in charge-coupled device technology - sub-electron noise and 4096x4096 pixel CCDs

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ABSTRACT

This paper reports on two new advancements in CCD technology. The first area of development has produced a special purpose CCD designed for ultra low-signal level imaging and spectroscopy applications that require sub-electron read noise floors. A nondestructive output circuit operating near its 1/f noise regime is clocked in a special manner to read a single pixel multiple times. Off-chip electronics average the multiple values, reducing the random noise by the square-root of the number of samples taken. Noise floors below 0.5 electrons rms are reported. The second development involves the design and performance of a high resolution imager of 4096x 4096 pixels, the largest CCD manufactured in terms of pixel count. The device utilizes a 7.5-micron pixel fabricated with three-level poly-silicon to achieve high yield.

1. SKIPPER CCD

1.1 Introduction

In the past, buried-channel CCDs often required a bias or "fat-zero" charge to successfully transfer very small charge packets. The fat-zero generated a shot noise component that was usually higher than the noise produced by the sensor's on-chip amplifier. The Texas Instruments 800x800 3-phase CCD, for example, requires a fat-zero of 100 electrons (e-) to fill-in a design induced trap associated with its transfer gate region[1]. Although the on-chip amplifier noise for the TI device is only 6 e- rms, the fat-zero required for complete transfer generates a shot noise of 10 e- increasing the overall noise floor of the detector to 11.6 e-.

CCD manufacturers have recently made notable progress in eliminating design and process induced trapping centers similar to those experienced with the TI CCD[2]. Today, charge transfer efficiency (CTE) performance is usually limited by bulk state traps, small electron traps due to impurities found naturally in the bulk silicon on which the CCD is made. Current CCDs exhibit near perfect CTE as a result of the high quality silicon grown today. For example, a "bulk state limited" CCD can transfer a 10,000 e- charge packet 521 transfers with less than 5 e- deferred without the aid of fat-zero charge[3].

Although charge packets of a few electrons can be transferred, the CCD is unable to read the charge accurately because of the relatively high noise floor inherent to the sensor's on-chip amplifier (typically a few electrons rms). Efforts this year have been directed at the CCD manufacturer to break the 1 e- noise barrier so that the high CTE now achieved can be fully exploited.

Theoretically, the read noise for the scientific CCD can be reduced without limit by the amount of process time spent on each pixel. There are, however, practical limits to this procedure. Employing short sample periods of typically less than 8 micro-seconds, we find that the noise of the CCD decreases by the square root of the sample time. However, for longer sample times, the noise only gradually decreases and, for some CCD camera systems, the noise actually increases due to low frequency noise sources encountered (e.g., 1/f noise generated by the CCD amplifier). Our current knowledge in minimizing CCD amplifier noise indicates that 2 to 3 e- may be the practical limit assuming that conventional output charge detection schemes are utilized (i.e., floating diffusion MOSFET amplifiers).

The CCD Skipper was invented to circumvent the 1/f noise problem and realize a square root reduction in noise with increasing sample time thereby allowing sub-electron noise floors to be achieved. The principal function of Skipper technology is to allow the user to nondestructively measure the charge contained in a pixel multiple times (similar to CID operation) using a "floating gate" amplifier. The samples collected for a given pixel are then averaged together off-chip reducing the random noise of the on-chip amplifier by the square root of the number of samples taken. For example, if a pixel is sampled 100 times, the random noise associated with the on-chip amplifier is diminished by a factor of ten.

1.2 Architecture, Operation and Fabrication

Figure 1 shows a design layout of an experimental Skipper CCD fabricated at Ford Aerospace. The design shows the output region and the floating gate electrode used to detect signal charge in the channel near the end of a three-phase horizontal register. The floating gate is connected to a MOSFET source follower amplifier and to a MOSFET reset switch used to preset the gate to a reference voltage before signal charge is dumped. The Skipper sequence begins by clocking the horizontal register one pixel and transferring charge into gate 1

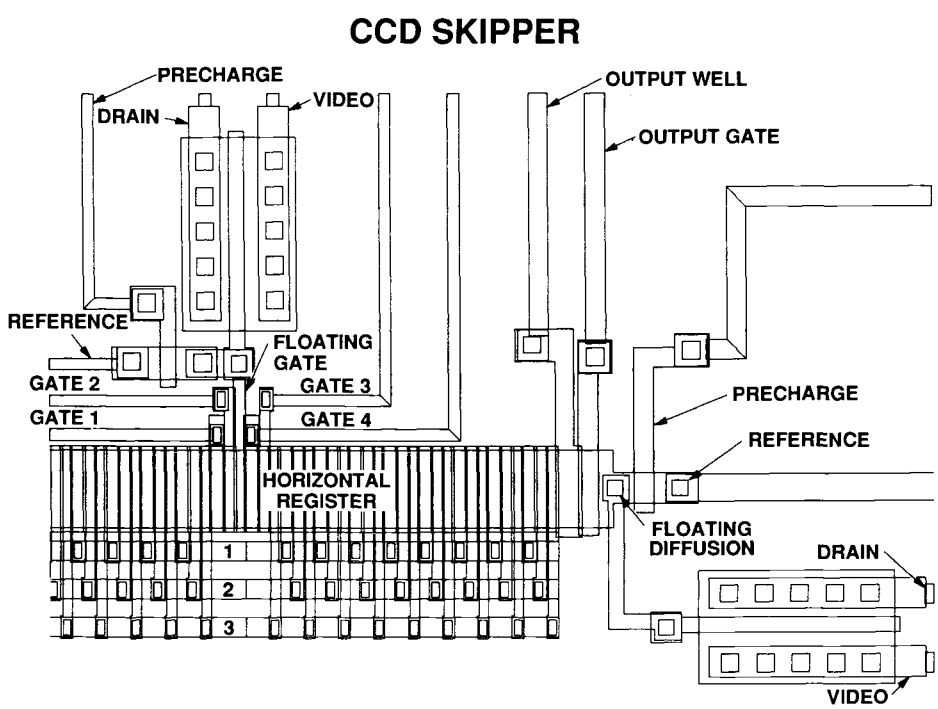

Figure 1. Design layout of an experimental Skipper CCD.

(refer to Figure 2). The horizontal clocks are then inhibited for the duration of the Skipper cycle and, shortly thereafter, the floating gate is preset to Vref. Gate 1 is then clocked low forcing charge to transfer through gate 2 into the potential well under the floating gate. The voltage at the output source of the amplifier changes in proportion to the amount of charge transferred beneath the floating gate. The voltage is then sampled by off-chip electronics resulting in the first sample for the pixel. The charge packet is then quickly moved back to gate 1 by clocking gates 2 and 1 high completing the sequence. The floating gate is reset again and the above cycle is repeated several times depending on the final noise level required.

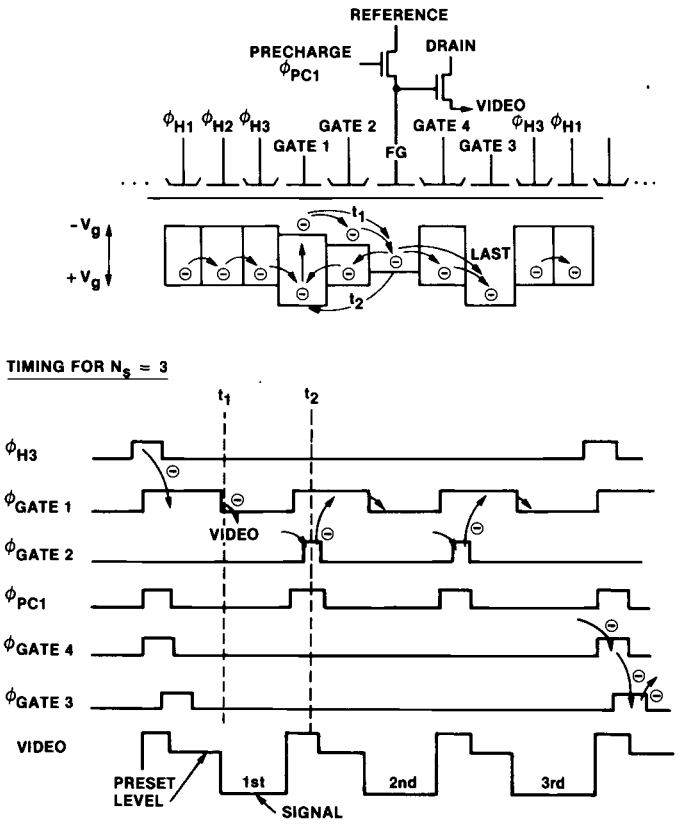

Figure 2. Timing diagram for the Skipper CCD shown in Figure 1.

When all samples for a pixel are collected, gates 3 and 4 are activated forcing charge back into the horizontal register (i.e., phase 3). As the horizontal register is clocked, the charge packet is transferred to a conventional floating diffusion MOSFET amplifier at which point it can either be sampled again (only once for this type of amplifier) or discarded through a second reset MOSFET.

The Skipper CCD is fabricated using processes identical to those used for other Ford CCDs. Fabrication details of Ford CCDs are briefly discussed below for the 4096x4096 pixel CCD.

1.3 Performance

Figure 3 shows processed video line traces generated by an experimental 64Vx256H Skipper CCD in response to a square-wave target. The clocks to the CCD sample 21 extended pixels and the first 89 video pixels sixty-four times each. The remaining 167 pixels are rapidly readout ("skipped") by sampling these pixels only once. Figure 3b magnifies Figure 3a showing the 89th pixel followed by 43 single-sampled pixels. Careful examination of the

89th pixel shows the random read noise associated with the 64 samples. This noise will later be suppressed off-chip by averaging these samples into a single value.

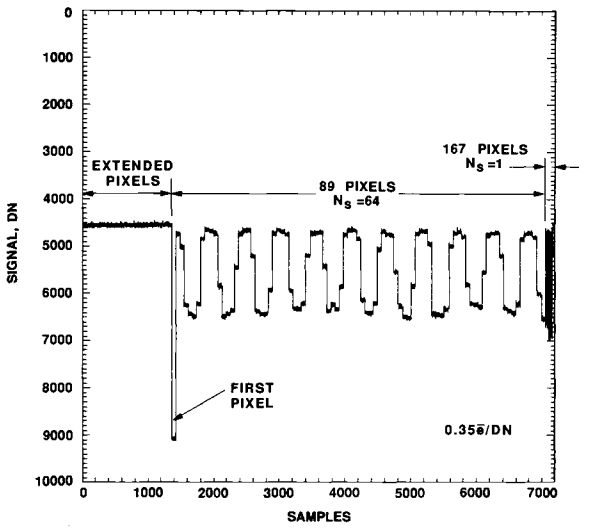

Figure 3a. A processed video line trace of a Skipper CCD in response to a square-wave target.

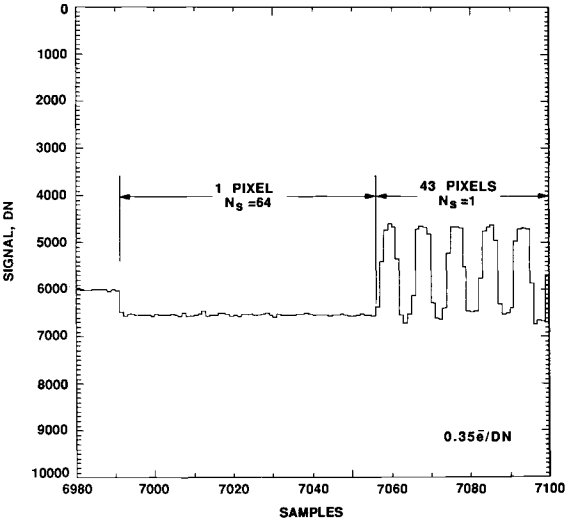

Figure 3b. A magnified view of Figure 3a showing the 89th pixel sampled 64 times. The 43 pixels that follow are only sampled once.

Figure 4 demonstrates sub-electron read noise performance for the same device in response to four low-light level point sources. Each pixel in the top image is displayed using only the first sample of a 64 sample/pixel set. The pixels in the bottom image utilize all 64 samples. Random read noise levels of 7.6 e- and 0.97 e- are measured for the top and bottom images respectively using the photon transfer technique.[1] The smallest point source signal seen in the bottom image is 3-4 e-. The two point images on the right side of the top image are completely hidden in the noise but are clearly seen in the bottom image due to the noise reduction.

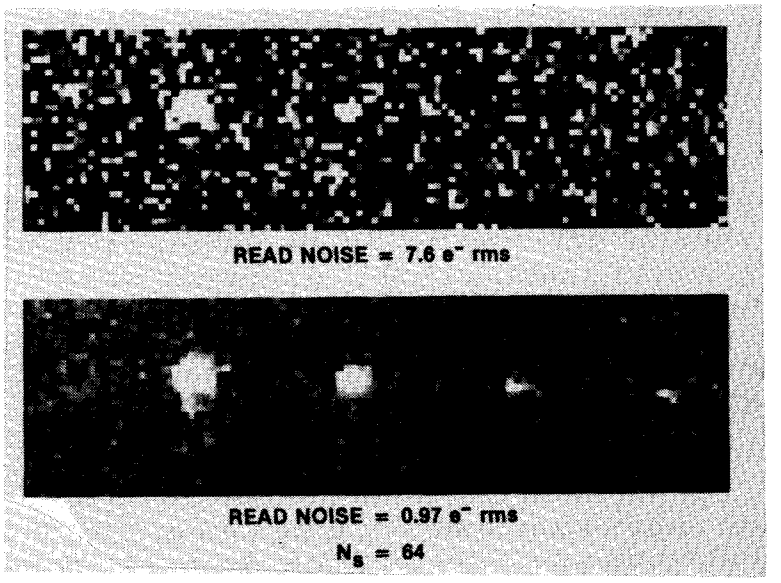

Figure 4. A Skipper response to 4 low-light-level point sources. The smallest point source seen in the bottom image is only 3-4 e-.

Figure 5 shows corresponding line traces taken through the four point images at a higher signal level (approximately 10 e- for the point source on the right side). In Figure 5a, single pixel sampling is employed, whereas Figure 5b uses all 64 samples to display improved response.

The experimental Skipper CCDs fabricated at Ford exhibit noise levels that range between 6 to 10 e- rms (single sampling). Employing 64 samples/pixel, the noise levels for the same CCDs are reduced to 0.75-1.25 e-. Noise levels below 0.5 e- have been achieved by employing 256 samples/pixel. It was observed that for more than 256 averages noise performance below this level begins to deviate from theory (i.e., square root noise relationship). Investigation into the quandary revealed that ultra-small signal sources on the array were responsible, sources that generate small amounts of signal variation from pixel-to-pixel which would not average out using multiple samples/pixel (i.e., dark current, spurious charge, luminescence, etc.)[1]. At this level, unwanted sub-electron signal sources are critical to Skipper CCD performance. For example, a dark signal of only 0.5 e-/pixel produces a shot noise component of 0.71 e-, enough to dominate a random read noise of 0.5 e-. Fortunately , we have found that these very small sources of charge can be controlled by cooling (thermal dark current), clock wave-shaping (spurious charge) and reduced voltage bias to the CCD (luminescence).

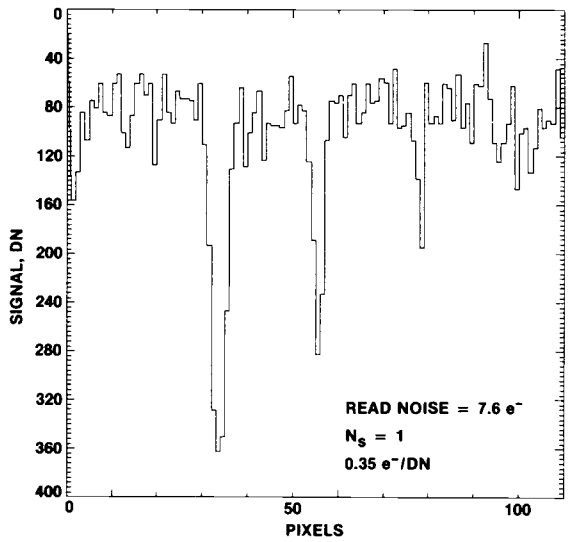

Figure 5a. Video line trace taken through the four point sources shown in Figure 4 at a slightly higher signal level. One sample/pixel is employed in this plot.

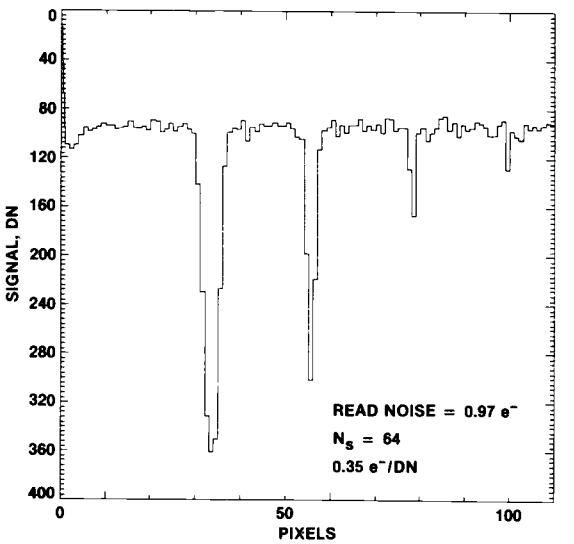

Figure 5b. Same line trace as Figure 5a employing 64 samples/pixel showing an improved noise floor.

For visible wavelength applications the Skipper CCD is only beneficial over a limited signal range due to shot noise limitations. The signal-to-noise (S/N) of an image generated by a Skipper CCD is derived by the formula:

$$S/N = S/(R^2/N_S + S)^{1/2} \quad (1)$$

where R is the read noise (rms e-, single sampling), N_S is the number of samples taken per pixel, S is the average signal level of the image (e-) and $S^{1/2}$ equals the signal shot noise.

Figure 6 plots S/N as a function of signal presenting a family of curves for various N_S . Each plot assumes a read noise of 10 e-. The useful dynamic range for multiple pixel averaging can be defined as the ratio of maximum to minimum applicable signal levels. The maximum applicable signal level is taken to be that at which the shot noise equals the read noise. In this case, multiple pixel averaging will result in no greater S/N increase than $2^{1/2}$ as N_S

approaches infinity. The minimum applicable signal level is that for which the lowest S/N acceptable to the user can be achieved with unlimited multiple pixel averaging. With these definitions, the useful dynamic range for the Skipper CCD is given by

$$DR = (R/(S/N)_m)^2 \quad (2)$$

where $(S/N)_m$ is the lowest signal-to-noise acceptable by the user. Assuming a 10 e- noise floor and a minimum S/N of 3, a useful dynamic range of 11 is calculated, as indicated in Figure 6.

From Eq. (2) it can be seen that the useful dynamic range decreases as the read noise is reduced. The dynamic range collapses to unity when a read noise of 3 e- is achieved, at which point multiple pixel averaging is not advantageous for visible imaging.

For detecting point sources of light on a black background (e.g., as in Figure 4) or individual photon events, the Skipper CCD is very beneficial since sub-electron noise floors can be provided. For example, CCDs are being applied to simultaneously count high energy photons and estimate their energy by measuring the amount of charge they generate. In an earlier paper[3], it was shown that the low-noise (3 e-) and near perfect CTE (0.999999) characteristic of today's CCDs have made it possible to achieve "Fano-noise-limited" performance over the soft x-ray regime, a condition where the detector's energy resolution is primarily limited by the statistical variation in the charge generated by the interacting x-ray photon. Noise levels less than 1 e- allow Fano-noise-limited performance to extend into the extreme UV. This noise level is presently achieved. If the noise floor can be lowered significantly below 1 e-, it is conceivable that the single photo-electron can be detected (a CCD type we refer to as the Quantum CCD). Developmental work in this area is underway.

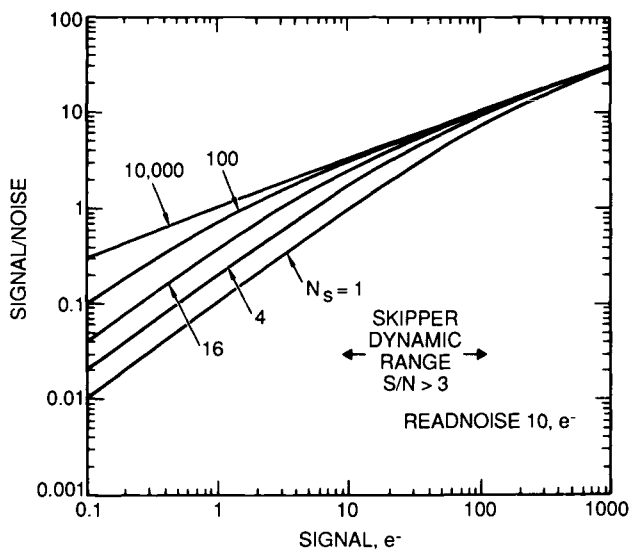

Figure 6. S/N plot for visible imagery for various N_S.

Figure 7 is a computer generated simulation for a Skipper CCD that is stimulated with boron x-rays (183 eV) that each generate 50 e-. The left image employs single sampling (N_S = 1) assuming an initial noise floor of 7 e-. The photon events are barely detectable in the image due to the high noise floor. In the image on the right, the noise floor is reduced to 0.61 e- by employing 128 samples/pixel. The events now are clearly seen.

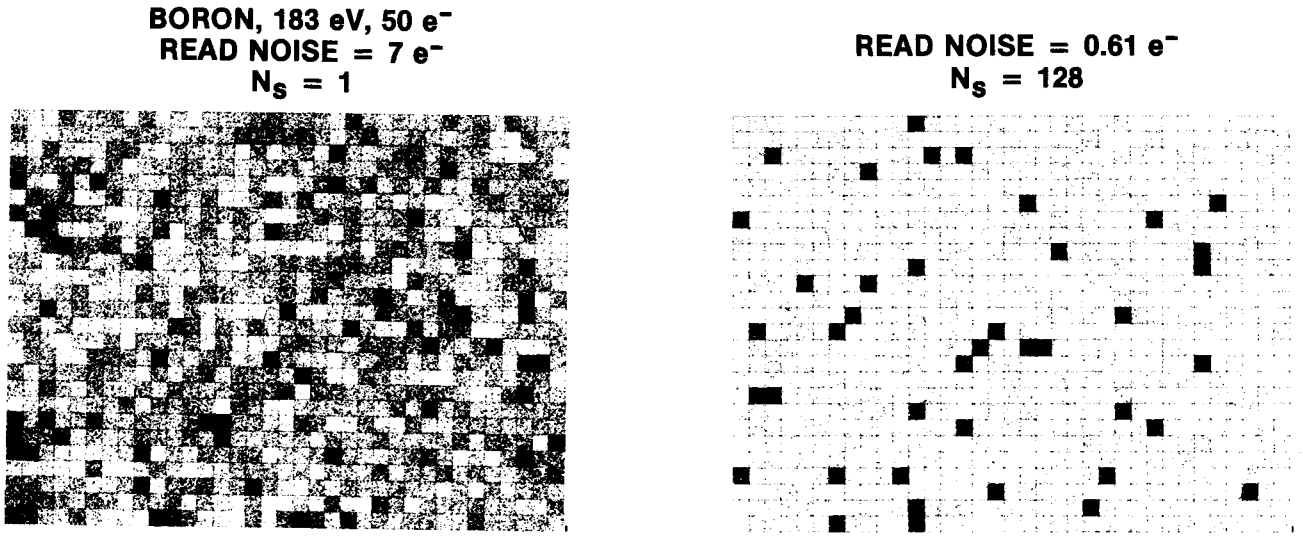

Figure 7. Computer simulation showing S/N improvement for boron x-ray events when the noise is reduced from 7 e- (left image) to 0.61 e- (right image) employing 128 samples/pixel.

The S/N in measuring an individual photon event for an averaging Skipper CCD is found by the formula:

$$S/N = S/((R^2/N_S)+S*F)^{1/2} \quad (3)$$

where F is the Fano-factor given empirically as 0.1, N_S is the number of samples/pixel, and S is the number of electrons generated by the interacting photon, found for silicon by E/3.65 where E is the energy of the photon in electron volts (eV).

Figure 8 plots Eq. (3) as a function of photon energy encompassing the EUV and soft x-ray spectrum for various N_S and assuming an initial read noise of 7 e-. Note for high energy photons (>1 keV) Fano-noise-limited performance is achieved by employing 16 samples/pixel. For low energies, multiple pixel sampling significantly improves the sensor's energy resolution; however, more samples are required. For instance, at 100 eV, 100 samples/ pixel improves the S/N by 5.36 times compared to single pixel sampling.

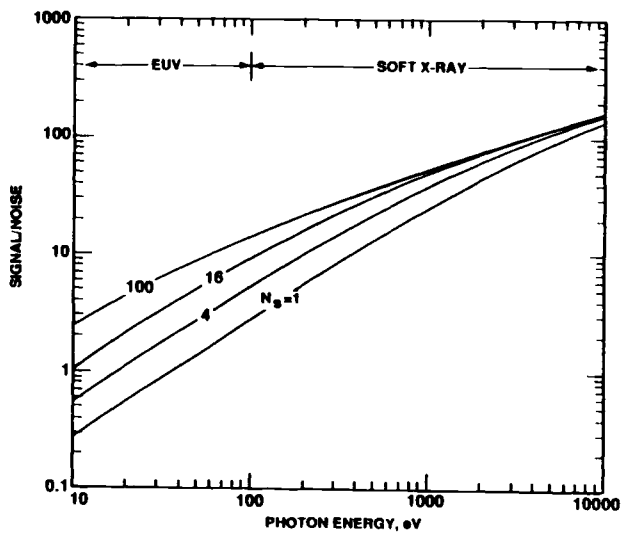

Figure 8. S/N plot for individual photon events for various N_S.

Figure 9 shows an x-ray image composed of individual x-ray events. Based on a single frame of data, each pixel in the left image is made from a single sample taken from a 64 sample set. The pixels in the right image include all 64 samples thereby reducing the noise by a factor of eight (below 1 e- rms). So comparisons can be directly made, the signals of the averaged image were multiplied by eight so an equal noise level is seen in the two images. The averaged image uncovers more charge associated with the x-ray event not seen in the single sampled image. For example, the horizontal events barely detected in the noisy image are clearly seen in the averaged image. These particular events are generated when x-ray photons interact outside the array below the horizontal register. As charge diffuses towards this register the event cloud expands resulting in the extended images seen.

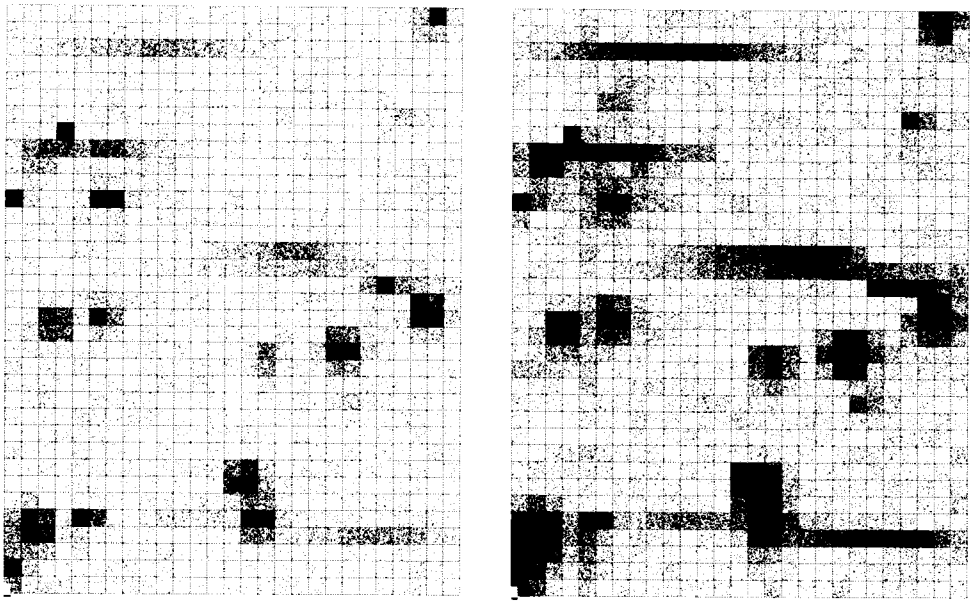

Figure 9. X-ray responses employing single pixel sampling (left) and 64 samples/pixel (right). The image on the right exhibits a read noise of less than 1 e- rms.

The Skipper CCD has also revealed that the x-ray event is considerably larger in extent than previously thought. In a earlier paper[3], we attempted to measure the Fano-factor using the CCD. These experiments always yielded a Fano-factor greater than the accepted value (F=0.1) by about a factor of two. Charge spreading among pixels causes the energy of the photon to be underestimated in conjunction with increasing the uncertainty in the absolute charge measured. These factors make it appear that a larger Fano-factor is at work. The Skipper CCD has allowed us to find small amounts of hidden charge buried in the noise resulting in smaller calculated Fano-factor.

1.4 Summary

The primary disadvantage in achieving sub-electron noise floors using the Skipper CCD is the large number of samples required which may result in excessive frame times for larger CCD imagers. Frame time can be minimized by allocating most of the signal processing time to sampling the video signal and reducing overhead timing functions such as ADC conversion time. Further, for most imaging applications it is not necessary to interrogate every pixel in an image multiple times. Alternatively, multiple sampling is performed only in those regions of interest and other areas of the array that are either void of charge or shot noise limited are skipped. This process can be automatically set up by utilizing two Skipper amplifiers incorporated into the horizontal register separated by a fixed number of pixels. The first floating gate is used to detect the incoming signal level to decide if the second gate should perform multiple sampling. Read time can also be reduced by fabricating Skipper CCDs that employ multiple floating gates making it possible to average several pixels simultaneously.

An important developmental task remaining is to improve Skipper performance by minimizing the noise associated with the floating gate amplifier. As indicated above, experimental floating gate amplifiers currently exhibit noise floors as low as 6 e-. Optimization of the amplifier could reduce the noise floor below 3 e- thereby decreasing the number of samples/pixel by a factor of 4 while yielding the same noise performance. The primary factor in reducing amplifier noise will be made by increasing the floating gate sensitivity (i.e., Volts/e-). This will be accomplished by reducing the capacitance associated with the floating gate and eliminating parasitic capacitances in the vicinity. For example, current Skipper CCDs could be improved by reducing the size of the horizontal register and the associated channel capacitance. In some applications, the size of the floating gate can also be made as small as possible since full well capacity is not an important factor.

The ultimate test for the Skipper CCD, yet to be achieved, is to detect the single photo-electron. Skipper cameras have been constructed which employ ultra high gain, in excess of 100 ADC counts per electron. Assuming that the noise can be lowered to 0.2 e- rms using multiple sampling, there is no fundamental reason why the photo-electron can't be detected. It will be interesting to see if the CCD can accomplish this feat in the near future.

2. 4096X4096 PIXEL CCD

2.1. Introduction

Almost two decades have passed since the first commercially available 100x100 pixel CCD was introduced by Fairchild Semi-conductor. Following its success, CCD groups began fabricating sensors with pixel counts compatible with commercial TV formats (i.e., 512Vx320H). Until about two years ago the 512x512 sensor was considered to be the largest practical sized CCD that technology could provide, although larger, expensive custom imagers were under development behind the scenes (i.e., the TI 800x800 CCDs[1]). Today the situation has changed remarkably, prompted by intense competition among CCD manufacturers. The high CTE performance reported above in conjunction with high fabrication yields has opened the door for ultra-large CCD arrays. For example, the 1024x1024 pixel CCD is routinely fabricated and is now considered the "standard" format by the scientific imaging community. The 2048x2048 CCD is being made by three CCD manufacturers (Kodak, Tektronix, and Ford Aerospace), and a few of these giant chips are actually generating science at selected astronomical observatories. Ford Aerospace has taken the lead in producing a 4096x4096 7.5-micron pixel sensor, the largest CCD fabricated in terms of pixel count[4]. The new sensor contains over 1600 times the number of pixels than the precursor 100x100 Fairchild CCD and is equivalent to over one hundred 512x320 CCDs. The 2048 and 4096 imagers clearly demonstrate that CCD technology is advancing at an accelerated pace. A brief discussion of the 4096 CCD is provided below.

2.2 Ford History

During the past four years, the Ford Aerospace Corporation has collaborated with outside CCD groups to develop large custom area array CCDs for scientific use. Initial efforts were launched by the Photometrics group who funded and directed activities which led up to the 516x516 4-phase (two-level poly) 20-micron pixel CCD[5]. Photometrics' objectives at that time were motivated by the lack of scientific grade CCDs with formats greater than/or equal to 512x512 pixels as required for their CCD camera systems. The endeavor at Ford successfully produced about 100 high-performance scientific sensors each of which exceeded the performance goals initially specified by Photometrics.

News spread quickly about Photometrics' accomplishments and prompted other organizations to team with Ford in developing CCDs for their special imaging needs. At the beginning of 1988, Science Applications International Corporation (SAIC) approached Ford and JPL to fabricate a custom 1024x1024 3-phase (three-level poly) CCD to be utilized in several of their proposed camera systems. This venture was also very successful with performance equal to the Photometrics CCD having been demonstrated[6]. As a side benefit, the yield for the

1024 CCD was considerably higher than that achieved for the Photometrics 516 CCD (about a factor of 100 in terms of pixel count).

Other Ford activities which have recently been successful include the CIT Mars Observer Camera line array CCDs (2048x1, 3456x1), the JPL CRAF/Cassini CCD (1024x1024), the Ford 2048x2048 7.5 and 15-micron CCDs, the Skipper CCD discussed above, and the CIT/JPL resistive gate CCD.

2.3 Architecture

The layout of the 4096 sensor is shown in Figure 10. The design is similar to layout configurations implemented by other CCD manufacturers (Thompson CSF, Tektronix, TI, etc.). The upper half of the 4096 CCD can be read out using the top horizontal register and the lower section using the bottom register thereby providing two-channel operation if desired. Alternatively, the whole array can be clocked out either to the top or bottom register using a single amplifier stage.

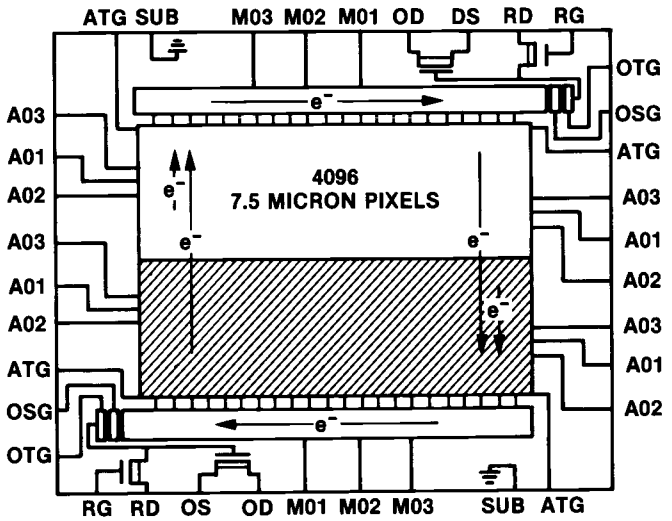

Figure 10. Layout of the 4096x4096 CCD.

Each horizontal register has twice the area of a vertical array pixel. This provides for signal summing of adjacent rows of the array in the horizontal register prior to the readout of a row. The horizontal register is extended 32 pixels past the edge of the array. An output well (Figure 11), the last storage gate in the horizontal register, is twice the capacity of a horizontal pixel. This provides for summing of adjacent columns in the array. Thus, with proper clocking, the 4096 CCD can be reduced to a 2048x2048 array with 15-micron pixels.

The output amplifier consists of a single stage source follower. A geometry of 6Lx60W-microns achieves an output sensitivity of 2 to 3 micro-V/e-. A single gate is used to reset the channel to the voltage set on the reset drain. Noise performance of the on-chip amplifier is typically 5 e- assuming a 4 micro-sec sample time.

The addition of a separate mask level and a second layer of aluminum, allows one to mask off one-half of the imaging area. In this manner, the device can be operated in a frame store mode.

Each pixel of the 4096 CCD is 7.5-microns square consisting of three phases. The active area of the device is 3.72 cm by 3.72 cm. The 7.5-micron pixel size was selected so that four imagers could be fabricated on a single four-inch wafer. A larger pixel would have reduced the number chips on the wafer affecting the yield of usable devices.

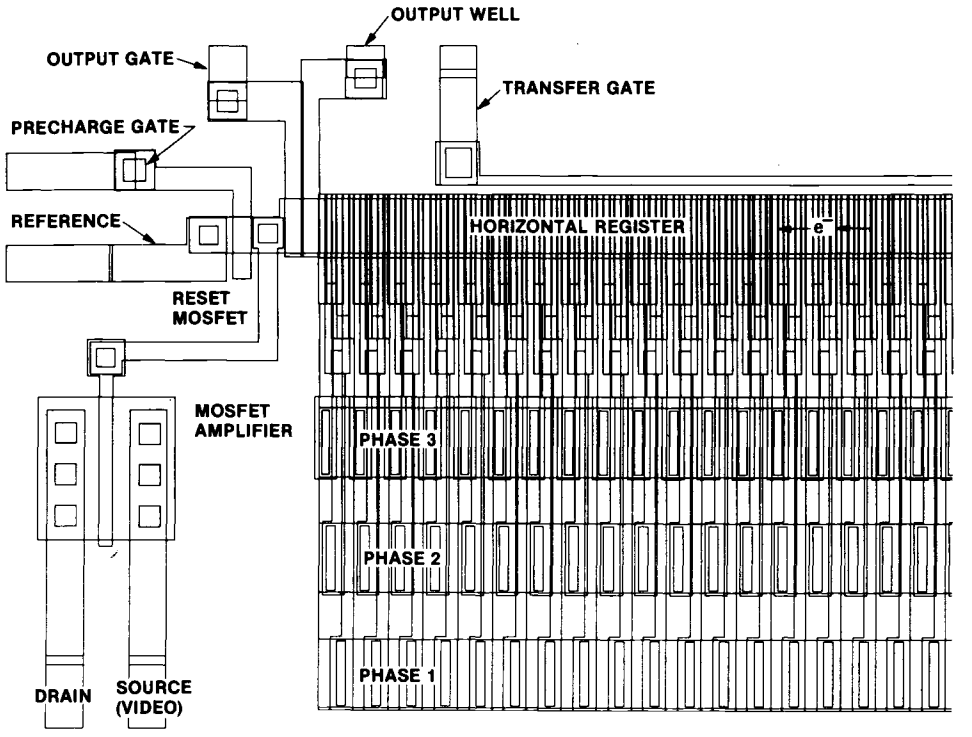

Figure 11. Design layout of the 4096 output structures.

2.4 Fabrication

Although a two-level poly process at Ford has been traditional, three-levels of poly were utilized for the 4096 array because of its size. This adds an additional level of poly-silicon processing to the fabrication; however, the improved yield by isolating each clock phase more than compensates. The three-phase design also allows more tolerance in defining the small 7.5-micron pixel. A four-phase double level poly CCD requires minimum design rules of 1.75-microns whereas 2.5-micron geometries are required for a three-level CCD process.

Experience at Ford has demonstrated that 30-50 ohm-cm p-type 15-micron epitaxial silicon on a 0.01-0.02 ohm-cm substrate provides the optimum trade off in dark current, CTE, charge collection efficiency (CCE) and response in addition to acting as a preferential etch material for thinning the device and implementing backside-illumination.

A standard local oxidation of silicon (LOCOS) process is used to define the active areas of the device. A phosphorus implant is used to define the buried channel of the CCD. An oxide-nitride gate dielectric is formed (500/500Å), and three layers of poly-silicon are sequentially deposited (1500Å), patterned, etched and oxidized to form the three clock phases. Next, an intermediate oxide layer is deposited. Contact holes are opened up and aluminum deposited to form interconnection of various structures. A protective overcoat glass is deposited and, if desired, a second layer of metal is deposited forming the shield plate for frame store operation.

A barrier mask allows a boron implant under phase 3 to adjust the channel potential and thus confine each pixel's signal charge during multi-pinned-phase (MPP) operation[3,6,7].

Results of the processing runs have been excellent with the first lot of 4096 imagers achieving better than a 50% shorts < (1 meg-ohm) yield. Very good cosmetically clean imagers have been produced.

2.5 Performance

The performance achieved by the 4096 sensor is comparable to other Ford CCD imagers[4,5,6]. A full well capacity of 10,000 e- and 20,000 e- is achieved in the MPP and the partially inverted modes, respectively. On-chip amplifier linearity is better than 0.5% over the sensor's dynamic range. Dark current generation rates using MPP, partially inverted, and non-inverted operation are 0.027, 0.12 and 1.1 nano-amps/cm^2 respectively at room temperature. A 45% peak QE is achieved at 7000Å. Pixel nonuniformity is less than 1.5% as measured by photon transfer, assuming partially inverted operation.

The CCD has been characterized using an Fe-55 x-ray source (1620 e-). CTE, for example, is better than 0.99999 for the vertical and horizontal registers without the addition of fat-zero charge. This performance is consistent with smaller Ford CCDs indicating CTE for the 4096 imager is bulk state limited (i.e., limited by the density of bulk states in the starting silicon material). A dozen or so small charge traps (<200 e-) are observed within the array signifying that the trap population for the 4096 device is low, as is characteristic of Ford CCDs.

The 4096 does not exhibit surface residual image if clocked MPP or partially inverted. These modes of operation furnish holes at the Si-SiO_2 interface which recombine with electrons that are trapped at the interface when the CCD signal exceeds full well[1,6].

Assuming 25 k pixels/sec pixel rate, typical of slow scan astronomical cameras, the 4096 sensor requires 11.3 minutes for complete frame read out (using a single amplifier). New problems are created because of the long read time. For example, one's patience wears thin waiting for the device to clear itself when it is mistakenly over-exposed. Fortunately by employing inversion techniques the 4096 sensor can be erased in 40 millisecs without horizontal charge back-up. This is readily accomplished by running the verticals rapidly (10 micro-sec/line) while inverted and freezing the horizontals in the non-inverted state. Under these operating conditions the horizontal register acts as a dump drain accepting any amount of charge transferred into it. Bias conditions are such that charge diffuses down the register to the output diode. We have found that the fast erasure mode is required to speed up testing when characterizing the sensor.

Figure 12 shows three images of a dollar bill taken with an experimental 4096 CCD. The device exhibits only one saturated column blem, two blocked channels and a few low-level traps. It is impossible for us to display the entire 4096 image format due to the number of pixels involved and, therefore, only a partial area can be displayed at any one time. Figure 12a displays a 600Vx1000H section of the device at a peak signal level of 500 e-. Figure 12b is a magnified view of Figure 12a covering an area of 300Vx400H pixels. The sub-area represents 0.72% of the sensor. Figure 12c shows a 112Vx150H pixel region representing only 0.1% of the active area. Individual pixels can be seen at this magnification. Curiously, this number of pixels displayed, although small, is still greater than the 100x100 Fairchild CCD that we tested nearly 18 years ago.

2.6 Summary

The 4096x4096 CCD is currently the largest CCD manufactured in terms of pixel count. The 4096 is the first CCD fabricated that can directly compete with the resolution capability of photographic film. The resolution power of the 4096 is truly awesome. For example, two football fields set side-by-side can be resolved to 1 inch/pixel (including the side and goal zones). Looking skyward, the 4096 CCD can cover 68 arc minutes of the sky with 1 arc sec resolution (the moon extends about 32 arc minutes).

The success of the 4096 CCD implies that even larger imagers are possible. Assuming that applications exist, it appears that the largest CCD that can be fabricated with 4-inch wafers is a 8192x8192 pixel device, although yield will be low since the CCD would occupy the entire wafer (similar to the Tektronix 2048x2048 CCD which utilizes pixels greater than 20-microns). However, a 8192 CCD would present numerous difficulties for the user, primarily the problem of storing huge amounts of data. A 8192 CCD would produce over 130 million bytes of information per image assuming 16 bit encoding. Such an enormous amount of information is equivalent to a 27 million-word book or about 250 encyclopedias. The sensor format would match that of 409 320x512 CCDs. Readout time

would also present a problem. Assuming a single channel operating at 25 k pixel/sec, the device would require 42 minutes for readout. There are no immediate plans to fabricate such a device at Ford or at any other CCD manufacturer.

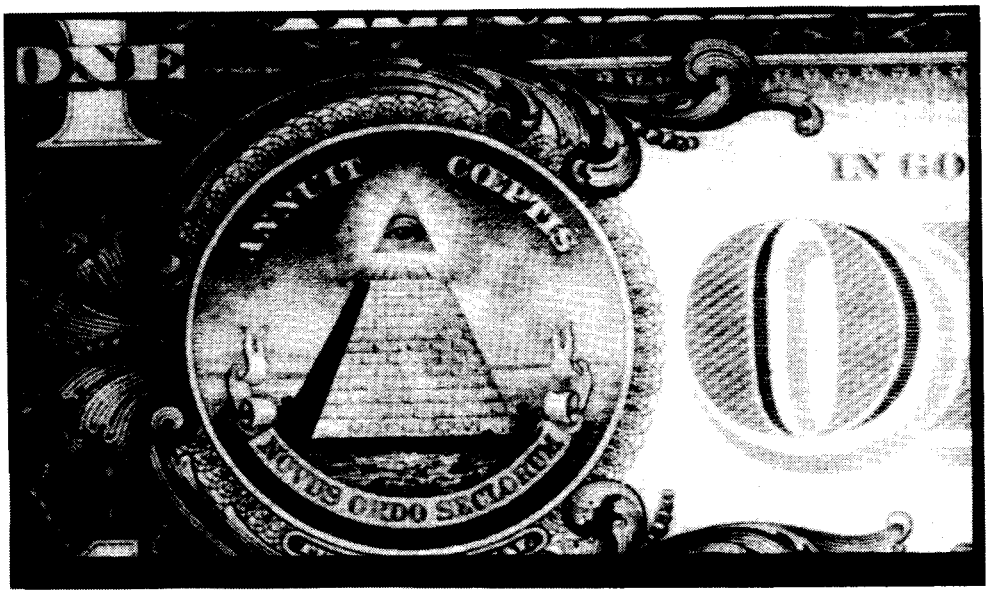

Figure 12a. Dollar bill image taken with the 4096 imager. A partial region occupying 600Vx1000H pixels that embodies 3.5% of the CCD.

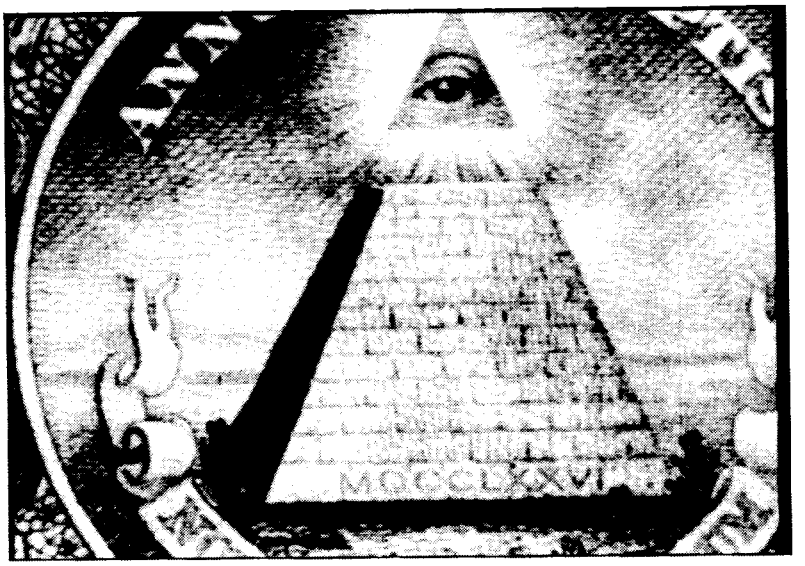

Figure 12b. Magnified view of Figure 12a of a 300Vx400H pixel section representing 0.72% of the CCD.

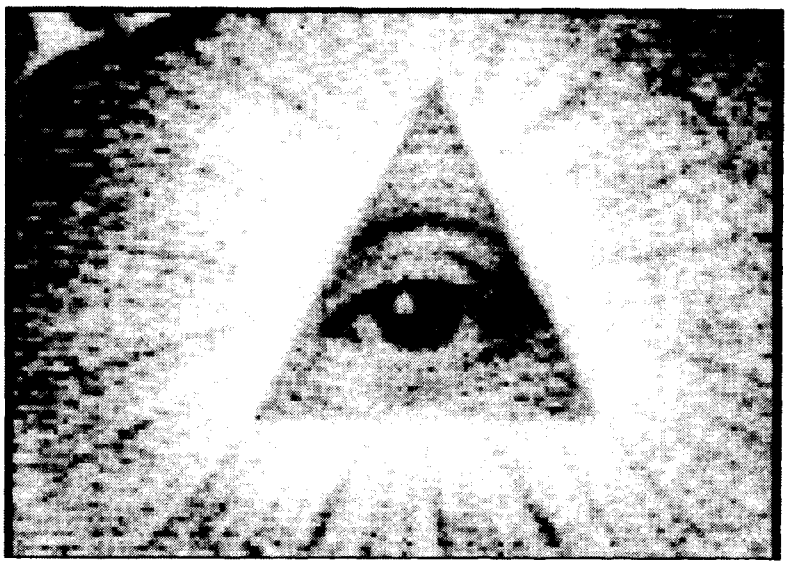

Figure 12c. Magnified view of Figure 12b showing 112Vx150H pixels representing only 0.1% of the device.

3. ACKNOWLEDGMENTS

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