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New Class of Power Converter for Performing the Multiple Operations in a Single Converter: Universal Power Converter

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Abstract: Universal power converters (UPCs) have aroused significant attention in performing multiple operations in a single power converter. Furthermore, they contribute to economic operation and improved system performance. In this work, a new configuration of the universal power converter (UPC) was proposed by using a simple switching arrangement. It can perform different modes of operations, such as AC–DC, DC–DC, DC–AC, AC–AC, and cyclo-converter operations. In DC–DC conversion, the proposed configuration can perform buck mode, boost mode, and buck–boost mode of operations. Moreover, in DC–AC conversion, it gives better total harmonic distortion (THD). The effectiveness of the proposed configuration was verified by an extensive simulation, using MATLAB/Simulink environment. A low-power prototype circuit was designed to test the viability of the proposed circuit configuration and validated with simulation results.

Keywords: DC–DC converter; DC–AC converter; AC–AC converter; cyclo-converter; universal converter

Citation: Mudadla, D.; Potnuru, D.; Satish, R.; Abdelaziz, A.Y.; El-Shahat, A. New Class of Power Converter for Performing the Multiple Operations in a Single Converter: Universal Power Converter. *Energies* **2022**, *15*, 6293. https://doi.org/10.3390/en15176293

Academic Editors: Alon Kuperman, Feng Liu, Zhiwei Liu, Ming Chi and Ming-Feng Ge

Received: 25 June 2022
Accepted: 22 August 2022
Published: 29 August 2022

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1. Introduction

Universal power converters (UPCs) have many advantages over conventional solutions [1–4] employing multiple single converters; the advantages include lower-cost characteristics, compact size, high power density, etc. This class of power converters is called "universal" because the inputs and outputs of the converters can be DC or AC. Therefore, they can be employed in various applications, including, but not limited to, photovoltaic (PV) power generation, battery–utility interfaces, and nanogrids. Therefore, UPCs are a suitable fit for nanogrids, electric vehicles (EVs), and photovoltaic (PV) applications [5–7].

Power electronic converters are classified into two types: non-isolated and isolated. In an isolated converter, the multi-winding transformer obtains high voltage gain and isolation between output and input ports. However, it has some drawbacks: more voltage stress, losses in the converter, converter size, and less converter efficiency [8–10]. Therefore, non-isolated converters have emerged in this field. There are several converter configurations in the category of non-isolated converters. Boost capacitor and passive clamp circuit-based DC–DC converters are suggested in Reference [11]. They improve the voltage gain and reduce voltage-stress spikes. However, they have a higher part count compared to the high-gain voltage converters, and where the coupled inductor size is larger than it is in the ordinary inductor. Similarly, a coupled-inductor and voltage-multiplier cell-based boost hybrid converter is proposed for high-gain applications [12]. A converter based on a switched inductor and capacitor hybrid is suggested in Reference [13] for improving converter performance. This converter operation is based on energizing the inductors in

series and discharging capacitors in parallel or vice versa. Nevertheless, this converter has more device count, leading to an increased converter cost and size. Furthermore, a new converter topology is presented for nanogrid application in Reference [14] and fuel application in Reference [15].

The combinations of two or more conventional converter features are used to derive a kind of a new DC–DC converter topology, and they are introduced as hybrid converters in References [16–20] for hybrid (DC–AC and DC–DC) power-conversion applications. A hybrid converter is suggested in Reference [21], using a phase-shifted full-bridge for electric vehicle charger applications. In this configuration, the limitations of the conventional PSFB converter are overcome. A hybrid full-bridge DC-to-DC converter is introduced for radiofrequency applications in Reference [7] to overcome the drawbacks of the filter size across the load and circulating currents of a conventional full-bridge converter. A hybrid step-down power factor correction (PFC) converter is presented in Reference [22]. It has combined features of boost PFC and buck PFC converter to improve the power factor. A switched-capacitor-based hybrid high-gain DC–DC converter is proposed in Reference [23]. It is derived from buck, boost, and buck–boost topologies. However, the number of capacitors causes extra cost and enhanced size.

A new topology of the universal power converter is proposed in Reference [24] to obtain all possible power conversions in a single stage, viz AC–AC and DC–AC. However, this converter has a complex structure with many switching devices. Along similar lines, another universal converter for battery-charging applications is suggested in Reference [25] and is suitable only for AC–DC and DC–DC with the buck–boost mode of operation. However, it is not ideal for DC–AC, and AC–AC power-conversion applications. A fully modular configuration is developed in References [21,26] for universal (AC–DC, DC–AC, and DC–DC) power-conversion applications. Moreover, a novel solar converter for applicability in DC and AC microgrid is proposed in Reference [27] and a universal power converter using buck–boost converter and full bridge circuit is proposed in Reference [28]. However, these converters are not fully universal in view of different types of sources and loads.

In this paper, a novel universal power converter that is first of its kind is introduced; the network topology looks like a front-end semiconductor switch connected to an H-bridge network. The application field of the proposed configuration can be used to perform multiple operations in a single converter, such as DC–DC, AC–DC, AC–AC, DC–AC, and cyclo-converter operations. Therefore, it is suitable for (i) renewable-energy integration with solar PV roof-top application, (ii) remote village DC microgrid application, (iii) flexibly connecting to AC or DC loads in a small commercial area application, etc.

The paper is arranged as follows: Section 2 describes the suggested topology and various operation modes. The parameter design and power analysis and comparative analysis are presented in Section 3. The simulation and experimental results in various configurations are discussed in Section 4. The proposed work is concluded in Section 5.

2. Proposed Universal-Power-Converter Configuration and Modes of Operation

The UPC is a relatively new class of power converter. The schematic circuit diagram of the proposed UPC is shown in Figure 1. Figures 2–8 show different circuit configurations of the developed converter, along with their equivalent circuits. The current through the inductor (i_L) and the voltage across the capacitor (v_C) are also presented in each mode of operation.

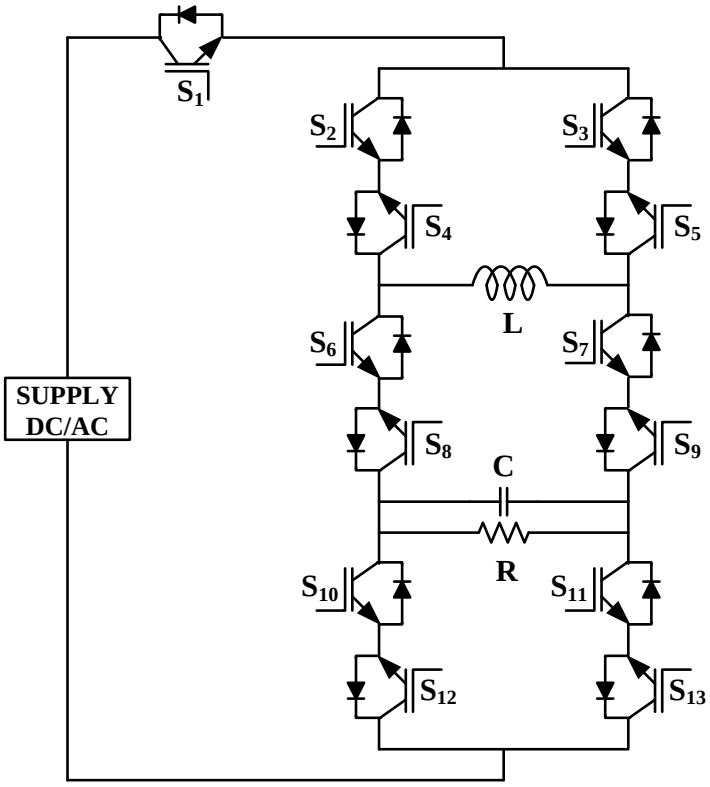


Figure 1. Proposed UPC topology.

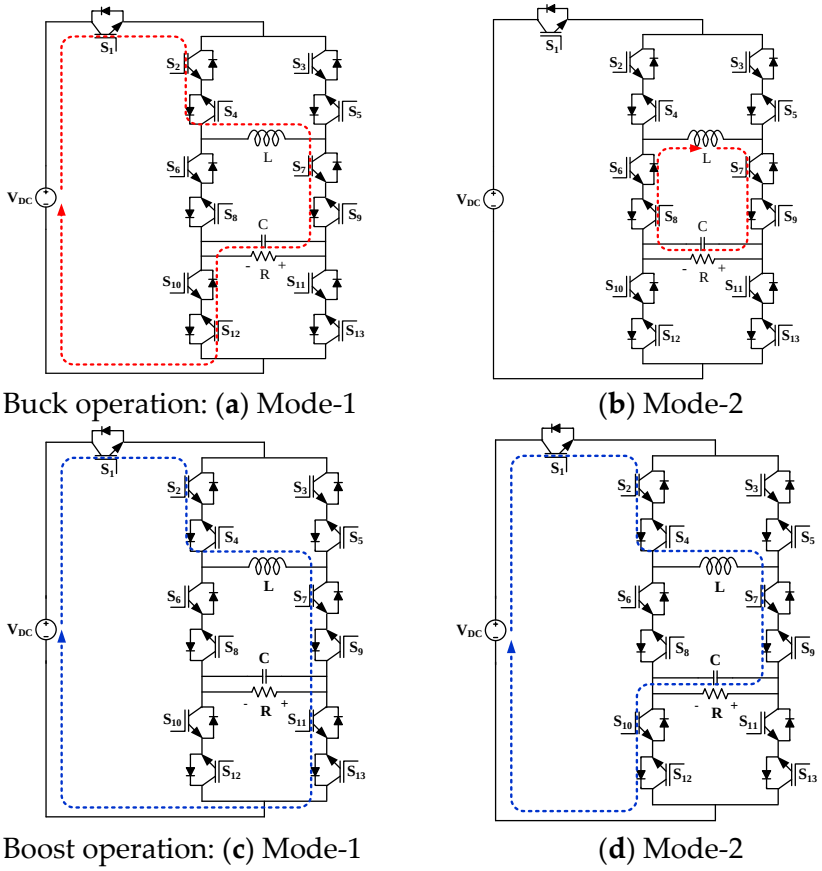


Figure 2. *Cont.*

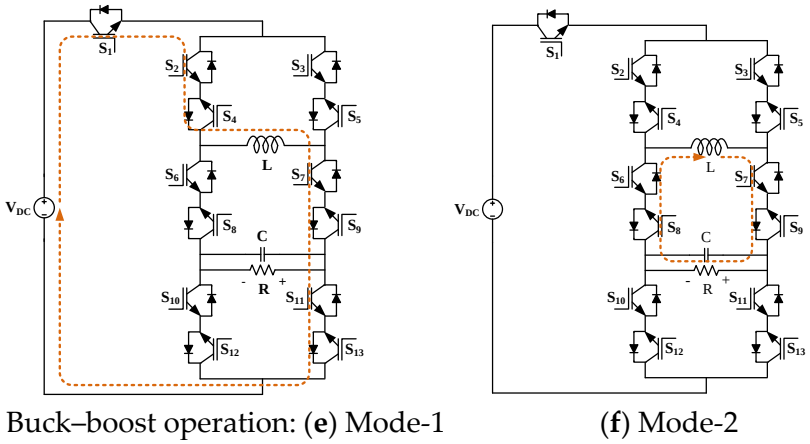


Figure 2. Equivalent circuits of UPC during DC–DC conversion: buck mode (**a**,**b**), boost mode (**c**,**d**), and buck–boost mode (**e**,**f**) of operation.

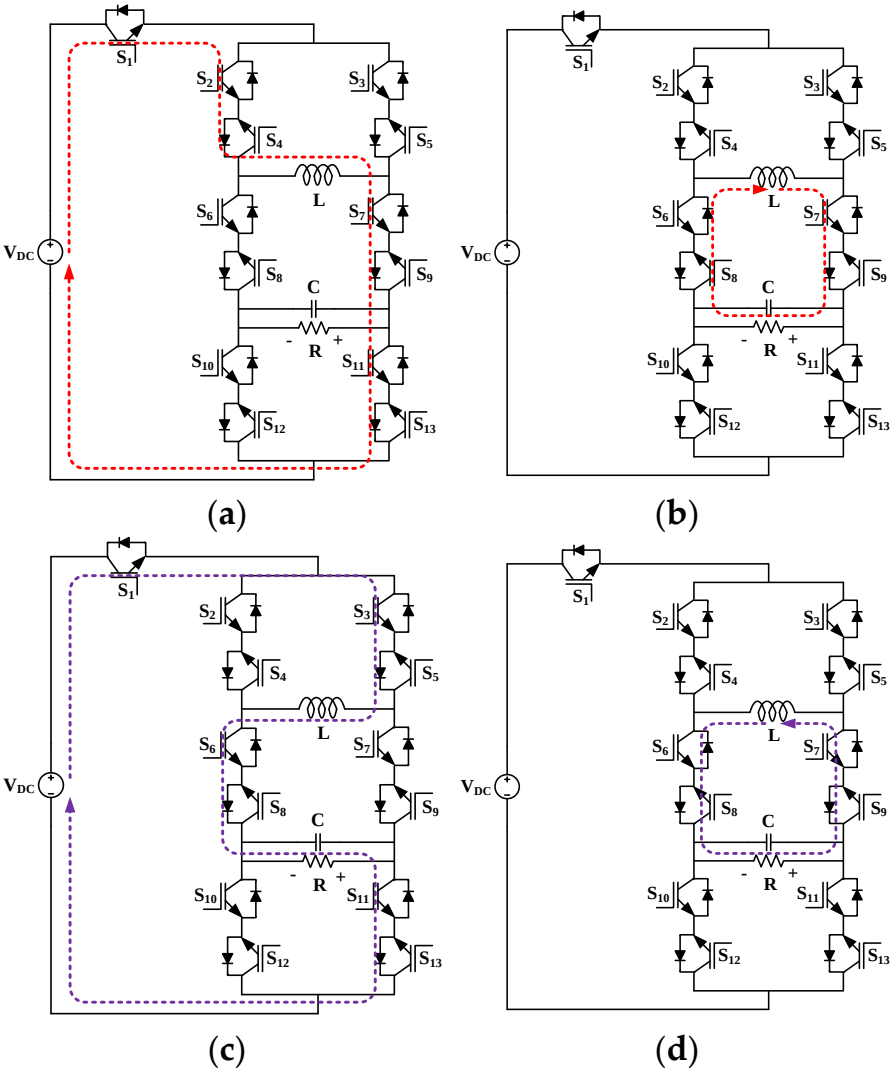


Figure 3. Equivalent circuits of UPC for different modes of operation during DC–AC conversion (inverter operation): (**a**) Mode-1, (**b**) Mode-2, (**c**) Mode-3, (**d**) and Mode-4.

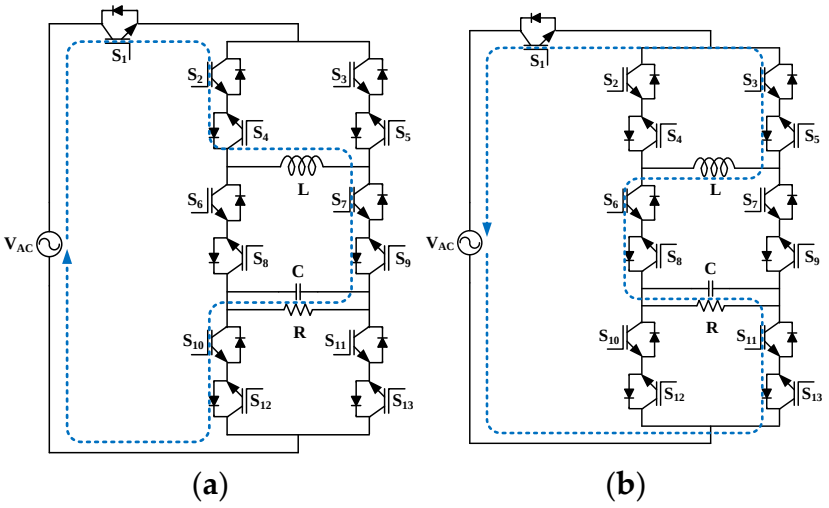


Figure 4. Equivalent circuits of different modes operation during rectifier operation: (**a**) Mode-1 and (**b**) Mode-2.

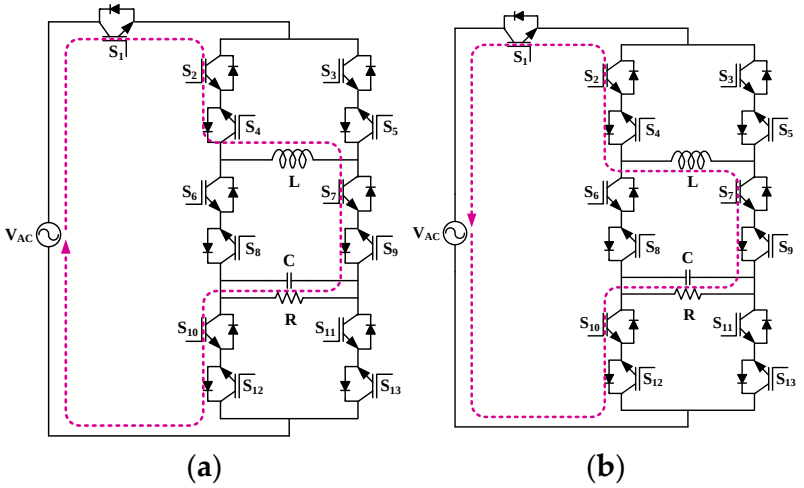


Figure 5. Equivalent circuits of different modes operation during AC voltage controller operation: (**a**) Mode-1 and (**b**) Mode-2.

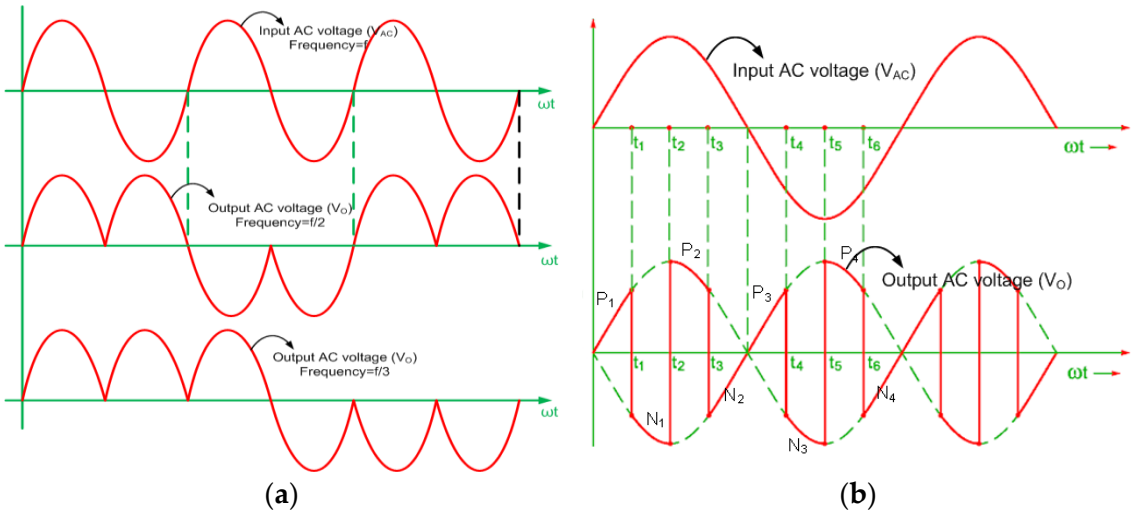


Figure 6. (**a**) Cyclo-converter's typical output voltage waveform for step-down operation and (**b**) cyclo-converter's typical output voltage waveform for step-up operation (fo = 2f).

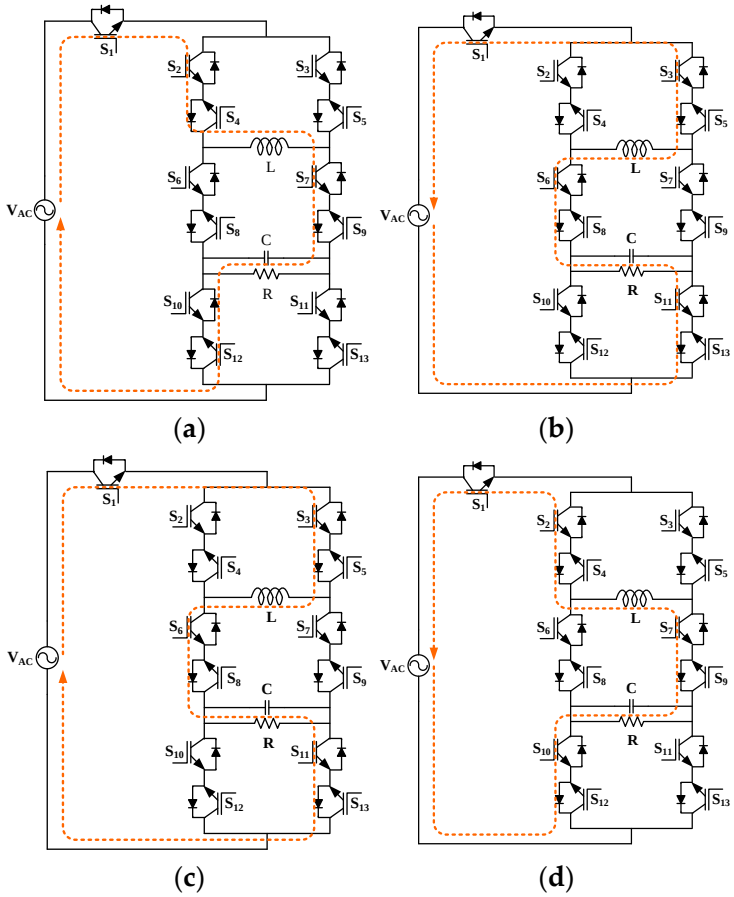


Figure 7. Equivalent circuits of different modes operation during cyclo-converter operation: (**a**) Mode-1, (**b**) Mode-2, (**c**) Mode-3, and (**d**) Mode-4.

The proposed converter has the following features:

(1) The proposed configuration has a reduced number of components compared with the individual conventional converters combined to obtain different modes of voltage conversion.
(2) It can perform the AC–DC, DC–DC, DC–AC, and AC–AC (cyclo-converter and ac voltage converter) operations with the single converter.

2.1. Various Circuit Configurations: DC–DC Converter Operation

2.1.1. DC–DC Converter (Buck Mode)

Switching State 1

In this operating mode, the switching action happens between the switches S_1, S_2, S_7, and S_{10}; the remaining power semiconductor switches are kept off. Now, the input DC source (V_{DC}) supplies energy to the load, and the inductor is energized accordingly. The corresponding circuit in this Switching State-1 is shown in Figure 2a.

Switching State 2

During this switching mode, the supply input is switched off, and the inductor (L) delivers its stored energy to the load (R) through the active switches S_7 and S_8. The circuit in this mode of operation is represented in Figure 2b.

The output voltage (V_0) expression in buck operation can be expressed as follows:

$$V_0 = V_{DC}d \tag{1}$$

where d is the duty ratio.

2.1.2. DC–DC Converter (Boost Mode)

Switching Mode 1

In this operating mode, active switches S_1, S_2, S_7, and S_{11} are turned on; the corresponding current flow direction is illustrated in Figure 2c. In this switching state, the voltage source charges the inductor, and the capacitor delivers the stored energy to the load R.

Switching Mode 2

Figure 2d shows the equivalent circuit in this mode of operation. During this mode, stored energy in the inductor is discharged and delivered to the capacitor and load (R) through the switches S_1, S_2, S_7, and S_{10}.

The output voltage (V_0) expression in boost operation can be expressed as follows:

$$V_0 = \frac{V_{DC}}{(1-d)} \tag{2}$$

where d is the duty ratio.

2.1.3. DC–DC Converter (Buck–Boost Mode)

Switching Mode 1

In this mode of operation, controlled devices S_1, S_2, S_7, and S_{11} are switched on, and the inductor (L) is energized by the input supply (V_{DC}). Similarly, the capacitor releases its stored energy to the load (R). The direction of current flow in this mode of operation is illustrated in Figure 2e.

Switching Mode 2

In this switching operation, the energy stored in the inductor is released to the load (R) through the switches S_7 and S_8; Figure 2f shows the equivalent circuit.

The output voltage expression in the buck–boost mode can be expressed as follows:

$$V_0 = \frac{V_{DC}d}{(1-d)} \tag{3}$$

where d is the duty ratio.

2.2. Various Circuit Configurations: DC–AC Conversion (Inverter Operation)

The proposed topology is operated in the inverter configuration, and the corresponding modes of operation, along with their equivalent circuits, are illustrated in Figure 3a–d.

Mode 1:

The switches S_1, S_2, S_7, and S_{10} are switched on in this mode, and the source port energizes the inductor; the resulting equivalent circuit is depicted in Figure 3a.

Mode 2:

The supply voltage remains off in this mode, and the energy stored in the inductor is de-energized by the devices S_7 and S_8; the resulting equivalent circuit is depicted in Figure 3b, wherein Modes 1 and 2 provide a positive output voltage level.

Mode 3:

The switches S_1, S_3, S_6, and S_{11} are turned on, and the inductor is energized by the input voltage; the resultant equivalent circuit is shown in Figure 3c.

Mode 4:

The energy stored in the inductor is de-energized through the switches S_6 and S_9 in this mode, and the resultant circuit is shown in Figure 3d. Modes 3 and 4 generate the negative level of output voltage.

The expression of the rms value for fundamental component of the output voltage is as follows:

$$V_{rms} = \sqrt{\left[\frac{1}{\pi}\int_{0}^{\pi} V_{DC}^{2}(t)dt\right]} \quad (4)$$

where V_{DC} is the input voltage.

2.3. Various Circuit Configurations: AC–DC Conversion (Rectifier Operation)

The designed UPC can also be operated as a rectifier, as shown in Figure 4a,b. This configuration has two modes of operation with respect to the resistive load.

Mode 1:

The switches S_1, S_2, S_7, and S_{10} are fired in the positive half cycle at an angle, α. From $\omega t = \alpha$ to π, the switches conduct, and the load voltage varies from 0 to $V_m \sin\omega t$. The current takes the path V_{Acph}-S_1-S_2-L-S_7-LOAD-S_{10}-V_{ACN}, and the load voltage is in phase with the load current in Figure 4a.

Mode 2:

In the negative half cycle, the switches S_{13}, S_8, and S_5 are made to conduct from $\omega t = \pi$ to 2π. In Figure 4b, it can be seen that the current flows through the path V_{Acph}-S_{13}-S_8-LOAD-L-S_5-V_{ACN}. The output voltage can be determined by using the following equation:

$$V_0 = \frac{1}{\pi}\int_{\alpha}^{\pi} V_m sin\omega t d(\omega t) \quad (5)$$

2.4. Various Circuit Configurations: AC–AC Conversion (AC Voltage Controller Operation)

Mode 1:

During the positive half cycle, switches S_1, S_4 and S_7 are fired at a delay angle, α, and it conducts from $\omega t = \alpha$ to π for resistive load. The path for the flow of the current, as shown in Figure 5a, is given by V_{Acph}-S_1-S_2-L-S_4- S_7-LOAD-S_{10}-V_{ACN} for resistive load.

Mode 2:

In the negative half cycle, the switches S_6 and S_5 are conducted from $\omega t = \pi + \alpha$ to 2π, and the current flows through the path V_{Acph}-S_{12}-S_9-LOAD-S_4-L-V_{ACN}, as shown in Figure 5b. The RMS value of output voltage can be determined by using the following equation:

$$V_{Or} = \left[\frac{1}{\pi}\int_{\alpha}^{\pi} V_m^2 sin^2\omega t d(\omega t)\right]^{1/2} \quad (6)$$

where α is the delay angle.

2.5. Various Circuit Configurations: AC–AC Conversion (Cyclo-Converter Operation)

The operation of the cyclo-converter is described here for step-down frequency (i.e., output frequency = supply frequency/2). The switching combination in step-down frequency is shown in Table 1. Similarly, it can be extended to the step-up frequency operation of the cyclo-converter. The corresponding switching combination at different output frequencies is show in Table 2. The theoretical waveforms of the proposed converter in step-down and step-up frequency modes of operation are illustrated in Figure 6a,b respectively.

Table 1. Step-down operation for one cycle of output voltage at different frequencies.

Output Frequency	Mode of Operation during Input Supply		Output Pulse Polarity	Switches Conducting
f/2	Positive half cycle	Mode.1	Positive	S_1, S_2, S_7, and S_{10}
	Negative half cycle	Mode.4	Positive	S_{12}, S_9, and S_4
	Positive half cycle	Mode.3	Negative	S_1, S_3, S_6, and S_{11}
	Negative half cycle	Mode.2	Negative	S_{13}, S_8, and S_5
f/3	Positive half cycle	Mode.1	Positive	S_1, S_2, S_7, and S_{10}
	Negative half cycle	Mode.4	Positive	S_{12}, S_9, and S_4
	Positive half cycle	Mode.1	Positive	S_1, S_2, S_7, and S_{10}
	Negative half cycle	Mode.2	Negative	S_{13}, S_8, and S_5
	Positive half cycle	Mode.3	Negative	S_1, S_3, S_6, and S_{11}
	Negative half cycle	Mode.2	Negative	S_{13}, S_8, and S_5
f/4	Positive half cycle	Mode.1	Positive	S_1, S_2, S_7, and S_{10}
	Negative half cycle	Mode.4	Positive	S_{12}, S_9, and S_4
	Positive half cycle	Mode.1	Positive	S_1, S_2, S_7, and S_{10}
	Negative half cycle	Mode.4	Positive	S_{12}, S_9, and S_4
	Positive half cycle	Mode.3	Negative	S_1, S_3, S_6, and S_{11}
	Negative half cycle	Mode.2	Negative	S_{13}, S_8, and S_5
	Positive half cycle	Mode.3	Negative	S_1, S_3, S_6, and S_{11}
	Negative half cycle	Mode.2	Negative	S_{13}, S_8, and S_5

Similar way the procedure is repeated for other output frequencies. Where f is input supply frequency.

Table 2. Step-up operation for one cycle of output voltage at different frequencies.

Step-Up Output Frequency	Mode of Operation during Input Supply		Output Pulse Polarity	Mode of Operation	Switches Conducting
2 × f	Positive half cycle	P_1	Positive	Mode.1	S_1, S_2, S_7, and S_{10}
		N_1	Negative	Mode.3	S_1, S_3, S_6, and S_{11}
		P_2	Positive	Mode.1	S_1, S_2, S_7, and S_{10}
		N_2	Negative	Mode.3	S_1, S_3, S_6, and S_{11}
	Negative half cycle	P_3	Positive	Mode.4	S_{12}, S_9, and S_4
		N_3	Negative	Mode.2	S_{13}, S_8, and S_5
		P_4	Positive	Mode.4	S_{12}, S_9, and S_4
		N_4	Negative	Mode.2	S_{13}, S_8, and S_5
3 × f	Positive half cycle	P_1	Positive	Mode.1	S_1, S_2, S_7, and S_{10}
		N_1	Negative	Mode.3	S_1, S_3, S_6, and S_{11}
		P_2	Positive	Mode.1	S_1, S_2, S_7, and S_{10}
		N_2	Negative	Mode.3	S_1, S_3, S_6, and S_{11}
		P_3	Positive	Mode.1	S_1, S_2, S_7, and S_{10}
		N_3	Negative	Mode.3	S_1, S_3, S_6, and S_{11}
	Negative half cycle	P_4	Positive	Mode.4	S_{12}, S_9, and S_4
		N_4	Negative	Mode.2	S_{13}, S_8, and S_5
		P_5	Positive	Mode.4	S_{12}, S_9, and S_4
		N_5	Negative	Mode.2	S_{13}, S_8, and S_5
		P_6	Positive	Mode.4	S_{12}, S_9, and S_4
		N_6	Negative	Mode.2	S_{13}, S_8, and S_5

Similar way the procedure is repeated for other output frequencies. Where f is input supply frequency.

Mode 1:

The switches S_1, S_2, S_7, and S_{10} are forward biased in the positive half cycle of input voltage, as shown in Figure 7a. These are triggered at $\alpha = 0$ and conduct from $\omega t = \alpha$ to π for a resistive load (R). The path for the flow of current in the circuit is given by V_{Acph}-S_1-S_2-L-S_7-LOAD-S_{10}-V_{ACN}.

Mode 2:

In the negative half cycle, the switches S_{13}, S_8, and S_5 are switched on, as given in Figure 7b. These are conducted from $\omega t = \pi$ to 2π for resistive load. The path for the flow of current in the circuit is given by V_{Acph}-S_{13}-LOAD-S_8-L-S_5-V_{ACN}.

Mode3:

In the positive half cycle, switches S_1, S_3, S_6, and S_{11} are forward biased, as shown in Figure 7c. These are conducted from $\omega t = 2\ \pi$ to 3π for resistive load. The path for the flow of current in the circuit is given by V_{Acph}-S_3-L-S_6-LOAD-S_{11}-V_{ACN}.

Mode4:

In the negative half cycle, the switches S_{12}, S_9, and S_4 are turned on, as shown in Figure 7d. It is conducted from $\omega t = 3\pi$ to 4π for resistive load. The path for the flow of the current in the circuit is given by V_{Acph}-S_{12}-LOAD-S_9-L-S_4-V_{ACN}.

3. Parameter Design and Power Loss Analysis

3.1. Parameter Design Procedure

The parameter design of circuit components depends mainly on the type of capacitor, inductor, switching frequency, and duty ratio, as detailed in Reference [29], and as given in Equations (7)–(13).

Step 1: The maximum and minimum power are given by the following:

$$\begin{aligned} P_{0max} &= V_0 I_{0max} \\ P_{0min} &= V_0 I_{0min} \end{aligned} \tag{7}$$

Step 2: The load-resistance maximum and minimum values are calculated as follows:

$$\begin{aligned} R_{Lmin} &= \frac{V_0}{I_{0max}} \\ R_{Lmax} &= \frac{V_0}{I_{0min}} \end{aligned} \tag{8}$$

Step 3: The output voltage conversion gain of the converter is as follows:

$$\begin{aligned} M_{V_{DC}min} &= \frac{V_0}{V_{DCmax}} \\ M_{V_{DC}nom} &= \frac{V_0}{V_{DC}} \\ M_{V_{DC}max} &= \frac{V_0}{V_{DCmin}} \end{aligned} \tag{9}$$

Step 4: The duty ratio range is determined by the following equations:

$$\begin{aligned} d_{min} &= \frac{M_{VDCmin}}{\eta} \\ d_{nom} &= \frac{M_{VDCnom}}{\eta} \\ d_{max} &= \frac{M_{VDCmax}}{\eta} \end{aligned} \tag{10}$$

where η is the converter efficiency.

Equations (9)–(11) give the proper selection of the duty ratio, which is related to voltage conversion and efficiency.

Step 5: The minimum values of inductance are determined as follows:

$$L_{min} = \frac{R_{Lmax}(1 - d_{min})}{2f_s} \tag{11}$$

Capacitance value can be obtained as follows:

$$C_{min} = \frac{D_{max} V_0}{V_{cpp} R_{Lmax} f_s} \tag{12}$$

where, V_0 is the output voltage, D_{max} is the maximum duty ratio, f_s is the switching frequency, R_{Lmax} is the maximum load resistance, and V_{cpp} is the peak-to-peak value of the capacitor.

$$V_{cpp} = \frac{V_r}{2} \tag{13}$$

The ripple voltage (V_r) is 1% V_0.

The above expression shows the relation between the duty ratio, load, and inductance parameters. The calculated parameter values are listed in Table 3.

Table 3. Parameter specifications.

Parameter	DC–DC Converter	Inverter	Rectifier	AC Voltage Controller	Cyclo-Converter
Input voltage (V_{DC})	50	50	48 V	48 V	48 V
Output currents (I_0)	2 A	2 A	4.2 A	4.2 A	2 A
Output power (P_0)	60 W	150 W	150 W	150 W	150 W
Switching frequency (f)	10 kHz	10 kHz	50 Hz	50 Hz	25 Hz
Inductor (L)	3 mH	10 mH	3 mH	3 mH	3 mH
Capacitor I	600 µF	470 µF	470 µF	470 µF	470 µF

3.2. Power-Loss Analysis

The conduction and switching losses constitute the losses in the converters [30] and are given by Equations (14)–(17):

$$P_{loss} = P_{con} + P_{sw} \tag{14}$$

The conduction losses are determined as shown below:

$$P_{con} = \frac{1}{T}\int_0^T (R_{on} i_F + V_{Fo}) i_F dt \tag{15}$$

where i_F, V_{Fo}, R_{on}, and T are the current in the forward direction, forward voltage, on-state device resistance, and switching period, respectively.

The total switching losses are determined as follows:

$$P_{sw} = \frac{1}{n}\sum_{j=1}^{n}\left[E_{OFF_j}(i_F, V_{OFF}) + E_{ON_j}(i_F, V_{OFF})\right] \tag{16}$$

where E_{OFF} and E_{ON} are the energy dissipation during switching.

Therefore, efficiency can be determined as follows:

$$\eta = \frac{P_{out}}{P_{out} + P_{sw} + P_{con}} \tag{17}$$

3.3. Comparative Analysis

It is always better to perform a comparative analysis with the other counter parts to gain insight into and determine the superiority of the proposed converter topology. The comparison of the proposed UPC with the other recently proposed hybrid converters in terms of number of power semiconductor switches, reactive elements, and modes of operation is shown in Table 4. It is observed that the proposed UPC offers a greater number of operating modes in one converter, with nearly the same total-number-of-parts count. However, every converter has its own merits and demerits.

Table 4. Comparison of proposed UPC with other hybrid converters.

Name of the Components	Ref. [9]	Ref. [17]	Ref. [18]	Ref. [20]	Ref. [25]	Proposed
Switches	9	5	4	4	12	13
Diodes	0	2	1	1	0	0
Inductors	1 (coupled)	1	4	3	2-(Inductors), 1-(Coupled)	1
Capacitors	2	1	3	2	2	1
Modes of Operation	DC–AC and DC–DC	DC–AC and DC–DC	DC–AC and DC–DC	DC–AC and DC–DC	DC–DC, DC–AC, and AC–DC	DC–DC, DC–AC, AC–DC, AC–AC, and cyclo-converter

4. Results and Discussions

4.1. Simulation Results

Using the MATLAB/Simulink environment, simulations were run to analyze the performance of the proposed converter. The test was conducted in different modes of operation, such as DC–DC, DC–AC, AC–DC, AC–AC, and cyclo-converter configurations. The input voltage, duty cycle, and switching frequency were 50 V, 60%, and 10 kHz, respectively. The proposed UPC was tested in the DC–DC conversion with the buck mode of operation. The output voltage and current flow through the inductor are shown in Figure 8a,b. The proposed configuration is operated in boost and buck–boost modes. The corresponding output voltage and inductor current are depicted in Figure 8c–f, respectively. From Figure 8a,c,e, it is clear that the results are close to the theoretical values and verified with output voltage expressions given by Equations (1)–(3). In the inverter configuration, the input voltage is taken as 50 V, and the corresponding load voltage and FFT analysis are illustrated in Figure 9a,b. It is observed that the proposed configuration has 8.56%THD in inverter operation. The performance of the proposed configuration under different modes of operation, such as rectifier (AC–DC), AC voltage controller (AC–AC), and cyclo-converter operations, was tested; the input voltage of 48 Vmax was fed to the converter, as shown in Figure 10a. Figure 10b depicts load voltage in rectifier mode at a firing angle of 30°. For the AC voltage controller operation, the controlled output voltage with a firing angle of 90° is shown in Figure 10c. The performance of the proposed configuration in the cyclo-converter operation was verified at a firing angle of 0°, and the corresponding output voltage is illustrated in Figure 10d. These results confirmed that the proposed UPC could perform multiple operations in a single converter.

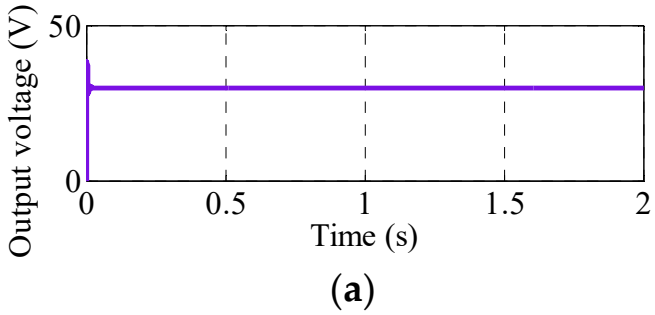


Figure 8. *Cont.*

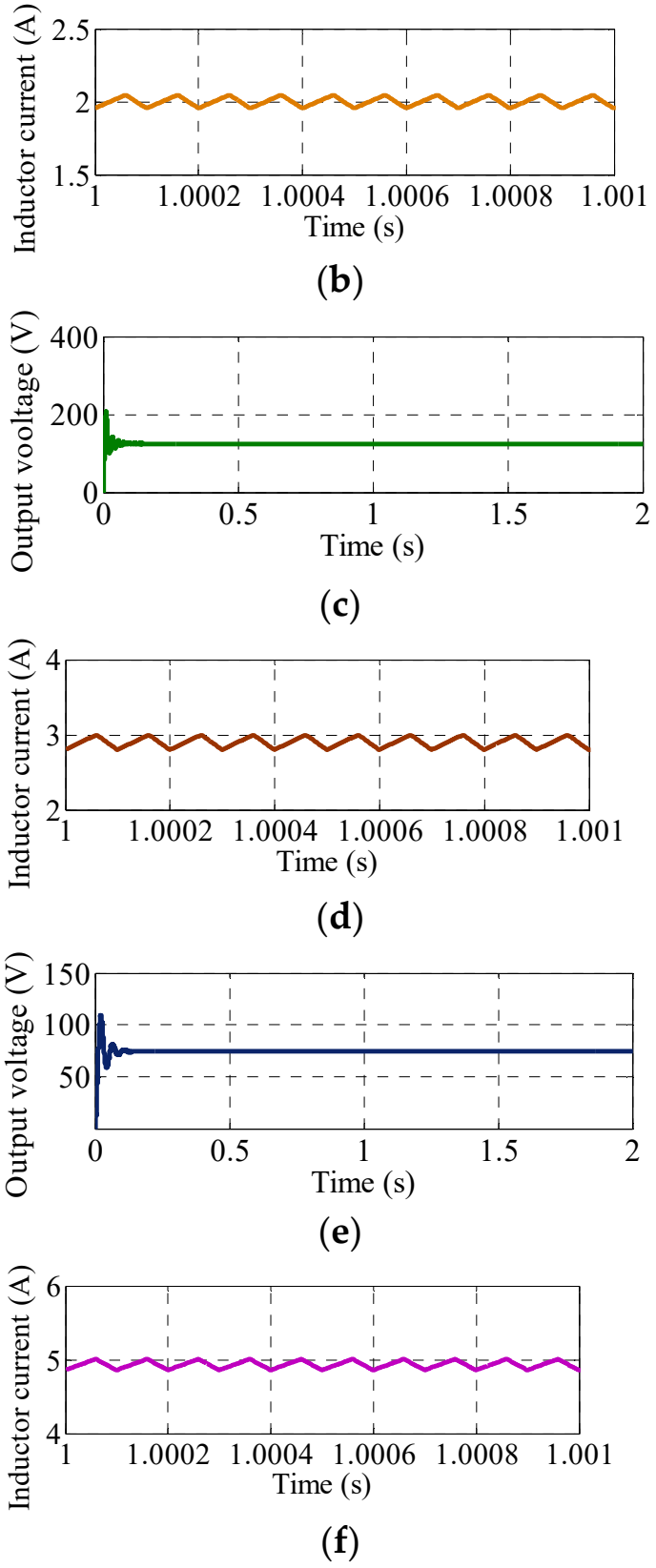


Figure 8. Simulation results of proposed UPC in DC–DC operation: (**a**) buck output voltage, (**b**) inductor current during buck operation, (**c**) boost output voltage, (**d**) inductor current during boost operation, (**e**) buck–boost output voltage, and (**f**) inductor current during buck–boost mode.

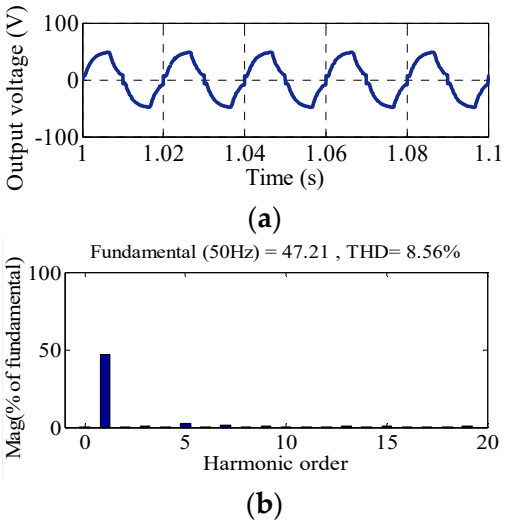


Figure 9. Simulation results of proposed UPC in inverter mode: (**a**) inverter output voltage and (**b**) FFT analysis.

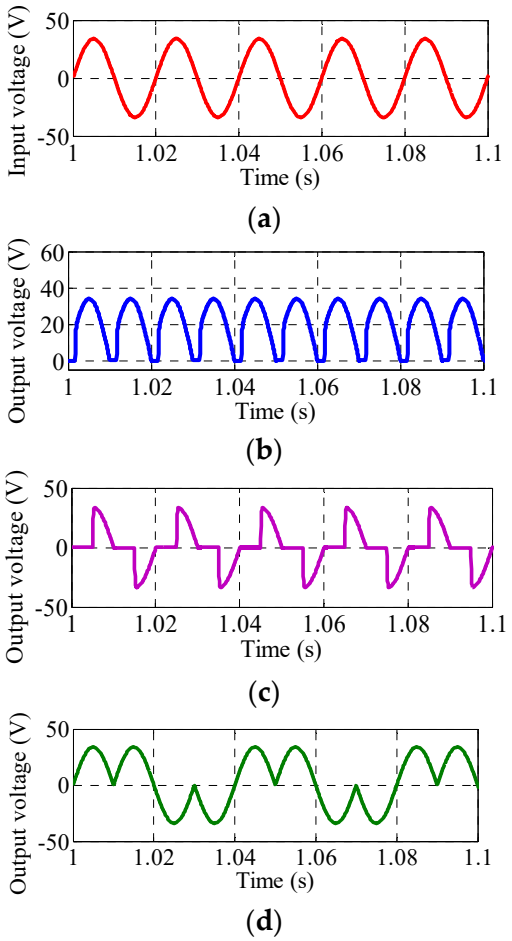


Figure 10. Simulation results of the proposed UPC in rectifier, AC voltage controller, and cyclo-converter mode: (**a**) input voltage, (**b**) rectifier output voltage, (**c**) AC voltage regulator output voltage, and (**d**) cyclo-converter output voltage.

4.2. Experimental Verification

A 100 W laboratory prototype was developed; to validate the low-power prototype, a circuit was developed in the laboratory to demonstrate the feasibility and benefits of the proposed UPC. It was tested under buck, boost, buck–boost, and inverter operations. In

DC–DC conversion, the test was performed with the input voltage of 50 V, duty cycle of D = 60%, inductor value of 3 mH, a capacitor value of 600 µF, and switching frequency of 10 kHz. The control module dSPACE1104 was used as a core controller for generating a controlling signal for active switches IGBTs (STGW30NC120HD). For the buck mode of operation, the experimental output voltage and current flow in the inductor are shown in Figure 11a,b respectively. Similarly, output voltage and inductor current in boost and buck–boost mode of operations are illustrated in Figure 11c–f, respectively. It can be observed that Figure 11a,c,e are close to both the theoretical and simulation results. Afterward, the proposed UPC was tested in an inverter configuration with an input voltage of 50 V. The corresponding output voltage and FFT analysis are depicted in Figure 12a,b, respectively. The proposed converter was also tested in rectifier, AC voltage controller, and cyclo-converter operations at the input voltage of 48 V. The corresponding input and output voltages are depicted in Figure 13a–d, respectively. The efficiency of the converter in the different modes of operation is shown in Figure 14a, and a power-loss analysis of the proposed converter in various operations is depicted in Figure 14b. Snapshots of the hardware experimentation on the UPC prototype circuit in the laboratory are illustrated in Figure 15.

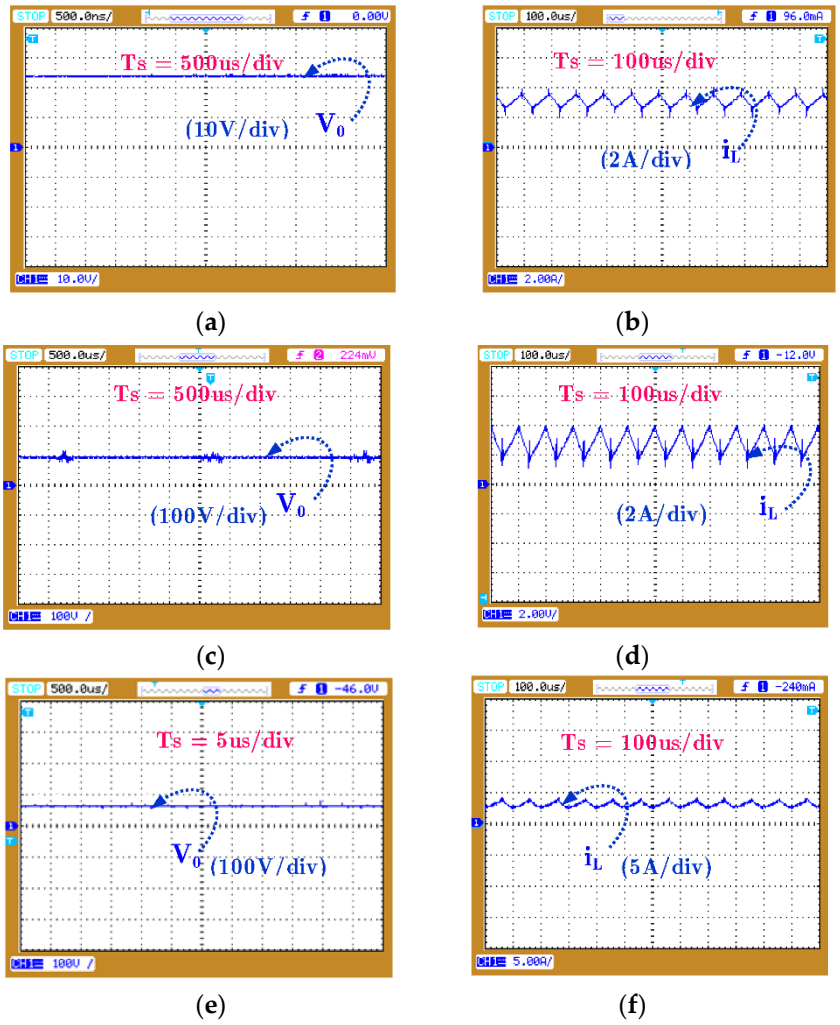
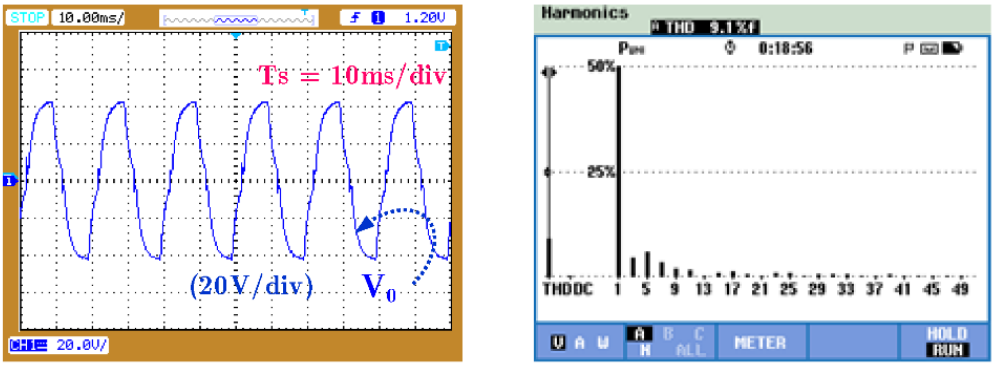
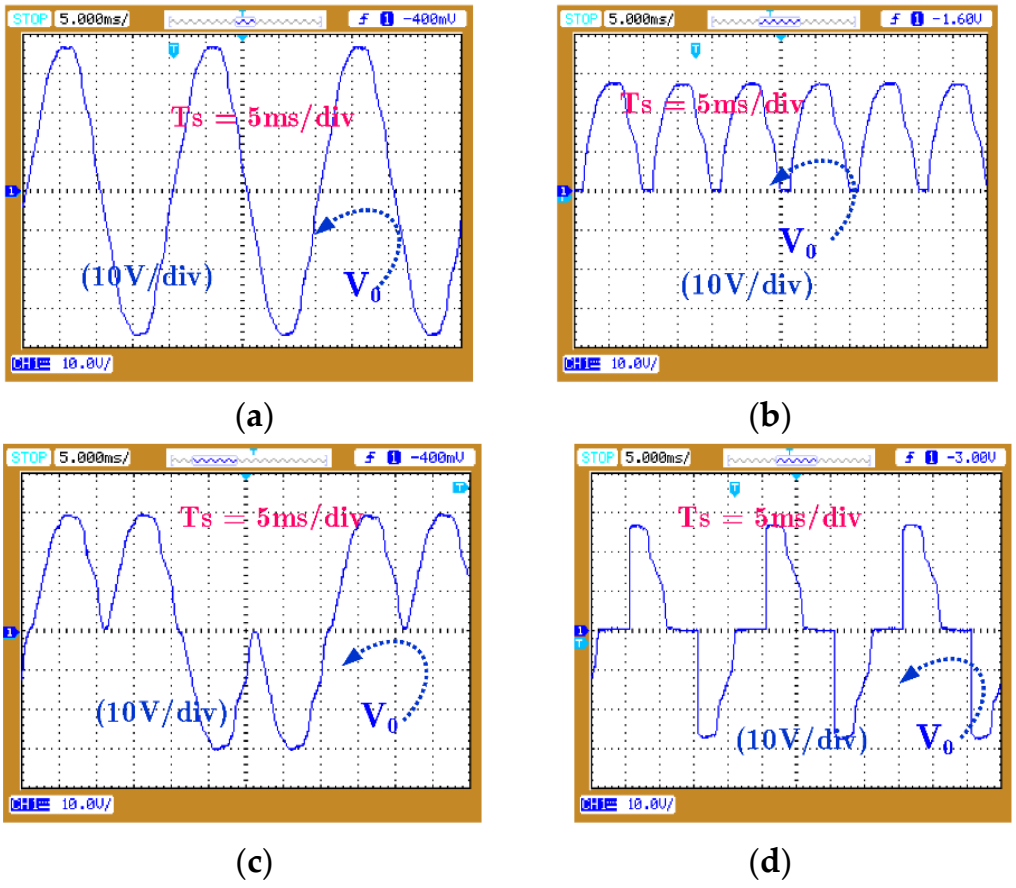


Figure 11. Experimental results of proposed UPC in DC–DC operation: (**a**) buck output voltage, (**b**) inductor current in buck operation, (**c**) boost output voltage, (**d**) inductor current in boost operation, (**e**) buck–boost output voltage, and (**f**) inductor current in buck–boost mode of operation.



(**a**) (**b**)

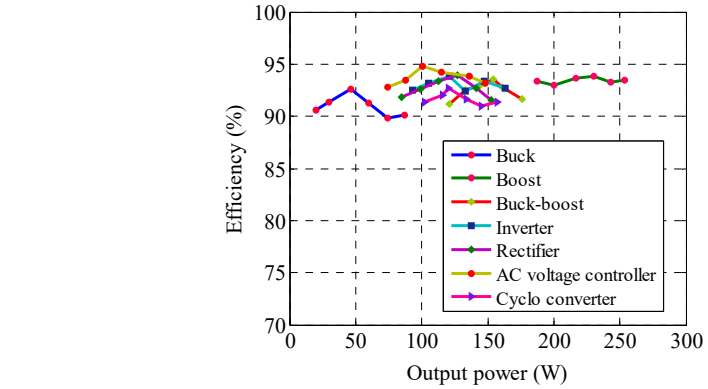
Figure 12. Experimental results of UPC in inverter operation: (**a**) output voltage and (**b**) FFT analysis.



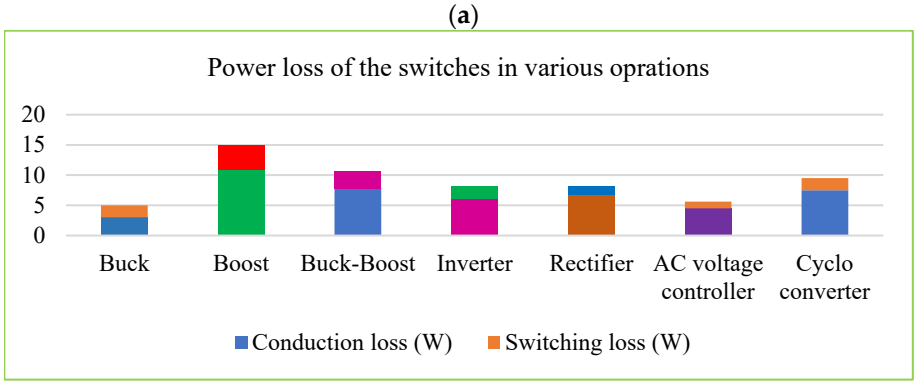
(**a**) (**b**)

(**c**) (**d**)

Figure 13. Experimental results of the proposed UPC in rectifier, AC voltage controller, and cyclo-converter mode: (**a**) input voltage, (**b**) rectifier output voltage, (**c**) AC voltage regulator output voltage, and (**d**) cyclo-converter output voltage.



(**a**)



(**b**)

Figure 14. (**a**) The proposed converter efficiency in the different operation modes and (**b**) power loss of the switches in various operations.

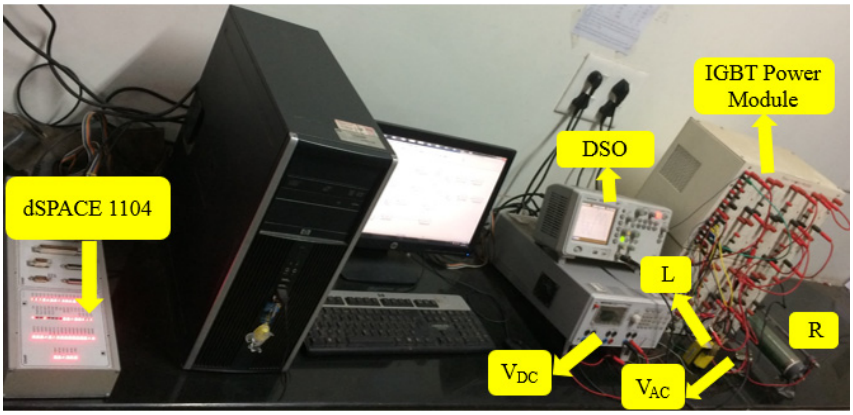


Figure 15. Snapshot of the hardware experimentation on the UPC prototype circuit in the laboratory.

5. Conclusions

In this paper, a new class of power converter called UPC is proposed for performing multiple operations in a single converter, such as DC–DC, DC–AC, AC–DC, and AC–AC (cyclo-converter and AC voltage converter) operations. The operating principle and different modes of operations were explained in detail. In DC–DC conversion, it can be performed as buck, boost, and buck–boost operations. Similarly, in DC–AC conversion, the proposed UPC gives a better %THD. Finally, the proposed converter operation and performance were validated with both simulation and experimental results.

Author Contributions: D.M., D.P. and R.S. designed the problem under study and performed the simulations and obtained the results; D.M., D.P. and R.S. wrote the paper, which was further reviewed by A.Y.A. and A.E.-S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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