New Figure-of-Merit Combining Semiconductor and Multi-Level Converter Properties

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ABSTRACT Figures-of-Merit (FOMs) are widely-used to compare power semiconductor materials and devices and to motivate research and development of new technology nodes. These material- and device-specific FOMs, however, fail to directly translate into quantifiable performance in a specific power electronics application. Here, we combine device performance with specific bridge-leg topologies to propose the extended FOM, or X-FOM, a Figure-of-Merit that quantifies bridge-leg performance in multi-level (ML) topologies and supports the quantitative comparison and optimization of topologies and power devices. To arrive at the proposed X-FOM, we revisit the fundamental scaling laws of the on-state resistance and output capacitance of power semiconductors to first propose a revised device-level semiconductor Figure-of-Merit (D-FOM). The D-FOM is then generalized to a multi-level topology with an arbitrary number of levels, output power, and input voltage, resulting in the X-FOM that quantitatively compares hard-switched semiconductor stage losses and filter stage requirements across different bridge-leg structures and numbers of levels, identifies the maximum achievable efficiency of the semiconductor stage, and determines the loss-optimal combination of semiconductor die area and switching frequency. To validate the new X-FOM and showcase its utility, we perform a case study on candidate bridge-leg structures for a three-phase 10 kW photovoltaic (PV) inverter, with the X-FOM showing that *(a)* the minimum hard-switching losses are an accurate approximation to predict the theoretically maximum achievable efficiency and relative performance between bridge-legs and *(b)* the 3-level bridge-leg outperforms the 2-level configuration, despite utilizing a SiC MOSFET with a lower D-FOM than in the 2-level case.

INDEX TERMS AC-DC power converters, DC-AC power converters, multilevel converters, power semiconductor devices, semiconductor device modeling, switched capacitor circuits.

I. INTRODUCTION

Figures-of-Merit (FOMs) are ubiquitous and powerful, and are used widely to compare candidate power semiconductor materials and realized devices. Material-based Figures-of-Merit (M-FOMs) compare the material properties that are critical to device operation, including critical electric field, electron mobility, and/or the thermal conductivity [1]–[5], and have driven the research, development, and recent commercialization of wide-bandgap (WBG) power semiconductors like Gallium Nitride (GaN) and Silicon Carbide (SiC). When a given M-FOM is combined with a particular device structure,

manufacturing process, and packaging technique (see Fig. 1(a)), higher-level device parameters – such as on-state resistance (R_{on}), equivalent output capacitance (C_{oss}), and gate charge (Q_g) – can be compared across power semiconductors as die area-independent device Figures-of-Merit, or D-FOMs [4]–[11], which are often used to compare technology generations and commercial devices across technology, manufacturer, and breakdown voltage in both academia and industry [12]. None of the proposed FOMs, however, translates directly to the performance of a power semiconductor bridge-leg in a particular power electronics application, a literature
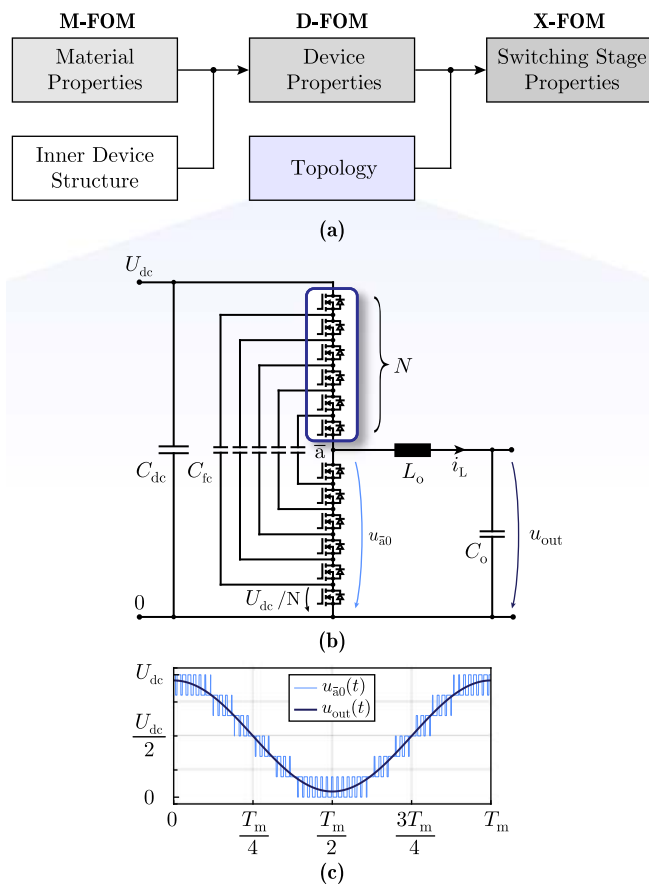
FIGURE 1. **(a) Comparison of FOMs, with the combination of material properties (M-FOM) and device structure leading to a device Figure-of-Merit (D-FOM), and the combination of device properties and topology leading to the application-specific Figure-of-Merit proposed here, the extended FOM, X-FOM. (b) Multi-level ("ML") bridge-leg with $N+1$ levels, with $2N$ devices per bridge-leg, each device withstanding U_{dc}/N, and (c), multi-level voltage waveform applied to the output filter inductor L_o.**

gap that leaves designers unable to compare the *combination* of devices and topologies to optimize bridge-leg performance in a particular application.

To address this shortcoming, we combine modern power semiconductor device properties with the increasingly-adopted multi-level bridge-leg configuration (Fig. 1(b)) to propose an *extended FOM* (X-FOM) that compares the performance of multi-level bridge legs across input voltage, power device selection, number of levels, switching frequency, and a host of other parameters to quantitatively compare performance among different configurations and predict the optimal bridge-leg efficiency. Compared to a conventional 2-level bridge-leg, multi-level converters (Fig. 1(b)) can utilize power semiconductors with lower voltage ratings for lower on-resistance [13], demonstrate increased power density [14], [15] and efficiency [16], [17]. In flying capacitor multi-level converters (FCML [18]), in particular, the filter size can also be reduced as more levels are added due to the lower volt-seconds applied to the output inductor [19] (Fig. 1(c)). Despite the demonstrated promise of these multi-level

converters, though, there does not exist a straightforward method to optimally select the power semiconductor alongside the correct number of levels in a multi-level topology. Here, we develop the fundamental understanding of the advantages of using a multi-level power semiconductor stage – a quantification summarized in the proposed X-FOM.

We first revisit the voltage scaling laws of on-state resistance and output capacitance across power semiconductor technologies (Section II) to arrive at a device-level Figures-of-Merit (D-FOM) for a hard-switching bridge-leg that considers the theoretical *minimum* hard-switching losses in the semiconductor devices (Section III). This improved D-FOM explicitly defines the maximum achievable efficiency of a bridge-leg with application-specific conditions. With these minimum losses defined, we then generalize the loss calculation and die area optimization to an arbitrary number of levels in a multi-level bridge leg (see Fig. 2) to arrive at the proposed extended FOM, or X-FOM (Section IV), which is a direct and straightforward comparison between various combinations of bridge-leg structure and power semiconductor selection. The new X-FOM is applied to a three-phase 10 kW photovoltaic (PV) inverter in a case study (Section V) to validate the minimum loss approximation and illustrate the utility of this new Figure-of-Merit. With this X-FOM verified as an accurate predictor of the maximum achievable efficiency for a given bridge-leg, we see that the X-FOM can be used directly to compare and motivate both device and topological improvements, finally bringing device considerations to the end power electronics application. Section VI summarizes the main findings and, in light of this new X-FOM, highlights promising research directions on both power devices and topologies.

II. SEMICONDUCTOR DEVICE VOLTAGE SCALINGS

To compare across topologies, we must first lay the foundation of understanding how semiconductor performance scales when a high-voltage switch is replaced with lower-voltage counterparts (e.g., when increasing the number of levels in a multi-level configuration, where each semiconductor must block U_{dc}/N, U_{dc} being the DC-link voltage and N number of levels minus one, cf., Fig. 1(b)). In this section, we consider this voltage scaling in the context of the two dominant power semiconductor loss mechanisms: conduction losses and switching losses.

A. CONDUCTION LOSSES
A first step towards calculating the maximum efficiency of a converter is to only consider the conduction losses of the power semiconductors. For the topology depicted in Fig. 1(b), the conduction losses are given by

$$P_{cond} = R_{eq}I_{rms}^2, \qquad (1)$$

where R_{eq} is the total on-state resistance of the simultaneously-conducting devices of the bridge-leg (i.e. NR_{on}, where there are $2N$ devices per bridge-leg and R_{on} is the on-state resistance of one switch), and I_{rms} is the RMS current through the inductor L_o. I_{rms} is given by the
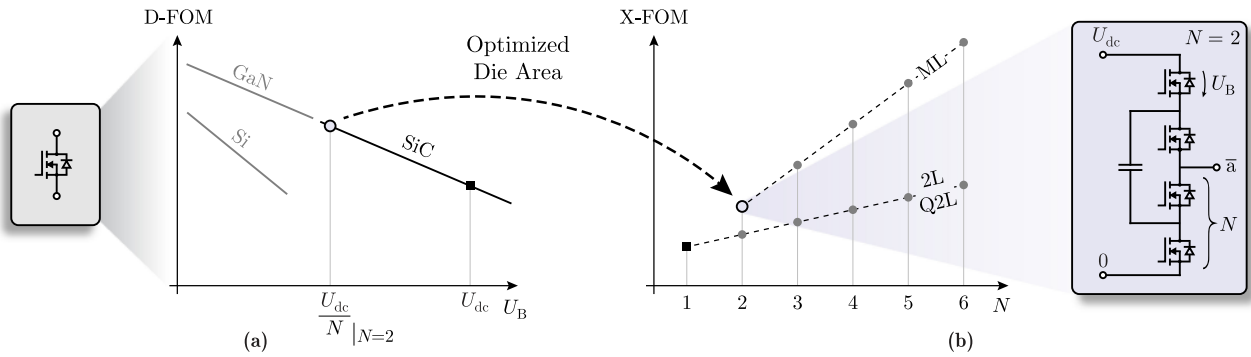
FIGURE 2. Relationship between the (a) device Figure-of-Merit, D-FOM, which depends only on semiconductor properties, and (b), the extended Figure-of-Merit, X-FOM, which combines the properties of both the semiconductor and converter structure, including the DC-link voltage U_{dc}, the RMS output current of the bridge-leg, and the switching frequency. The developed mapping between the D-FOM and X-FOM assumes a semiconductor die area that is optimized to minimize the hard-switched semiconductor losses of the bridge-leg.

power and voltage specifications of the application, and assuming L_o is selected for a relatively small current ripple, conduction losses can only be decreased by reducing R_{eq}. This assumption is not reliant on the particular selection of L_o – even if the ripple RMS current ($I_{rms,HF}$) is, e.g., 30% of the fundamental RMS, the conduction losses change by only 9% ($I_{rms}^2 + I_{rms,HF}^2 = I_{rms}^2 + (0.3I_{rms})^2 = 1.09I_{rms}$), as shown in Fig. 4(a–b).

To analyze the conduction loss difference between a single high-voltage device and several series-connected lower-voltage devices (Fig. 1(b)), we must first consider the voltage dependence of the on-state resistance, R_{on}, as a function of the blocking voltage of a device, U_B. The on-state resistance can be written as the area-specific on-resistance (R'_{on}), and further rewritten with a technology-specific constant (k_R) and voltage-scaling factor (α_R), as:

$$R_{on}(U_B) = \frac{R'_{on}(U_B)}{A_{die}} = \frac{k_R U_B^{\alpha_R}}{A_{die}} \approx \frac{k_R U_B^2}{A_{die}}, \qquad (2)$$

where A_{die} is the die area. For vertical devices, and only considering a very basic model, i.e., the resistance contributed by a one-dimensional (1-D) ideal drift region, α_R is theoretically equal to 2, as derived in Appendix A and given widely (e.g., in [4]).

This approximation for α_R is given as a first step to facilitate an understanding of the scaling laws, and, in the following, the assumption of $\alpha_R \approx 2$ for applicable device technologies for hard-switched converters, i.e., Si MOSFETs, SiC MOSFETs, and GaN-on-Si HEMTs, will be examined. Fig. 3 shows a survey of commercially available state-of-the-art devices and Table 1 gives the empirically-fit exponential coefficients and constants for each technology.

For Si MOSFETs, the empirical fitting agrees with the theoretical $R'_{on} \propto U_B^{2.5}$ scaling found when considering the dependence of electric field on doping concentration [20]. For SiC MOSFETs and GaN-on-Si HEMTs, the voltage scaling terms are less than the $\alpha_R \approx 2$ predicted by the simple model (see Appendix A for a discussion of the root causes of the respective voltage scalings) but agree with previously-derived

empirical fits of α_R [23]. These technology-specific scaling factors have far-reaching impacts on the desirability and design of multi-level topologies, as they define the reduction in individual R_{on} with lower blocking voltage. With the voltage scaling of specific on-resistance – and therefore conduction losses – well-defined, we repeat the process to determine the dependence of switching losses on device blocking voltage.

Remark: One common application where it is sufficient to only evaluate the R_{on} scaling is in Triangular Current Mode (TCM) operation [25]–[27], which in contrast to CCM that features one hard-switching and one soft-switching transition per switching period (cf., Fig. 4(a), (b)), features two soft-switching transitions per switching period. Hence, at a cost of 33% higher conduction losses (RMS currents for TCM are $2/\sqrt{3}$ higher relative to CCM), TCM eliminates hard-switching losses, where typically the hard-switching losses are an order of magnitude larger than in the soft-switched transitions [28]–[32].

B. SWITCHING LOSSES

To accurately model the minimum hard-switching losses, we first reexamine a single hard-switching transition in a bridge-leg to find the correct linear-equivalent capacitance model and losses from hard-switching. To derive these scaling laws, we reiterate that the $V - I$ overlap period is assumed to be small and therefore only capacitive switching losses occur, an assumption that is later relaxed when we compare this model to experimentally-measured switching losses. Nonetheless, this assumption is reasonable with the operating conditions considered here for hard-switched high-efficiency applications, where switched currents are typically much lower than rated currents [17], [33], and fast switching transitions are desired as well as enabled by WBG devices.

These capacitive losses, which occur under zero-current switching (ZCS), represent the minimum hard-switching losses, the desired quantity to assess the maximum achievable efficiency with the various bridge-leg configurations. A single hard-switching transition is shown in Fig. 4(c), (d), where the parasitic output capacitor (C_{oss}) of T_1 starts charged to U_{dc} in
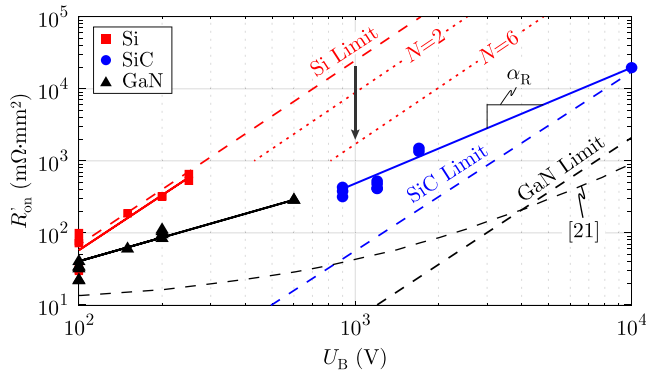
FIGURE 3. Specific on-state resistance R'_{on} at 25 °C junction temperature (T_j) for a selection of commercial power semiconductors. The Si, SiC and GaN theoretical limits from [20]–[22] are shown (dashed) together with the power function fits ($k_R \cdot U_B^{\alpha_R}$) given in Table 1. The Si scaling with increased number of series-connected devices ($N = 2$ and $N = 6$) toward multi-level converters use a constant (individual) die area scaling.

TABLE 1. Scaling Factors α_R and k_R for R'_{on}. k_R is Given Such that R'_{on} is in m$\Omega \cdot$ mm² and is Fit at $T_j = 25$ °C

	Si	SiC	GaN
k_R	$4.8 \cdot 10^{-4}$	$7.2 \cdot 10^{-3}$	0.26
α_R	2.5	1.6	1.1

the initial state (Fig. 4(c), $\overline{T}_1$ conducting) and the transition ends with T_1 conducting and the C_{oss} of $\overline{T}_1$ charged to U_{dc} (Fig. 4(d)) by the supply. We assume that the two switches are identical and the inductor current remains constant during the switching transition. The minimum hard-switching energy dissipated per cycle (E_{sw}) is given as [24]:

$$E_{sw} = Q_{oss}(U_{dc})U_{dc} = C_{oss,Q}(U_{dc})U_{dc}^2 \qquad (3)$$

where $C_{oss,Q}(U_{dc})$ is the voltage-dependent charge-equivalent output capacitance [24], [34]. The losses in (3) are equal to the ZCS losses, and are the minimum hard-switching losses where the $V - I$ overlap losses [23] don't exist due to zero load current. These minimum losses match very precisely with the measurements presented in Section V and with reported results in prior literature [31], [32].

Therefore, as a first step, the hard-switching losses are written as:

$$P_{sw} = Q_{oss}(U_{dc})U_{dc}f_{sw} = C_{oss,Q}(U_{dc})U_{dc}^2 f_{sw}, \qquad (4)$$

where f_{sw} is the switching frequency and $C_{oss,Q}(U_{dc})$ is the charge-equivalent output capacitance evaluated at U_{dc}.

Similarly to the derivation for the relationship between R_{on} and the blocking voltage of the device, U_B, we desire a voltage-scaling for $C_{oss,Q}$. This charge-equivalent capacitance can be written as the area-specific charge-equivalent capacitance ($C'_{oss,Q}$), and further rewritten with a technology-specific constant (k_C) and voltage-scaling factor (α_C) for this capacitance, as:

$$C_{oss,Q}(U_B) = C'_{oss,Q}(U_B)A_{die} = k_C U_B^{\alpha_C} A_{die} \approx k_C U_B^{-1} A_{die}. \qquad (5)$$
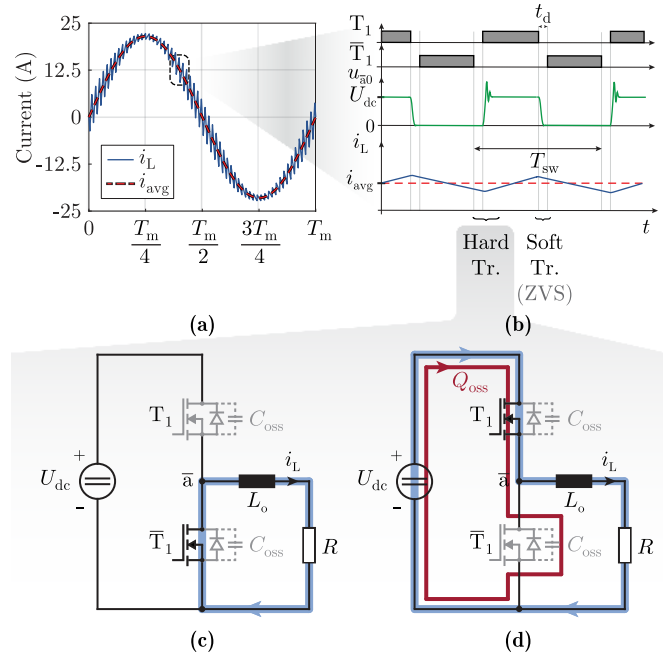

FIGURE 4. (a) Continuous conduction mode (CCM) simulated waveforms, where i_L is the inductor current and i_{avg} is the filtered output current. (b) Detailed transition waveforms for a switching period (T_{sw}), where t_d denotes the deadtime. (c) Start of the hard-switched transition, and (d), end of the hard-switched transition. During the switch transition, C_{dc} (modelled as a voltage source) supplies a charge of Q_{oss} at voltage U_{dc}, and this supplied energy equals the dissipated energy of $Q_{oss}U_{dc}$ [24].

For vertical devices, and only considering the one-dimensional (1-D) ideal drift region, $\alpha_C = -1$, as derived in Appendix A. This capacitance scaling is typically not considered in deriving voltage-scaling laws for semiconductors, but, as we show in the following sections, is critical in determining a voltage-specific X-FOM for any type of hard-switched converter. This α_C approximation is again used to develop an intuition of the scaling laws before finding technology-specific α_C values for candidate devices.

To relate the assumption of $\alpha_C \approx -1$ to the actual device characteristics, we again survey commercially-available devices, this time for their respective $C'_{oss,Q}$ values across blocking voltage, U_B. This survey is shown in Fig. 5 with fittings in Table 2, where we find that, for all candidate technologies, the approximation of $\alpha_C \approx -1$ is relatively close to the empirical fittings. Si has the largest voltage-dependence of the available technologies, with $\alpha_C = -1.6$, and GaN has the flattest $C'_{oss,Q}$ characteristic with voltage at $\alpha_C = -0.7$.

With a reduction in device voltage rating, then – for example, when moving from a 2-level to a multi-level configuration – the on-resistance decreases (Fig. 3), reducing the conduction losses, but the output capacitance increases (Fig. 5), resulting in larger switching losses. The existing of an optimal semiconductor area to tradeoff switching losses and conduction losses is well-known; observing these counteracting scaling laws with N, however, we also recognize that an optimal *total* semiconductor die area for a given number of
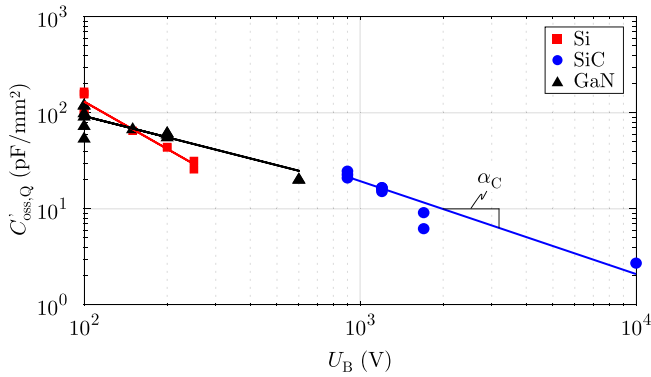
FIGURE 5. Specific charge-equivalent output capacitance $C'_{\mathrm{oss,Q}}$ for a selection of commercially-available power devices. The power function fits ($k_{\mathrm{C}} \cdot U_{\mathrm{B}}^{\alpha_{\mathrm{C}}}$) are given in Table 2.

TABLE 2. Scaling Factor α_{C} and k_{C} for $C'_{\mathrm{oss,Q}}$. k_{C} is Given Such That $C'_{\mathrm{oss,Q}}$ is in $\mathrm{pF} \cdot \mathrm{mm}^{-2}$

	Si	SiC	GaN
k_{C}	$2.4 \cdot 10^5$	$1.6 \cdot 10^4$	$2.7 \cdot 10^3$
α_{C}	-1.6	-1.0	-0.7

levels must exist. In the next section, we derive the optimal die area and minimum semiconductor losses for a two-level bridge leg before subsequently generalizing these findings to a multi-level configuration in Section IV.

III. OPTIMAL POWER SEMICONDUCTOR LOSSES FOR TWO-LEVEL BRIDGE-LEGS

For a 2-level bridge-leg (like in Fig. 1(b) with $N = 1$) with a DC input voltage U_{dc}, a filter inductor output current I_{rms}, and a switching frequency $f_{\mathrm{sw}}|_{2\mathrm{L}}$, the losses in the bridge-leg can be calculated as [10], [35]:

$$P_{\mathrm{semi}} = I_{\mathrm{rms}}^2 \frac{R'_{\mathrm{on}}(U_{\mathrm{dc}})}{A_{\mathrm{die}}} + C'_{\mathrm{oss,Q}}(U_{\mathrm{dc}})U_{\mathrm{dc}}^2 f_{\mathrm{sw}}|_{2\mathrm{L}} A_{\mathrm{die}}, \quad (6)$$

where we observe that an increase of die area (A_{die}) reduces conduction losses but increases the switching losses, as shown in Fig. 6. Naturally, this leads to a loss-minimizing ($\frac{\mathrm{d}P_{\mathrm{semi}}}{\mathrm{d}A_{\mathrm{die}}} = 0$), optimal total bridge-leg semiconductor area of:

$$A_{\mathrm{die,opt,tot}}\big|_{2\mathrm{L}} = 2\frac{I_{\mathrm{rms}}}{U_{\mathrm{dc}}}\sqrt{\frac{R'_{\mathrm{on}}(U_{\mathrm{dc}})}{C'_{\mathrm{oss,Q}}(U_{\mathrm{dc}})f_{\mathrm{sw}}|_{2\mathrm{L}}}} \quad (7)$$

and the minimized semiconductor losses in the 2-level bridge-leg of:

$$P_{\mathrm{semi,min}}\big|_{2\mathrm{L}} = 2I_{\mathrm{rms}}U_{\mathrm{dc}}\sqrt{f_{\mathrm{sw}}|_{2\mathrm{L}}R'_{\mathrm{on}}(U_{\mathrm{dc}})C'_{\mathrm{oss,Q}}(U_{\mathrm{dc}})}, \quad (8)$$

both of which are shown under normalized conditions in Fig. 6. Before introducing scaling to these loss-optimized conditions with the number of levels and/or individual device blocking voltage, three observations from this simple derivation merit discussion.
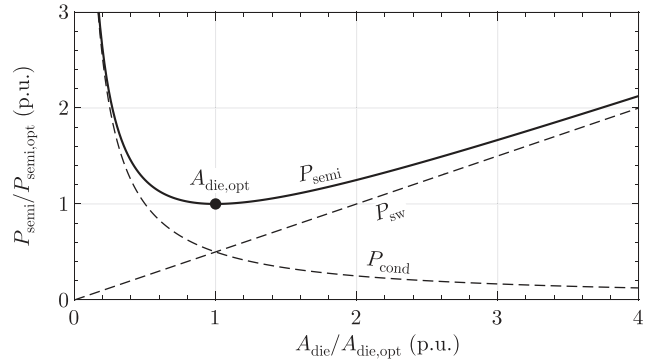
FIGURE 6. 2-level loss-minimized optimal semiconductor die area and minimum bridge-leg losses (considering only semiconductor losses), from (7) and (8), for an arbitrary f_{sw}.

- *Effect of f_{sw} on $P_{\mathrm{semi,min}}$*: $P_{\mathrm{semi,min}}$ depends on $\sqrt{f_{\mathrm{sw}}}$. Hence, if the desired f_{sw} is doubled, the optimal losses will increase by 41% and the optimal die area will decrease by 30%.
- *Effect of A_{die} on $P_{\mathrm{semi,min}}$*: $P_{\mathrm{semi,min}}$ features a rather flat curve as a function of A_{die} around $A_{\mathrm{die,opt}}$, as seen in Fig. 6. If, e.g., the selected die area is $A_{\mathrm{die}} = 2 \times A_{\mathrm{die,opt}}$, the bridge-leg losses only increase by 25%. With a $3\times$ larger A_{die} than $A_{\mathrm{die,opt}}$, losses increase by 67%.
- *Optimal number of parallel devices from $A_{\mathrm{die,opt}}$*: The loss-optimal number of parallel *devices* rather than the loss-optimal device *area* can be simply derived from (7) by substituting the absolute values (R_{on}, $C_{\mathrm{oss,Q}}$) for the specific values (R'_{on}, $C'_{\mathrm{oss,Q}}$) with Eqns. (2) and (5). With the die area typically not publicly-available, this substitution allows the designer to select the optimal device number from only absolute, datasheet-provided values.

Lastly, we see that the minimum achievable losses of the bridge-leg are influenced through $R'_{\mathrm{on}}C'_{\mathrm{oss,Q}}$ in (8). For a given blocking voltage requirement, a "better" semiconductor would lower R'_{on} and/or $C'_{\mathrm{oss,Q}}$, and we see the opportunity to define a device-level Figure-of-Merit as:

$$\text{D-FOM}(U_{\mathrm{B}}) = \frac{1}{\sqrt{R'_{\mathrm{on}}(U_{\mathrm{B}})C'_{\mathrm{oss,Q}}(U_{\mathrm{B}})}}. \quad (9)$$

This D-FOM does not require knowledge of the die area of the device, as $R'_{\mathrm{on}}C'_{\mathrm{oss,Q}} = R_{\mathrm{on}}C_{\mathrm{oss,Q}}$, and the D-FOM for a given semiconductor therefore can be determined from non-proprietary datasheet parameters. Similar device FOMs that depend on R'_{on} and the differential C'_{oss} [6] and energy-equivalent output capacitance $C'_{\mathrm{oss,E}}$ [10], [36], [37] have been reported, but the $C_{\mathrm{oss,Q}}$ dependency proposed here is the correct metric to determine the *minimum* hard-switching losses of a half-bridge. Finally, we can rewrite (8) compactly as:

$$P_{\mathrm{semi,min}}\big|_{2\mathrm{L}} = \frac{2I_{\mathrm{rms}}U_{\mathrm{dc}}\sqrt{f_{\mathrm{sw}}|_{2\mathrm{L}}}}{\text{D-FOM}|_{2\mathrm{L}}}. \quad (10)$$

D-FOM OF COMMERCIAL DEVICES

With the introduction of the D-FOM and its influence on the losses, we numerically compare the D-FOM of commercial semiconductors in Fig. 7.

Now, to understand the influence of the blocking voltage requirement on the D-FOM, and therefore, on the optimal area and minimum bridge-leg losses, we define a voltage-scaling parameter $\alpha_{\text{D-FOM}}$ (from the R'_{on} and $C'_{\text{oss,Q}}$ power function fits with respect to the blocking voltage U_{B} (2) and (5)):

$$\alpha_{\text{D-FOM}} = -\frac{(\alpha_{\text{R}} + \alpha_{\text{C}})}{2} \approx -0.5. \quad (11)$$

Using $\alpha_{\text{D-FOM}}$, we can rewrite the D-FOM as:

$$\text{D-FOM}(U_{\text{B}}) = \frac{1}{\sqrt{R'_{\text{on}}(U_{\text{B}})C'_{\text{oss,Q}}(U_{\text{B}})}} = \frac{1}{\sqrt{k_{\text{R}}k_{\text{C}}}}\frac{1}{U_{\text{B}}^{-\alpha_{\text{D-FOM}}}}$$

$$\approx \frac{1}{\sqrt{k_{\text{R}}k_{\text{C}}}}\frac{1}{\sqrt{U_{\text{B}}}} \quad (12)$$

The technology-specific voltage scaling factors $\alpha_{\text{D-FOM}}$ are given in Table 3. This factor describes the scaling of performance of different semiconductor technologies as a function of blocking voltage, where the higher the absolute value of $\alpha_{\text{D-FOM}}$, the higher the D-FOM gain of reducing the blocking voltage of the switches, as shown in Fig. 7. For every material, the power factor of on-state resistance voltage dependence is larger than the output capacitance factor (compare Table 1 to Table 2), resulting in higher D-FOMs for lower blocking voltages in the same device class. For instance, Silicon devices, with $\alpha_{\text{D-FOM}} = -0.5$, feature a larger benefit of reducing the blocking voltage of each device than SiC or GaN devices, which feature $\alpha_{\text{D-FOM}} = -0.3$ and $\alpha_{\text{D-FOM}} = -0.2$, respectively.

Using the voltage-scaling approximations, (8) can instead be rewritten as:

$$P_{\text{semi,min}}\big|_{2\text{L}} \approx 2I_{\text{rms}}U_{\text{dc}}\sqrt{U_{\text{B}}}\sqrt{f_{\text{sw}}|_{2\text{L}}}\sqrt{k_{\text{R}}k_{\text{C}}} \quad (13)$$

We see that a reduction of semiconductor blocking voltage (U_{B}) would straightforwardly result in a higher semiconductor D-FOM and therefore lower losses in a 2-level bridge-leg (cf., Eq. (13)). However, U_{dc} is typically specified for a given application – not a degree of freedom – so alternative bridge-leg topologies are required to utilize the improved D-FOM of lower-voltage devices for a given U_{dc}. This motivates the exploration of multi-level converters, where we seek to quantify how and if the superior properties of lower-voltage semiconductors, as indicated in (12) and (13), together with the topology change, can achieve higher performance.

IV. MULTI-LEVEL BRIDGE-LEG GENERALIZATION

When replacing a 2L bridge leg with a multi-level (ML) configuration, the following characteristics are obtained:
1) A series connection of N devices, where each device must block U_{dc}/N,
2) An increase of the effective switching frequency at the output node ($\bar{\text{a}}$ in Fig. 1(b)): for an $(N + 1)$-level ML

converter, the effective switching frequency at the output node is

$$f_{\text{eff}} = N f_{\text{sw}}|_{\text{ML}}, \quad (14)$$

where $f_{\text{sw}}|_{\text{ML}}$ is the switching frequency of the individual devices.
3) Smaller voltage steps at the output node $\bar{\text{a}}$: as shown in Fig. 1(b), there is a multi-level $(N + 1)$ output voltage waveform, reducing the voltage steps across the filter inductor in a switch cycle to only U_{dc}/N.

Note again that the ML is a generalization of a 2L case, where for the 2L case, $N = 1$.

To directly compare the ML bridge-leg to a 2L counterpart, we constrain the volt-seconds applied to the filter inductor to be constant (this constraint is later relaxed in Section V-B). By fixing the volt-seconds applied to the filter inductor, the current ripple term, $L_{\text{o}}\Delta i_{\text{L}}$ is also fixed between the 2L and ML topologies. In the 2L case, the voltage-time product is:

$$L_{\text{o}}\Delta i_{\text{L}} = \frac{U_{\text{dc}}}{4 f_{\text{sw}}|_{2\text{L}}}, \quad (15)$$

where Δi_{L} is the peak-to-peak current ripple. For the two advantages of the ML topology given above, however, the ripple in the ML case is reduced by:

$$L_{\text{o}}\Delta i_{\text{L}} = \frac{\left(\dfrac{U_{\text{dc}}}{N}\right)}{4\left(N f_{\text{sw}}|_{\text{ML}}\right)} = \frac{U_{\text{dc}}}{4N^2 f_{\text{sw}}|_{\text{ML}}} \Rightarrow L_{\text{o}}\Delta i_{\text{L}} \propto \frac{1}{N^2}, \quad (16)$$

where $f_{\text{sw}}|_{\text{ML}}$ is the switching frequency of a single device in the multi-level bridge-leg (and not the effective switching frequency f_{eff}). Therefore, for the same $L_{\text{o}}\Delta i_{\text{L}}$, the switching frequency in the ML topology can be reduced by N^2 as:

$$f_{\text{sw}}|_{\text{ML}} = \frac{f_{\text{sw}}|_{2\text{L}}}{N^2}. \quad (17)$$

For the general case, the bridge-leg losses in the ML topology are:

$$P_{\text{semi}} = N I_{\text{rms}}^2 \frac{R'_{\text{on}}(U_{\text{dc}}/N)}{A_{\text{die}}} + N C'_{\text{oss,Q}}(U_{\text{dc}}/N)\left(\frac{U_{\text{dc}}}{N}\right)^2 f_{\text{sw}}|_{\text{ML}} A_{\text{die}} \quad (18)$$

where the modeling of the switching losses for a multi-level bridge-leg is discussed in detail in Appendix C. When we consider the switching frequency reduction for a fair bridge-leg comparison, the loss-minimized losses become:

$$P_{\text{semi,min}}\big|_{\text{ML}} = \frac{2I_{\text{rms}}U_{\text{dc}}\sqrt{f_{\text{sw}}|_{\text{ML}}}}{\text{D-FOM}\left(\dfrac{U_{\text{dc}}}{N}\right)} = \frac{2I_{\text{rms}}U_{\text{dc}}\sqrt{f_{\text{sw}}|_{2\text{L}}}}{\underbrace{N \cdot \text{D-FOM}\left(\dfrac{U_{\text{dc}}}{N}\right)}_{\text{X-FOM}(U_{\text{dc}},N)}}, \quad (19)$$

where the final step of this equation substitutes (17) and therefore applies the assumption that a constant volt-second product is applied to the filter inductor. This loss-minimized
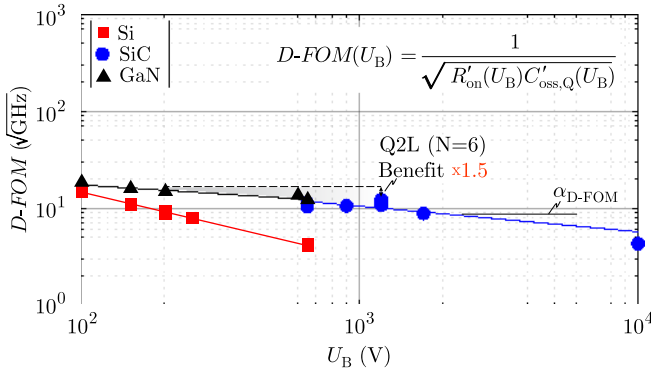
FIGURE 7. The device Figure-of-Merit D-FOM for a survey of commercially available power semiconductors plotted over their blocking voltage, where the $C_{oss,Q}$ is calculated for two-thirds of the rated voltage, and the R_{on} is the typical value at 25 °C. For the Quasi 2-Level (Q2L) operation of bridge-legs, refer to Appx. B.

TABLE 3. Scaling Factor $\alpha_{D\text{-}FOM}$ for D-FOM for Commercially Available Power Semiconductors

	Si	SiC	GaN
$\alpha_{D\text{-}FOM}$	-0.5	-0.3	-0.2

bridge-leg total semiconductor area is:

$$A_{die,opt,tot}\big|_{ML} = 2\frac{N^2 I_{rms}}{U_{dc}}\sqrt{\frac{R'_{on}(U_{dc}/N)}{C'_{oss,Q}(U_{dc}/N)\,f_{sw}\big|_{ML}}}$$

$$\approx N^{1.5} A_{die,opt,tot}\big|_{2L}, \tag{20}$$

where the approximations of (2) and (5) and the constant volt-second assumption are applied to reach the final equation. Keeping these same assumptions, and following the same process as in the previous derivations, we find:

$$P_{semi,min}\big|_{ML} \approx \frac{P_{semi,min}\big|_{2L}}{N^{1.5}} \tag{21}$$

and for the multi-level converter Figure-of-Merit:

$$X\text{-}FOM(U_{dc}, N) = N \cdot D\text{-}FOM\left(\frac{U_{dc}}{N}\right)$$

$$= \frac{N}{\sqrt{R'_{on}\left(\frac{U_{dc}}{N}\right)C'_{oss,Q}\left(\frac{U_{dc}}{N}\right)}}$$

$$= N^{(1-\alpha_{D\text{-}FOM})} \cdot D\text{-}FOM(U_{dc})$$

$$\approx N^{1.5} \cdot D\text{-}FOM(U_{dc}). \tag{22}$$

Relative to the 2-level benchmark, and using the same output filter and applied volt-seconds, the multi-level topology enables a loss reduction of $N^{1.5}$ at the cost of $N^{1.5}$ larger die area. Note, that Eqs. (18)–(22) are also valid for the 2-level case ($N = 1$), recalling that the multi-level derivation in this section is the generalization of the 2-level bridge-leg.
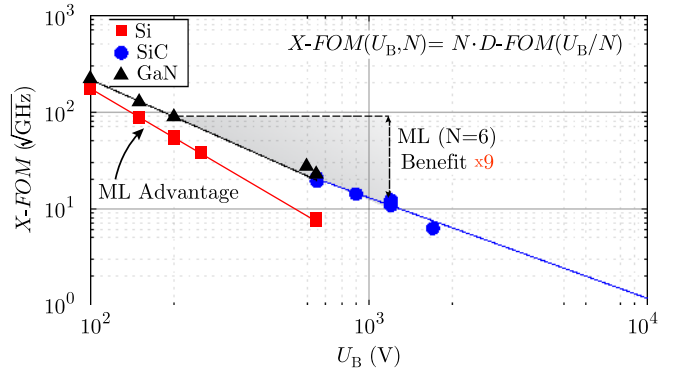
FIGURE 8. The extended Figure-of-Merit X-FOM for multi-level bridge-legs for the same device survey and operating conditions as Fig. 7. The X-FOM values are normalized around the 1200 V devices, which serve as a benchmark for 2L bridge-legs operating with $U_{dc} = 800$ V.

X-FOM OF COMMERCIAL DEVICES

With the Figures-of-Merit for multi-level bridge-leg configurations defined, we can numerically compare commercial semiconductors for an example application and consider the broader implications of the D-FOM and X-FOM. For a tangible comparison, we take the case of a grid-interfaced PV inverter, assuming $U_{dc} = 800$V bus voltage and, to include a reasonable voltage margin, a device voltage rating of 1200V for a 2-level base case scenario.

In Fig. 8, we highlight that the improvement when moving from a 2-level with 1200V SiC MOSFETs to the 7-level case with 200V GaN HEMTs, the X-FOM improves by a factor of $N^{1-\alpha_{D\text{-}FOM}} = N^{1.2} \approx 9$ for the 7-level configuration, as shown in Fig. 8, and the semiconductor bridge-leg losses will decrease by the same factor for a fixed voltage-time product applied to the inductor. This massive reduction in semiconductor losses may enable the designer to eliminate the forced cooling system (fan and heatsink) and realize other system improvements [17], [38]. Recognizing, however, that improvements in power density may also be desired, we relax the assumption of a fixed $L_o \Delta i_L$ in the following section to explore the X-FOM-predicted system-level benefits of the multi-level topology.

### V. CASE STUDY & EXPERIMENTAL VERIFICATION

To this point, we have defined an extended FOM, X-FOM, that can be applied to multi-level bridge-legs to determine the performance of the switching stage. Using the X-FOM, we identified that multi-level topologies can lead to higher performance, both because of the higher D-FOM of lower voltage devices and the switching frequency multiplication with smaller voltage steps that results from the nature of multi-level structures. To highlight the powerful topology analysis provided by the X-FOM, and how this can be translated into a quantifiable increase in performance, a case study is presented, analyzed, and validated with experimental results.

A. CASE STUDY DEFINITION

The analyzed system consists of the inverter stage of a grid-connected three-phase PV inverter, like the one highlighted in

TABLE 4. Nominal Characteristics of the Two Selected Devices. All Values are Given for 25 °C and for the Switched Voltage U_{sw}

Num. Levels	Tech.	U_{rated}	Manuf.	Part Number	U_{sw}	R_{on}	$C_{oss,Q}$	Q_{oss}	$Q_{oss}U_{sw}$	D-FOM	X-FOM
2-Level	SiC	1200 V	*Wolfspeed*	C3M0032120K/D	800 V	32 mΩ	249 pF	199 nC	160 uJ	$10.7\sqrt{GHz}$	$10.7\sqrt{GHz}$
3-Level (ML)	SiC	650 V	*Infineon*	IMZA65R027M1H	400 V	27 mΩ	367 pF	147 nC	59 uJ	$9.5\sqrt{GHz}$	$19.0\sqrt{GHz}$
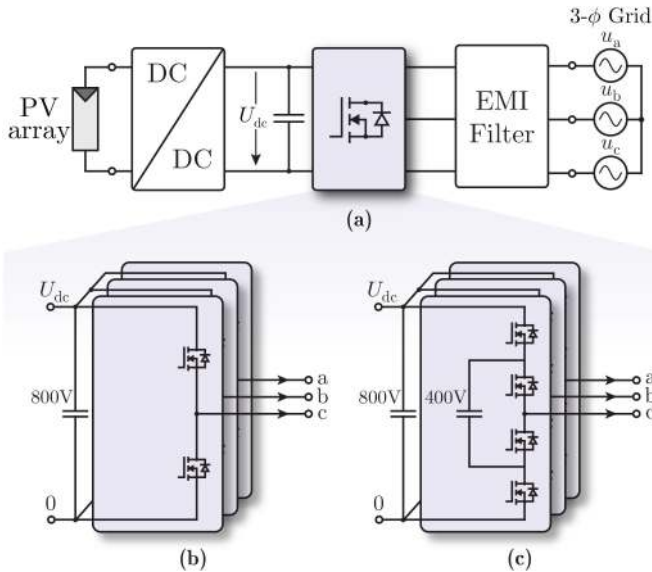
FIGURE 9. (a) Example use case for the efficiency-optimized bridge-legs considered here, shaded in blue, which are part of the DC-AC conversion stage in a three-phase, grid-connected photovoltaic (PV) array with an 800V DC-link (U_{dc}) and a 400 V_{rms} line-to-line grid voltage. (b) 2-level bridge-leg configuration that can use 1200 V-rated switches, and (c) 3-level FCML bridge-leg configuration that can feature switches rated for 600-650 V.

Fig. 9(a). The key nominal characteristics are a rated power of 10 kW, a DC-link voltage of 800 V, and an RMS grid interface voltage of 400 V_{rms} (line-to-line).

In this context, two different bridge-leg configurations are considered for each of the three phases:

- 2-level bridge-legs featuring 1200 V semiconductor technology (Fig. 9(b)), and,
- 3-level FCML bridge-legs featuring 600-650 V semiconductor technology (Fig. 9(c)).

A state-of-the-art commercially-available SiC MOSFET is selected for the implementation of each of these configurations, respectively:

- 1200 V 32mΩ SiC device, and,
- 650 V 27mΩ SiC device.

The key characteristics of these switches are shown in Table 4. As Fig. 7 shows, 650V GaN HEMTs have a similar D-FOM to the selected 650V SiC MOSFET, but for a direct comparison on an X-FOM basis, we prefer to use two devices from the same technology class – i.e., without commercial 1200V GaN HEMTs available, we choose the 650V SiC MOSFET for the comparison instead of a GaN HEMT. However, with the similar D-FOM (cf., Fig. 7), many of the conclusions drawn will be directly transferable to 600/650V GaN HEMTs.

For the following analysis, a balanced three-phase grid is assumed, where each one of the three phases processes, on average, the same power. We can therefore focus, without loss of generality, our analysis on only one of the phases and/or bridge-legs, under the premise that it processes one third of the rated power (3.3 kW).

B. USING THE X-FOM TO TRADEOFF SEMICONDUCTOR EFFICIENCY AND POWER DENSITY

Until now, we have been exploring the case where $L_o \Delta i_L$ is held constant across different number of levels, and we have aimed to minimize the semiconductor stage losses. By relaxing this constraint, however, we can introduce a second degree of freedom to the converter design space that leverages the advantages of ML topologies.

To explore this design space [39], Eq. (19) that describes the minimum (conduction + switching) semiconductor losses $P_{semi,min}$ can be rewritten with (15) and (17) as a function of the voltage-time product $L_o \Delta i_L$:

$$P_{semi,min}\Big|_{ML} = \frac{I_{rms}U_{dc}^{1.5}}{\sqrt{L_o\Delta i_L}\cdot X\text{-FOM}(U_{dc},N)}. \tag{23}$$

With this loss-minimized equation that now includes the filter stress as $L_o \Delta i_L$, we can analyze the potential performance gains of the bridge-leg and the filter stress in turn.

1) P_{semi} REDUCTION

With the same filter and same filter inductor stresses $L_o \Delta i_L$ for the 3-level and 2-level case, the difference between the minimum achievable losses of a system with the *same voltage-time product* ($L_o \Delta i_L$) is:

$$\frac{P_{semi,min,3L}}{P_{semi,min,2L}} = \frac{X\text{-FOM}_{2L}}{X\text{-FOM}_{3L}} = 0.56 \tag{24}$$

The vertical arrow in Fig. 10(a) represents this improvement – an increase in X-FOM (cf., Table 4) directly translates into a 44% reduction in the minimum achievable semiconductor losses.

2) FILTER $L_o \Delta i_L$ REDUCTION

On the other hand, the bridge-leg losses could be held constant and we could seek to miniaturize the filter by taking advantage of the $L_o \Delta i_L$ reduction [19]. In this case, the ratio of $L_o \Delta i_L$ between converter topologies and/or device technologies is given by the square of the inverse of the X-FOM:

$$\frac{(L_o\Delta i_L)_{3L}}{(L_o\Delta i_L)_{2L}} = \left(\frac{X\text{-FOM}_{2L}}{X\text{-FOM}_{3L}}\right)^2 = 0.32 \tag{25}$$
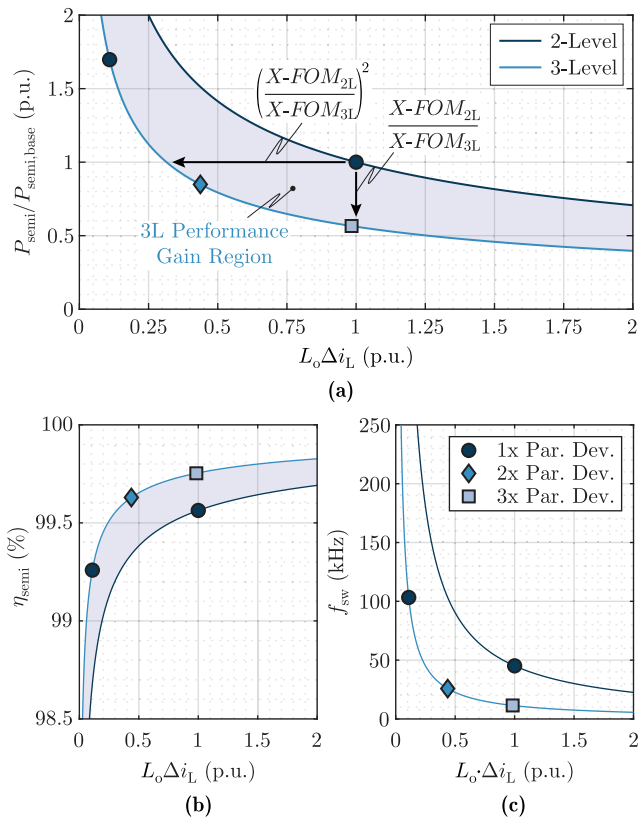
FIGURE 10. Axes and tradeoffs of performance gains from increasing the X-FOM from a 2-level to a 3-level FCML bridge-leg: (a) semiconductor (conduction + switching) losses normalized to the 2-level case, (b) semiconductor-stage efficiency, and switching frequency (c) vs. $L_o \Delta i_L$. The X-FOM values are taken from Table 4, and all values are calculated for rated power (3.3 kW) assuming a junction temperature of 75 °C. The ● represents that one single device (of the 1200 V 32mΩ SiC device for the 2-level case and of the 650 V 27mΩ SiC device for the 3-level case) is the optimum for that operating point, the ♦ represents that two paralleled devices (twice the die area) is optimal, and the ■ represents that three paralleled devices is optimal for the respective operating point.

In Fig. 10(a), this is represented by the arrow pointing to the left, where the voltage-time product is reduced by 68% for the improvement in X-FOM between the considered 2-level and 3-level bridge-legs. For the same current ripple, then, the inductance can be reduced, or vice-versa, or some combination of both. The consequences of reducing $L_o \Delta i_L$ are comprehensively shown in [19], where, with fixed semiconductor losses among two-, three- and seven-level bridge-legs, the passive component volume decreases by 65% (3-level) and 89% (7-level) relative to the two-level bridge-leg.

3) COMBINED P_{semi} AND $L_o \Delta i_L$ PERFORMANCE GAIN
Finally, the shaded areas in Fig. 10 focus on this combined improvement design space. In the highlighted "Performance Gain Region," the designer can use the knob of switching frequency to select any combination of bridge-leg improvement and filter size and/or efficiency improvement. Although the D-FOM is lower for the 3-level case than for the 2-level case (9.5 $\sqrt{GHz}$ vs. 10.7 $\sqrt{GHz}$, respectively, cf., Table 4),

it features a nearly 2× higher X-FOM, explaining the resulting "Performance Gain Region" in Fig. 10. These significant gains in semiconductor losses and filter stress are entirely driven by the topology advantage – the 3-level bridge-leg device has a slightly *worse* D-FOM than the SiC MOSFET for the 2-level design, and therefore does not benefit from the typical gains of moving to lower-voltage devices (cf., Fig. 7).

We reiterate here that the performance gain region is valid for the case in which we always choose the optimal die area (or number of parallel devices). However, since only discrete devices are available from power semiconductor manufacturers, Fig. 10 also shows where one, two, and three parallel 650 V 27mΩ SiC devices (resulting in an equivalent R_{ds} of 27mΩ, 13.5mΩ and 9mΩ, respectively) are the optimal choice vs. the benchmark case of one single 1200 V 32mΩ device for the two-level bridge-leg.

For the benchmark 2-level bridge-leg, one single 1200 V 32mΩ device is the optimal choice at $f_{sw} = 46$ kHz. For the 3-level bridge-leg, one single 650 V 27mΩ device is optimal at $f_{sw} = 103$ kHz, two parallel devices are optimal at $f_{sw} = 26$ kHz, and three parallel devices are optimal at $f_{sw} = 11$ kHz, as seen in Fig. 10(c) (the relationship between f_{sw} and $L_o \Delta i_L$ is given in Eqn. (16)). If the goal is to minimize the filter stresses, the 3-level design should be realized with one single 650 V 27mΩ device switching at $f_{sw} = 103$ kHz. If the goal is instead to halve the semiconductor losses while maintaining a similar or identical filter, then the design should be realized with three parallel-connected 650 V 27mΩ devices switching at $f_{sw} = 11$ kHz. (Note that here we always refer to the individual device switching frequency (f_{sw}), and not the effective switching frequency (f_{eff}), cf., Eqn. (14).)

Finally, the X-FOM can be used to identify the maximum achievable efficiency of the semiconductor stage of a hard-switched bridge-leg, shown in Fig. 10(b) at the rated power. The efficiency of the bridge-leg, considering only the semiconductor losses, is calculated as:

$$\eta_{semi} = \frac{P_{in} - P_{semi}}{P_{in}} = 1 - \frac{P_{semi}}{P_{in}} \qquad (26)$$

where P_{in} is the input power.

C. ADDING MEASURED SWITCHING LOSSES TO THE X-FOM THEORY
Thus far, with both the D-FOM and the X-FOM, we have only accounted for conduction losses and the capacitive hard-switching losses, which are the minimum losses that can occur in a hard-switched bridge-leg ($E_{sw,min} = U_{sw}Q_{oss}$) [10]. As a final step towards validating the efficacy of the X-FOM concept in predicting the performance of different bridge-leg structures, we now include the measured switching losses instead of the minimum theoretical hard-switching losses.

To obtain accurate switching loss data, we use the calorimetric switching loss measurement method presented and validated in [32], [40], [41]. In this method, the switches are mechanically attached and thermally coupled to a brass block. By measuring the time required to increase the brass block
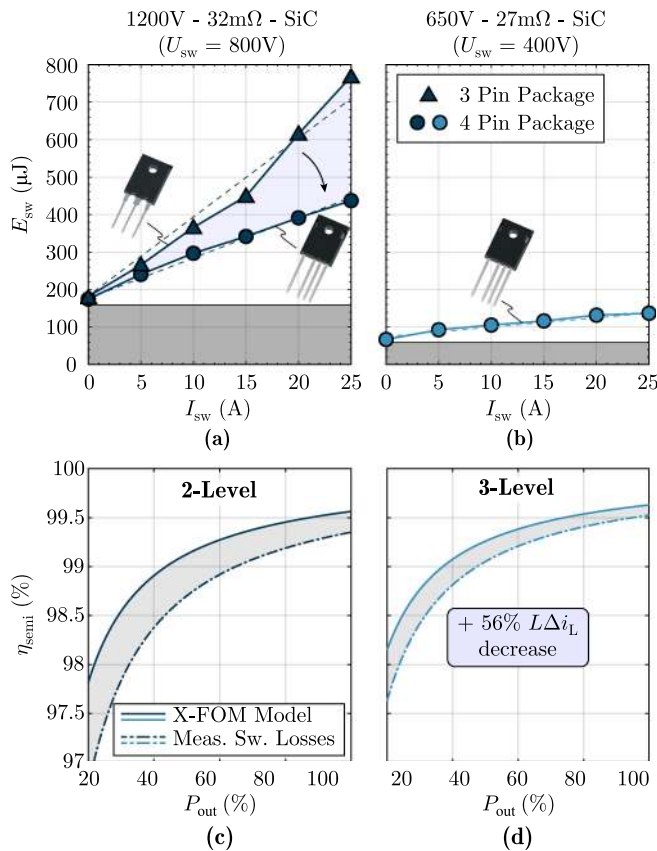
FIGURE 11. (a–b) Measured switching losses (hard + soft transition) of the 1200 V and 650 V devices, respectively, given in Table 4. In (a–b), the area shaded in grey represents the share of switching losses accounted for in the X-FOM calculations, i.e., the minimum hard-switching losses of $Q_{oss}U_{sw}$, and the dashed lines show the linearization of the switching losses (cf., Eqn. (27) and Table 5). In (c) and (d) the bridge-leg semiconductor efficiency is shown for the X-FOM model (19) and with the measured switching losses for the 2-level and 3-level bridge-leg cases in 4-pin packages, respectively. The 2-level bridge-leg uses one parallel device (● in Fig. 10) and the 3-level case uses two parallel devices per switch (♦ in Fig. 10).

temperature by a given amount (e.g., $\Delta T = 10\ °C$), and by subtracting the conduction losses (R_{on} of the devices under test is measured with varying temperature during the calibration), the semiconductor switching losses can be extracted.

The measured losses for the 1200 V 32mΩ SiC devices in both 3-pin and 4-pin TO-247 packages are presented in Fig. 11(a), and the measured hard-switching losses for the 650 V 27mΩ SiC device in a 4-pin TO-247 package are presented in Fig. 11(b), for an average junction temperature of 129.5 °C (±10 °C) and 91.5 °C (±10 °C), respectively (to guarantee the accuracy of the switching loss measurements by ensuring that the switching losses are always larger than the conduction losses [31], for the 1200 V devices, a larger brass block is needed [40] and correspondingly higher losses have to be generated leading to a slightly higher junction temperature). The employed gate drivers are the 1EDI60I12AF from *Infineon*, and all of the measurements were taken with 0Ω (both turn-on and turn-off) external gate resistances. Since 4-pin devices

TABLE 5. First Order Polynomial Coefficients for Devices in Fig. 11(a–b) Resulting from a Polynomial Fit According to Eqn. (27)

| | 1200 V - 32 mΩ | | 650 V - 27 mΩ |
	3-pin	4-pin	4-pin
$k_{sw,0}$ [μJ]	180.0	176.6	76.4
$k_{sw,1}$ [μJ/A]	21.0	10.9	2.7

feature a Kelvin source connection, the current dependence of the switching losses is drastically reduced relative to the 3-pin devices that don't feature a dedicated Kelvin source contact [42]. This can be clearly seen in Fig. 11(a), where for the same MOSFET the 3-pin device shows (for example, at 25 A) 64% higher losses than the 4-pin device. Therefore, the measurements on the 4-pin package are used for the losses of the 1200 V device, and the switching loss reduction from a 3-pin to a 4-pin package is revisited at the end of this section.

Nevertheless, the switching losses in Fig. 11(a–b) still feature a current dependent term, which can be modelled with a first order polynomial (linear) curve [43]:

$$E_{sw}(I_{sw}) = k_{sw,0} + k_{sw,1}I_{sw}. \qquad (27)$$

The first term, $k_{sw,0}$, is current-independent (but die area-dependent) and is described by Eqn. (3) as $k_{sw,0} = C_{oss,Q}(U_{dc})U_{dc}^2$. The second term, $k_{sw,1}$, describes the linear dependence of switching losses on the current ($V - I$ overlap losses), can be empirically measured, and depends on different factors that limit the switching speed such as the turn-on gate resistance, gate voltages, and gate loop inductance (including the common source inductance, the effect of which can be reduced if the device features a Kelvin connection, cf., Fig. 11(a–b) and Table 5), as well as on the reverse recovery charge of the (parasitic) body diodes [44], [45]. Assuming that the current splits equally among N_{par} paralleled devices and considering Eqn. (27), then the switching losses are:

$$E_{sw}(I_{sw}, N_{par}) = N_{par}\left(k_{sw,0} + k_{sw,1}\frac{I_{sw}}{N_{par}}\right)$$
$$= N_{par}k_{sw,0} + k_{sw,1}I_{sw} \qquad (28)$$

where $N_{par} = A_{die}/A_{die,base}$, with $A_{die,base}$ as the benchmark die area for which $k_{sw,0}$ and $k_{sw,1}$ have been parameterized. We see that the linear term of the equation does (ideally) not depend on the die area or number of parallel-connected devices. In other words, one can switch, for example, one device with 25 A or two devices with 12.5 A each, the latter with larger constant (capacitive) losses but equal current-dependent losses. Note that a linear fit is also adequate for GaN devices, as shown e.g., in [46] for 600V devices and in [32] for 200V devices, as well as e.g., for 200V silicon devices [32]. Hence, when writing the semiconductor losses as in Eqn. (6) and deriving the optimal die area ($\frac{dP_{semi}}{dA_{die}} = 0$), the linear part of the switching losses has no effect on the optimal die area, but it does influence the absolute value of the losses, which will be larger when we include the current dependence of the switching losses.

This is highlighted in Fig. 11(c–d), where the calculated semiconductor efficiency over output load of a 2-level bridge-leg with *one* parallel device is shown in comparison to a 3-level bridge-leg with *two* parallel devices (as detailed in Fig. 10 and Table 4). In both cases, the predicted peak semiconductor efficiency at rated load matches those shown in Fig. 10(b), where the 2-level bridge-leg should reach 99.56% and the 3-level bridge-leg 99.63%. When we add the measured switching losses, the peak efficiency is reduced to 99.35% and 99.53%, respectively, leading to a 0.21% and 0.10% deviation between the X-FOM model and the actual losses. This difference arises because the X-FOM only includes the minimum hard-switching losses, providing a minimum boundary for the losses (and identifying the maximum bridge-leg performance). The linear switching loss term only provides a loss offset that shifts the efficiency curve downwards (Fig. 11(c–d)) but, we reiterate, does not influence the optimal die area selection. Finally, note that the larger deviation in the 2-level efficiency curves in Fig. 11(c–d) originates from the linear switching loss term, which is larger in the 1200 V devices than in the 650 V devices (Fig. 11(a–b)).

In the end, even with the measured switching losses, the 3-level achieves both a 0.18% semiconductor efficiency increase (a 27% decrease in loss fraction) and a 56% $L_o \Delta i_L$ decrease, which, according to [19], would reduce the inductor volume by approximately the corresponding fraction.

In this case study, the X-FOM identified the performance improvement for the PV inverter semiconductor stage when moving from a 2-level bridge-leg to a 3-level bridge-leg. By using the X-FOM approach, we can calculate the relative gains that are expected in terms of semiconductor losses and filter stress, identify the maximum achievable efficiency of the semiconductor stage for both cases, and obtain the optimal combinations of switching frequency and number of parallel devices. Although additional losses that occur surrounding the bridge-leg losses in a full converter system (e.g., magnetics, flying capacitors, clamping diodes) are not directly considered, with the X-FOM we clearly identify an advantage in terms of the switching losses, the filter stress, or a combination of both by moving from a 2-level to a 3-level bridge-leg structure. Finally, by including the switching loss measurements, the X-FOM-predicted performance gain of the 3-level bridge-leg (relative to the 2-level structure) is validated, where we confirm that there is no region in the switching loss and filter stress performance space where the 2-level outperforms the 3-level structure (even when using devices with a higher D-FOM for the 2-level bridge-leg).

D. FUTURE CHALLENGES OF WBG DEVICES
One of the largest challenges identified with the X-FOM – setting aside technology specific issues like the reverse recovery charge for Silicon and SiC MOSFETs [47] and dynamic R_{on} for GaN HEMTs [48] – is the need for the development of advanced semiconductor packaging solutions. From Fig. 11(a) it becomes clear that the efficiency difference between the X-FOM-predicted efficiency and the real efficiency can
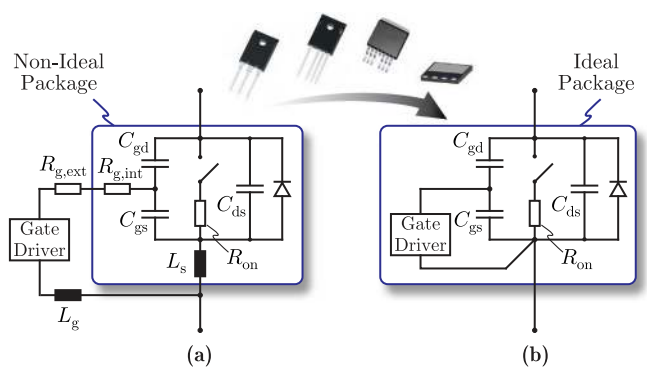

FIGURE 12. (a) Gate driver, power semiconductor package and model of a voltage-controlled switch with the main parasitics that influence the switching transients, and **(b)** the idealization of the gate driver and semiconductor packaging that reduce the inevitable parasitic elements. L_g is the gate driver loop inductance, $R_{g,ext}$ the external gate resistance, $R_{g,int}$ the internal MOSFET gate resistance and L_s the common gate-source inductance.

be reduced by simply adding a Kelvin connection [42]. As semiconductor technology has improved (and especially with the faster switching speed provided by WBG devices [49], [50]), better device packages with reduced parasitics that increase switching performance and reduce overvoltages [44], [45], [51] have become available (e.g., devices with planar bond wires [52] or direct PCB connection [53], [54] for SiC devices and surface-mounted devices for GaN HEMTs [55]). With the integration of the gate driver circuitry, as shown in Fig. 12, into both lower-voltage (< 200 V) [56], [57] and higher-voltage semiconductors (> 600 V) [58], [59] (which leads to lower parasitic inductances L_g and L_s, higher power density, reduced component count, lower system complexity, and lower cost [60], [61]), there is the potential to further reduce current-related switching losses. With these developments, the X-FOM approach becomes an increasingly valuable tool to quantify both the relative and absolute performance of a certain combination of semiconductor and topology.

VI. CONCLUSION
By applying fundamental principles to model the conduction and switching losses of hard-switched semiconductor bridge-legs, a device Figure-of-Merit (D-FOM) is derived and extended to the X-FOM. While the D-FOM only refers to the performance of an individual semiconductor device, the X-FOM quantitatively compares the performance of individual devices of all voltage ratings across a number of topologies, with a particular focus on multi-level structures here. The X-FOM is a simple-yet-powerful metric to evaluate the performance of the semiconductor stage of a system. It identifies, among others,

1) the performance gain that can be obtained either in semiconductor stage losses and/or in the filter design requirements,
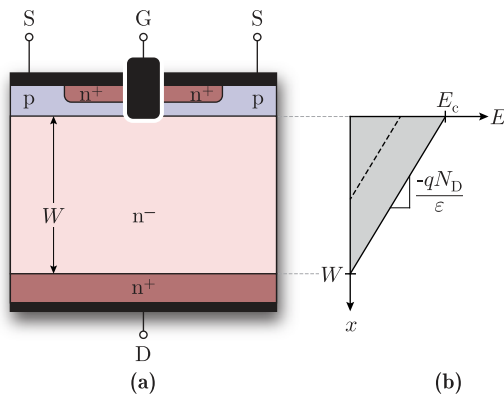
FIGURE 13. (a) Vertical n-type MOSFET structure and (b) electrical field distribution in the drift region. (a) and (b) are considered for the derivation of the theoretical scaling of R'_{on} and $C'_{oss,Q}$ with blocking voltage to complement the empirical study performed in this work.

2) the maximum efficiency that can be achieved by the semiconductor stage by selecting the loss-optimal die area for each frequency, and
3) the loss-optimal die area (or number of parallel devices) for each switching frequency.

Furthermore, the X-FOM reveals the underlying enablers behind the higher efficiency and/or reduced filter size of multi-level converters, and provides a simple tool to quantify these two parameters. This is shown by applying the X-FOM to a case study where the semiconductor stage performance of a three-phase PV inverter is analyzed, in which we show that the 3-level bridge-leg offers superior performance to its 2-level counterpart on both power semiconductor loss and filter stress – despite using fundamentally lower-performance devices. This is further validated by adding measured switching loss data to the X-FOM theory and analysis.

Finally, the X-FOM also identifies the remaining performance gap between the losses of *ideally*-packaged power semiconductors and *real* commercial ones. This reaffirms the X-FOM as a valid performance metric for future power electronics converters, where devices with switching losses close to the theoretical minimum are expected to become increasingly available.

APPENDIX A
SEMICONDUCTOR PHYSICS BASED DERIVATION OF THE PROPOSED DEVICE FIGURE-OF-MERIT

To understand the fundamental dependencies on the blocking voltage of the specific on-state resistance R'_{on} and specific charge equivalent capacitance $C'_{oss,Q}$, a physics-based derivation of these values is presented in the following for a vertical MOSFET device (Fig. 13(a)), where a one-dimensional (1D) approximation of an ideal drift region is assumed [22]. This basic derivation should only serve as a theoretical framework to understand principal physical semiconductor dependencies. For detailed semiconductor physics analysis of WBG devices, please refer to [22].

A. CONDUCTION LOSSES: R'_{on} SCALING

For the R'_{on} derivation, only the resistance of the n$^-$ drift region is considered, since the resistance of this region dominates the R'_{on} for vertical MOSFETs with blocking voltages above 50V [62]. We further make the traditional assumption of unipolar carrier conduction.

The blocking voltage U_B for a vertical MOSFET that maximizes its electric field such that the critical field E_c is reached at the breakdown voltage (cf., Fig. 13(b)) is given by:

$$U_B = \frac{E_c W}{2}, \tag{29}$$

from which the required width of the drift region W is:

$$W = \frac{2U_B}{E_c}. \tag{30}$$

Assuming an optimally-doped drift region, the doping concentration N_D is:

$$qN_D = \frac{\varepsilon E_c}{W} = \frac{\varepsilon E_c^2}{2U_B}, \tag{31}$$

where q is the elementary charge, and ε the permittivity. With the on-state resistance

$$R_{on} = \frac{W}{\sigma A} = \frac{W}{qN_D \mu A} \tag{32}$$

where σ is the conductivity, μ the donor carrier mobility and A the semiconductor area, the specific (area-related) on-state resistance can be calculated with (30) and (31) as:

$$R'_{on} = R_{on}A = \frac{4U_B^2}{\mu \varepsilon E_c^3} \propto U_B^2. \tag{33}$$

Therefore, the theoretical limit for vertical devices shows a dependency $R'_{on} \propto U_B^2$. It is widely documented in literature, though, that the empirical Si dependence on blocking voltage for vertical devices is $R'_{on} \propto U_B^{2.5}$ (mainly due to the dependency of E_c on N_D, where lowering N_D, which is required for blocking higher voltages, cf., (31), also leads to a reduction in E_c) [23], [62], [63] and coincides with the device survey performed in Section II. Both Si and SiC devices are variations of vertical structures, and although the device structure may vary, for instance, by including field plates to shape the electric field profile [64], this derivation yields a valid insight for both of these technology classes.

For lateral GaN-on-Si HEMTs, the ideal on-resistance, only considering the drift region (valid for high breakdown voltages), is [21], [65]:

$$R'_{on} = \frac{L_{drift}^2}{q\mu Q_s}, \tag{34}$$

where L_{drift} is the drift region length and Q_s is the 2-D electron gas (2DEG) charge-sheet density. Assuming a constant electric field in the drift region, the drift length is $L_{drift} = U_B/E_c$, and we again find the $R'_{on} \propto U_B^2$ theoretical dependency. At lower voltages, the channel resistance dominates – which is not voltage-dependent – and R'_{on} has a lower proportionality constant (we find $R'_{on} \propto U_B^{1.1}$ in our empirical survey). These
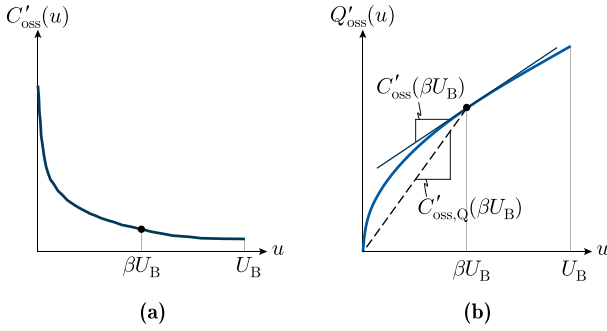
FIGURE 14. Exemplary (a) (differential) output capacitance C'_{oss} and (b) output charge as a function of u, where the distinction between C'_{oss} and $C'_{\text{oss,Q}}$ evaluated at $u = \beta U_{\text{B}}$ is shown.

two regions of U_{B} dependence are shown in Fig. 3 and are discussed in [21].

B. SWITCHING LOSSES: $C'_{\text{oss,Q}}$ SCALING

Similar to the derivation of R'_{on}, a basic physical derivation for the specific charge equivalent capacitance across the depletion region of vertical devices $C'_{\text{oss,Q}}$ is presented here.

The definition of specific (differential) capacitance is:

$$C'_{\text{oss}}(u) = \frac{dQ'_{\text{oss}}(u)}{du}, \tag{35}$$

where u is the voltage across the depletion region and Q'_{oss} is the specific charge in the depletion region. To obtain C'_{oss}, a relation between the charge and the voltage has to be found, for which the voltage drop across the drift region is derived as a function of x (cf., Fig. 13):

$$du(x) = \frac{qN_{\text{D}}x}{\varepsilon}dx = \frac{x}{\varepsilon}dQ'_{\text{oss}}(x), \tag{36}$$

which leads to the capacitance:

$$C'_{\text{oss}}(x) = \frac{dQ'_{\text{oss}}(x)}{du(x)} = \frac{\varepsilon}{x}. \tag{37}$$

However, since the capacitance as a function of voltage u (and not x) is desired, by integrating the voltage u over x (see (36)) and solving for x with use of (31):

$$x = \frac{2}{E_{\text{c}}}\sqrt{U_{\text{B}}}\sqrt{u} \tag{38}$$

is obtained, which is then substituted in (37) to yield [6]:

$$C'_{\text{oss}}(u) = \frac{\varepsilon E_{\text{c}}}{2}\frac{1}{\sqrt{U_{\text{B}}}\sqrt{u}}. \tag{39}$$

Now that the specific differential capacitance across the depletion region $C'_{\text{oss}}(u)$ has been modelled, the charge-equivalent specific capacitance $C'_{\text{oss,Q}}(u)$ can be analytically obtained. For this, the charge stored in the depletion region has to be calculated. This is done as a function of the voltage utilization of the device β (defined as $u = \beta U_{\text{B}}$, where

$0 \leq \beta \leq 1$):

$$Q'_{\text{oss}}(\beta) = \int_0^{\beta U_{\text{B}}} C'_{\text{oss}}(u)du = \varepsilon E_{\text{c}}\sqrt{\beta}. \tag{40}$$

The charge Q'_{oss} stored in the depletion region is independent of the blocking voltage U_{B}, and only depends on E_{c} (and not W). This is because for a given E_{c}, to block a higher voltage U_{B}, the depletion region W is enlarged (see (29)), but to stay below the critical field E_{c} the charge density N_{D} must be reduced, leading to a U_{B}-independent charge in the drift region (see Fig. 13(b) and (31)). Note, however, that for devices that feature two-dimensional (2D) p-n junctions (e.g., field plate or superjunction concepts [23], [32], [64]) instead of 1D p-n junctions, additional Q'_{oss} charge to the one modelled in (40) is introduced in the device (due to the 2D nature of the p-n junction) as a tradeoff to reduce the R'_{on}.

With the charge defined, the (absolute) charge-equivalent capacitance is calculated as

$$C'_{\text{oss,Q}}(\beta) = \frac{Q'_{\text{oss}}(\beta)}{\beta U_{\text{B}}} = \frac{\varepsilon E_{\text{c}}}{\sqrt{\beta}U_{\text{B}}}. \tag{41}$$

For $\beta = 1$, i.e., a full voltage rating utilization of the device,

$$C'_{\text{oss,Q}} = \frac{\varepsilon E_{\text{c}}}{U_{\text{B}}} \propto \frac{1}{U_{\text{B}}} \tag{42}$$

where it can be seen that $C'_{\text{oss,Q}}$ is inversely proportional to the blocking voltage U_{B} for vertical devices. Finally, we note that using (29) and (37) in (42), it can be found that:

$$C'_{\text{oss,Q}}(u) = 2C'_{\text{oss}}(u), \tag{43}$$

yielding that the (absolute) charge-equivalent capacitance is double the value of the (differential) capacitance across the junction for any given voltage, which is in fair agreement with real semiconductor devices (see Table 6).

C. DEVICE FIGURE-OF-MERIT

With the previous derivations, the D-FOM obtained in Section III can be expressed as a function of the permittivity ε and the resistivity (ρ) or the conductivity (σ):

$$\text{D-FOM} = \frac{1}{\sqrt{R'_{\text{on}}C'_{\text{oss,Q}}}} = \sqrt{\frac{1}{2\varepsilon\rho}} = \sqrt{\frac{\sigma}{2\varepsilon}}. \tag{44}$$

Alternatively, using the R'_{on} and $C'_{\text{oss,Q}}$ as a function of physical properties of the materials (see (33) and (42)), the D-FOM can also be defined as:

$$\text{D-FOM} = \frac{1}{\sqrt{R'_{\text{on}}C'_{\text{oss,Q}}}} = \frac{E_{\text{c}}}{2}\frac{\sqrt{\mu}}{\sqrt{U_{\text{B}}}} \propto \frac{1}{\sqrt{U_{\text{B}}}}, \tag{45}$$

where we see that the D-FOM is inversely proportional to the square root of U_{B}. This dependency of the D-FOM on $\frac{1}{\sqrt{U_{\text{B}}}}$ proves to be the case of Si devices, however for the SiC and GaN cases, the dependency is slightly lower, with $\frac{1}{U_{\text{B}}^{0.3}}$ and $\frac{1}{U_{\text{B}}^{0.2}}$, respectively (cf., Fig. 7 and Table 3).

TABLE 6. Capacitance and Energy Values for a Survey of Different Voltage MOSFETs. All of the Capacitance, Charge, and Energy Values are Evaluated at $u = U_{sw}$

Device		Capacitance			$E_{sw,min}$		
Model	$U_{sw}(V)$	$C_{oss,Q}$ (pF)	C_{oss} (pF)	$C_{oss,Q}/C_{oss}$	$Q_{oss}U_{sw}$ (µJ)	E_{oss} (µJ)	$Q_{oss}U_{sw}/E_{oss}$
1200 V SiC	800	250	131	1.9	159.7	53.1	3.0
650 V SiC	400	482	292	1.7	77.3	27.9	2.8
600 V GaN	400	102	71	1.4	16.4	6.4	2.6
200 V GaN	133	523	365	1.4	9.2	3.7	2.5
200 V Si	133	1336	370	3.6	23.6	5.4	4.4

D. ZERO-CURRENT SWITCHING - MINIMUM HARD-SWITCHING LOSSES

Refs. [24], [35] and Fig. 4 show that the minimum hard-switching losses occur while switching zero current and arise due to the capacitive switching losses (see Fig. 4) for bridge-legs that only employ switch-switch pairs (and not diode-switch pairs). These are defined as $E_{sw,min} = Q_{oss}(U_B)U_B$, assuming that the blocking voltage is the switched voltage.

However, to get an understanding of how these losses relate to the energy stored in the output capacitance of the device (typically referred to as E_{oss} in the datasheets, a convention that is kept here), (39) can be taken to obtain the energy stored in the capacitance:

$$E_{oss}(U_B) = \int_0^{U_B} C_{oss}(u)u\,du = \frac{1}{3}\varepsilon E_c U_B \qquad (46)$$

whereas from (40) with $\beta = 1$,

$$Q_{oss}(U_B)U_B = \varepsilon E_c U_B \qquad (47)$$

Hence, the minimum hard-switching losses occurring while switching zero current switch-switch pairs are:

$$E_{sw,min} = Q_{oss}(U_B)U_B = 3E_{oss}(U_B), \qquad (48)$$

concluding that the minimum hard-switching losses for switch-switch pairs are approximately three times larger than the E_{oss}, closely matching the energy values given in Table 6 for real semiconductor devices.

APPENDIX B
QUASI TWO-LEVEL BRIDGE-LEG

A first step toward using lower-voltage devices is replacing a single higher voltage device with a series connection of N devices that each must block U_{dc}/N, which is shown in Fig. 15(a). This "Quasi 2-level" (Q2L) configuration switches all of the high-side or low-side devices simultaneously (no gate signal interleaving), resulting in the eponymous 2-level output voltage waveform shown in Fig. 15(b). In this case, the flying capacitors shown in the background of Fig. 15(a) can be used (employing capacitors with substantially reduced capacitance compared to the multi-level operation) to symmetrically partition the blocking voltage [38], [66].

To maintain the same filter structure and stresses as in the benchmark 2-level topology (by ensuring $f_{sw}|_{Q2L} = f_{sw}|_{2L}$),

(a)

(b)
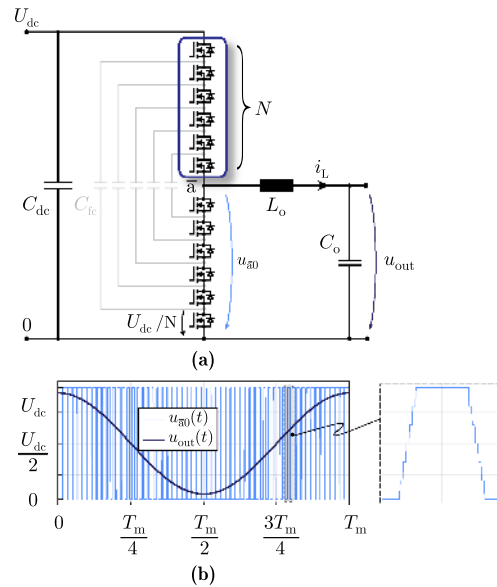
FIGURE 15. (a) Quasi Two-Level ("Q2L") bridge-leg configuration, with $2N$ devices per bridge-leg, featuring (b) a 2-level waveform with staircase shaped transitions [66]. Each power device must withstand U_{dc}/N, and small capacitors may be added to ensure equal voltage balancing during switching transients [38].

rewriting (6) the minimum semiconductor losses are:

$$P_{semi,min}\big|_{Q2L} = \frac{2I_{rms}U_{dc}\sqrt{f_{sw}|_{2L}}}{\text{D-FOM}\left(\frac{U_{dc}}{N}\right)}, \qquad (49)$$

which occur when using the optimal bridge-leg semiconductor area of:

$$A_{die,opt,tot}\big|_{Q2L} = 2\frac{N^2 I_{rms}}{U_{dc}}\sqrt{\frac{R'_{on}}{C'_{oss,Q}{}^{(U_{dc}/N)}f_{sw}|_{2L}}} \approx$$
$$\approx \sqrt{N}A_{die,opt,tot}\big|_{2L}. \qquad (50)$$

With (2) and (5), we find that the optimum die area $A_{die,opt,tot}$ of a Q2L bridge-leg is $\sqrt{N}\times$ larger than for a 2L bridge-leg.

Comparing (10) and (49), we see that the losses in the Q2L arrangement are only lowered by the ratio of D-FOM($\frac{U_{dc}}{N}$) to D-FOM(U_{dc}), i.e., there is no topological advantage (switching frequency multiplication) beyond the improved D-FOM of lower voltage devices (as there is for multi-level structures, as discussed in Section IV). Hence, for the quasi same output voltage waveform (i.e., same filter stress), the bridge-leg
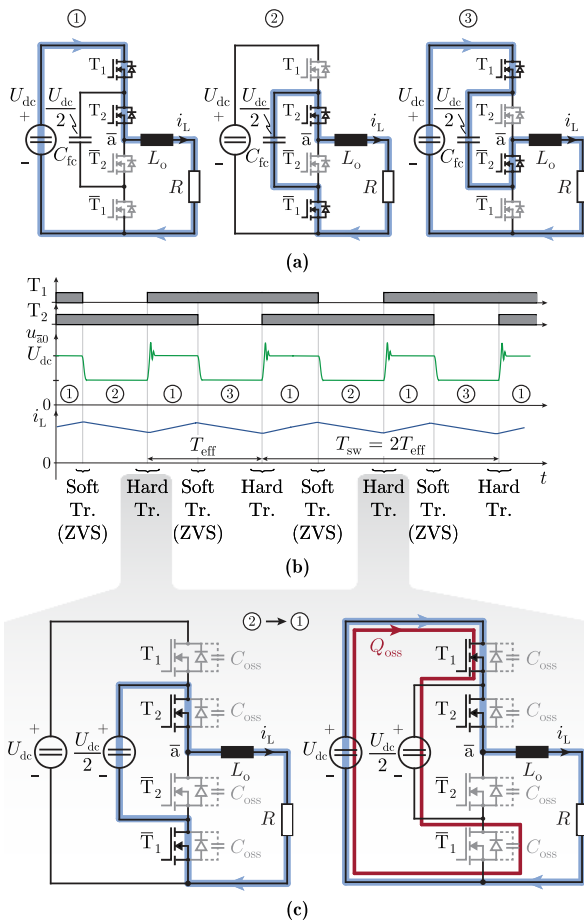
FIGURE 16. **(a)** Conduction states for the middle (2nd) and uppermost (3rd) levels of a 3-level FCML bridge-leg, shown for positive i_L. **(b)** Characteristic waveforms of the 3-level bridge-leg: T_1 and T_2 gate signals ($\overline{T}_1$ and $\overline{T}_2$ feature the opposite gate signals, respectively), the output voltage node voltage $U_{\overline{a}0}$ and the output current i_L. **(c)** Hard-switched transition for a 3-level bridge-leg, where the load current commutates from $\overline{T}_1$ to T_1. C_{fc} is considered to be a lossless voltage source with voltage $\frac{U_{dc}}{2}$ during the switching instant.

semiconductor losses are reduced by a factor $\approx \sqrt{N}$:

$$P_{\text{semi,min}}\big|_{Q2L} \approx \frac{P_{\text{semi,min}}\big|_{2L}}{\sqrt{N}}, \tag{51}$$

at the cost of an $\approx \sqrt{N}$ factor increase in die area. The X-FOM for the Q2L topology is, then, as:

$$\text{X-FOM}\big|_{Q2L} = \text{D-FOM}\left(\frac{U_{dc}}{N}\right) \approx \sqrt{N} \cdot \text{D-FOM}\big|_{2L}. \tag{52}$$

APPENDIX C
SWITCHING LOSSES IN MULTI-LEVEL BRIDGE-LEG SEMICONDUCTORS

In Section II-B, the minimum (capacitive) hard-switching losses were analyzed for a 2-level bridge-leg. This analysis is extended to a multi-level flying capacitor arrangement in the following. For the sake of clarity, initially a 3-level bridge-leg

is considered and later generalized to an $(N + 1)$-level structure.

Fig. 16(a), (b) revisit the conduction states for the middle (2nd) and the uppermost (3rd) level of a 3-level bridge-leg: state ① outputs U_{dc} at the node $\overline{a}$ (with reference to the negative DC bus), whereas state ② and ③ are generating $u_{\overline{a}} = \frac{U_{dc}}{2}$. Assuming a positive inductor current i_L, state ② charges and ③ discharges the flying capacitor C_{fc}.

For positive i_L, the switching transitions from state ② → ① and ③ → ① are hard-switched transitions, and ① → ② and ① → ③ are soft-switched transitions (the opposite holds for negative i_L).

To analyze the minimum (capacitive) hard-switching losses, the ② → ① hard-switched transition, which occurs once every switching period T_{sw} for the switch pair T_1 and $\overline{T}_1$, is shown in Fig. 16(c).

A charge Q_{oss} is delivered by the input voltage source, resulting in a charging of the C_{oss} of $\overline{T}_1$ to $u_{\overline{T}_1} = \frac{U_{dc}}{2}$, and a (slight) charging of C_{fc}. Considering C_{fc} as a temporary lossless voltage source with voltage $\frac{U_{dc}}{2}$, and performing an energy balance of the switching transition [24], this results in a dissipated energy of

$$E_{\text{dissipated}} = Q_{oss}\frac{U_{dc}}{2} = Q_{oss}U_{sw}. \tag{53}$$

This equation holds for $(N + 1)$-level bridge-legs, where $U_{sw} = \frac{1}{N}U_{dc}$, and Q_{oss} is the output capacitance charge evaluated at U_{sw}.

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