New fundamental insights into capacitance modeling of laterally non-uniform MOS devices

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***Abstract*— In compact transistor modeling for circuit simulation, the capacitances of conventional MOS devices are commonly determined as the derivatives of terminal charges, which in their turn are obtained from the so-called Ward-Dutton charge partitioning scheme. For devices with a laterally non-uniform channel doping profile, however, it is shown in this paper that *no* terminal charges exist from which the capacitances can be derived. Instead, for such devices a new model is presented for the capacitances themselves. Furthermore, a method is given to incorporate such a capacitance model into circuit simulators, which are traditionally based on terminal charge models. Comparison with 2-D device simulations and a segmentation model shows that for a constant mobility the new capacitance model provides an accurate description for a MOSFET with a laterally diffused channel doping profile. Through a comparison with high-frequency measurements the agreement between model and experimental results is discussed.**

***Index Terms*— Diffused Doping, LDMOS, Modeling, Charge Partitioning, Integrated Circuit Design.**

I. Introduction

LDMOS devices are well-known examples of MOS devices with a laterally non-uniform channel doping profile. Accurate modeling of the capacitances in high-voltage LDMOS devices is a prerequisite for integrated RF-design of, for instance, switched-mode power supplies and power amplifiers. For high-voltage devices often the sub-circuit model approach is followed, but the effect of the lateral non-uniformity in the channel is usually neglected [1]-[4]. In the sub-circuit models of [5] and [6], the lateral non-uniformity is taken into account, but results have been limited to the dc-behavior and its conductances. For capacitance modeling, efforts have been taken to incorporate the lateral channel non-uniformity in a terminal charge model [7]-[9]. However, we have shown [10] that incorporation of the lateral channel non-uniformity via a terminal charge model is *in*correct. Instead, we have developed a new capacitance model, which takes into account the lateral non-uniformity. Furthermore, we have provided a method to incorporate such a capacitance model into circuit simulators which are traditionally based on terminal charge models.

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In this paper, the results of [10] are elaborated, and the new capacitance model is derived in detail. Furthermore, we show additional, experimental results by comparing this capacitance model with high-frequency measurements performed on a MOSFET with a laterally diffused channel doping profile. In Sec. II the typical capacitance behavior of laterally non-uniform MOS devices, like an LDMOS transistor, is shown, and in Sec. III the charge and capacitance modeling of uniform MOSFETs is recalled. In Sec. IV it is shown that a terminal charge model does not exist for the description of the capacitances of laterally non-uniform devices. Next, in Sec. V the new capacitance model for laterally non-uniform MOS devices is derived. In Sec. VI the method for incorporation of the capacitance model into a circuit simulator (traditionally based on charge models) is demonstrated. Finally, in Sec. VII the new capacitance model is verified by comparison with high-frequency measurements, 2-D device simulations, and circuit simulations using a segmentation approach [11].

II. LDMOS devices

In Fig. 1 a cross-section of an LDMOS device is given. Due to diffusion from the source-side, the p-well doping of the LDMOS device decreases from source (S) to drain (D). In this way, a laterally non-uniform inversion channel region is formed with its doping concentration $N_A(x)$ being dependent on the lateral position x along the channel. The n^--drift region is needed to withstand high voltages applied between source and drain. In the specific LDMOS device of Fig. 1, the gate (G) extends over the drift region. In Fig. 2 a typical capacitance measurement on such an LDMOS device is shown, together with the simulation result of a sub-circuit model comprising MOS Model 11 (MM11; [12]) for the channel region and MOS Model 31 (MM31; [12]) for the drift region. Notice that the oxide of an LDMOS device is sufficiently thick to have no gate leakage.

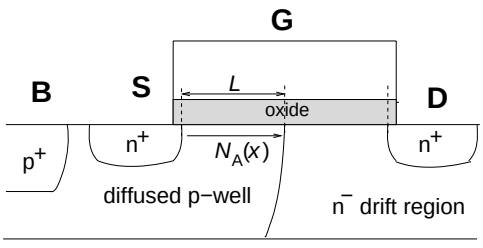

Fig. 1. Cross-section of an LDMOS device with a diffused p-well MOS channel region and an n^--type drift region.

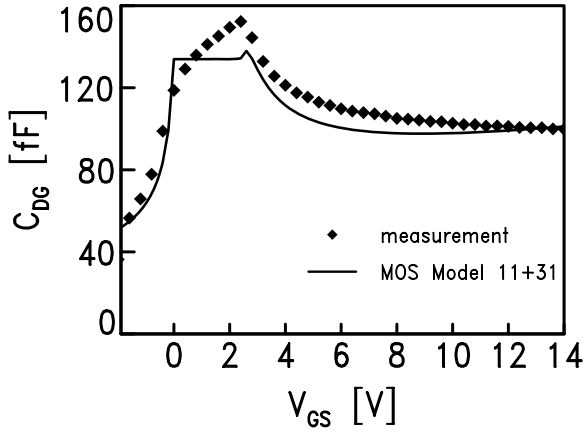

Fig. 2. Drain-gate capacitance of an LDMOS device at $V_{\rm DS} = 0$ V: symbols represent measurements and the solid line represents sub-circuit model simulations. The device has a total oxide capacitance of 180fF and a threshold voltage of 2.8 V. Note that the threshold voltage in the sub-circuit model is dictated by the I-V characteristics, which is determined by the threshold voltage of the channel region at the source side.

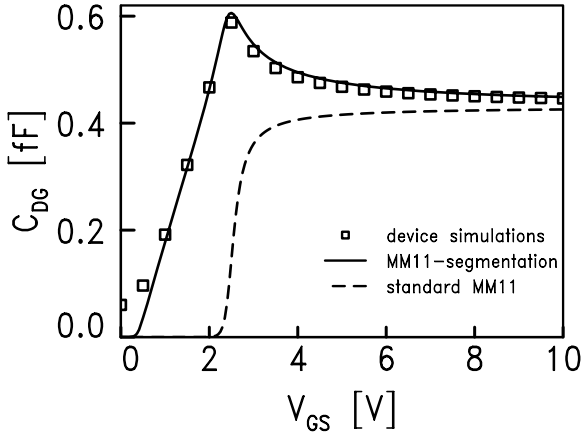

Fig. 3. Drain-gate capacitance of a MOSFET ($C_{\rm ox} = 0.86$ fF) with a laterally non-uniform channel doping profile ($D = 2.78$) at $V_{\rm DS} = 0$ V: symbols represent device simulations with MEDICI; the dashed line represents a compact model simulation with MM11; the solid line represents a circuit simulation with 20 segments each modeled by MM11 with parameters varying according to the doping profile (see also [11]).

The discrepancy between measurements and the sub-circuit model seen in Fig. 2 around the threshold voltage, triggered device simulations of a MOSFET with a non-uniform channel doping profile but without a drift region. For the non-uniform channel doping profile an exponential decay according to

$$N_A(x) = N_{A0} \exp\left[-D\left(\frac{x}{L}\right)^2\right] \tag{1}$$

is taken, where N_{A0} represents the doping concentration at the source ($x = 0$), and D ($D > 0$) represents the decay towards the drain ($x = L$). For such a MOSFET, the drain-gate capacitance obtained by device simulations using MEDICI is plotted in Fig. 3. In this figure we observe that a standard MOS model, like MM11, is not capable of describing the typical capacitance behavior of a laterally non-uniform MOS device. By comparison with a segmentation model [11] using 20 segments each modeled by MM11 with parameters varying according to the doping profile, we conclude that the peak in the capacitance behavior is caused by the non-uniform channel doping profile. Although the capacitance behavior of the laterally non-uniform device is accurately described by the segmentation model, the use of such model with many segments has been found to be limited because of the chance of non-convergence during simulation if no additional measures are taken.

III. Laterally uniform MOSFETs

Before turning to laterally non-uniform MOSFETs, we recall the charge- and capacitance modeling of *uniform* MOSFETs (see also [10]). As shown by [13], the total current I_i through terminal i of a uniform MOSFET is given by

$$I_i(t) = I_{\rm T}(t) + \frac{{\rm d}Q_i}{{\rm d}t}, \tag{2}$$

where $I_{\rm T}$ is the transport current and Q_i is the terminal charge in terms of the terminal voltages V_j. The source- and drain charge are obtained from the inversion charge using the well-known Ward-Dutton charge partitioning scheme. From the terminal charges Q_i the capacitances C_{ij}, which are defined in terms of the Y-parameters as $C_{ij} \equiv {\rm Im}\left[Y_{ij}\right]/(2\pi f)$, can be written as

$$C_{ij} = (2\delta_{ij} - 1)\frac{\partial Q_i}{\partial V_j}, \qquad i,j = {\rm S,G,D,B} \tag{3}$$

(see also [16]), where δ_{ij} is the Kronecker delta, i.e. $\delta_{ij} = 1$, $i = j$ and $\delta_{ij} = 0$, $i \neq j$. Thus, the existence of a terminal charge Q_i implies

$$(2\delta_{ik} - 1)\frac{\partial C_{ij}}{\partial V_k} = (2\delta_{ij} - 1)\frac{\partial C_{ik}}{\partial V_j} \tag{4}$$

and the integral $q_{{\rm c},\,i}$ of the charging current through terminal i, given by

$$q_{{\rm c},i}(t) \equiv \int_0^t \left[I_i(\tau) - I_{\rm T}(\tau)\right]{\rm d}\tau, \tag{5}$$

equals zero for a closed voltage cycle in time, i.e. $q_{{\rm c},\,i}(t_{\rm cycle}) = 0$, where $t_{\rm cycle}$ is the period of the cycle.

In Fig. 4 we have plotted the integral of the charging current through the drain-, gate-, source- and bulk terminal of a uniform MOSFET, described by MM11 (without gate leakage). We observe that indeed all the integrals are exactly equal to zero after a closed voltage cycle in time.

IV. Laterally non-uniform MOSFETs

We have tested both implications (4) and (5) of the existence of terminal charges for a laterally non-uniform MOSFET, using device simulations as well as circuit simulations with the segmentation approach mentioned above (see also [10]). Again, we do not consider gate leakage, since LDMOS devices have an oxide that is sufficiently thick. In Fig. 5, we observe that $\partial C_{\rm DG}/\partial V_{\rm D} \neq -\partial C_{\rm DD}/\partial V_{\rm G}$, which implies that (4) does not hold for the drain-related capacitances. In Fig. 6, on the other hand, we observe that the integrals of the charging current for several closed voltage cycles in time through the bulk- and gate terminal exactly equal zero. The integrals of

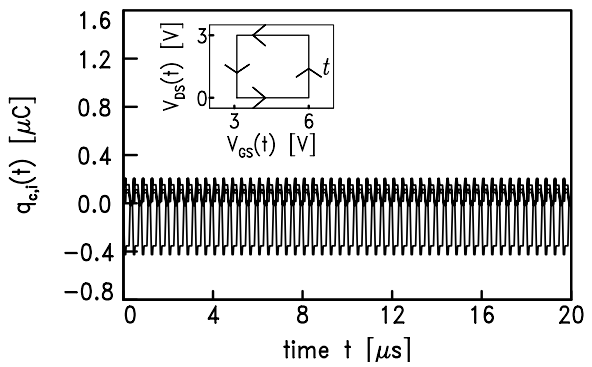

Fig. 4. Integral of the charging current through the drain- source-, gate- and bulk terminal of a uniform MOSFET, described by MM11, for 50 closed voltage cycles in time according to the inset ($t_{\rm cycle} = 0.4$ μs).

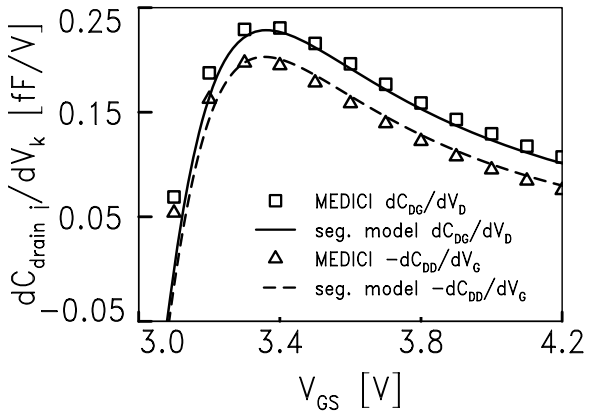

Fig. 5. Partial derivatives of drain-related capacitances for a laterally non-uniform MOSFET with a diffused doping profile according to (1) with $D = 2.78$, at $V_{\rm DS} = 0.5$ V.

the charging current through the drain- and source terminal, however, are not equal to zero.

Thus, (4) and (5) do *not* hold for the drain- and source terminal of a laterally non-uniform MOSFET. As a result, *no* terminal drain- and source charge exists for these devices. A terminal gate- and bulk charge, on the other hand, does exist (provided that there are no gate leakage currents). The above is in line with the general observations on non-linear dissipative systems [14] and with the terminal charge conservation constraints in [15]. Consequently, for a compact model of laterally non-uniform MOSFETs, instead of a terminal drain- and source charge, expressions for the capacitances have to be derived directly.

V. New capacitance model for laterally non-uniform devices

The electron drain-to-source current $I = I(x,t)$ at position x and time t is given by the transport equation and the continuity equation, according to (see [16])

$$\begin{cases} I = -W\,\mu\,Q_{\rm inv}\,\dfrac{\partial V}{\partial x}, \\ \dfrac{\partial I}{\partial x} = W\,\dfrac{\partial Q_{\rm inv}}{\partial t}, \end{cases} \tag{6}$$

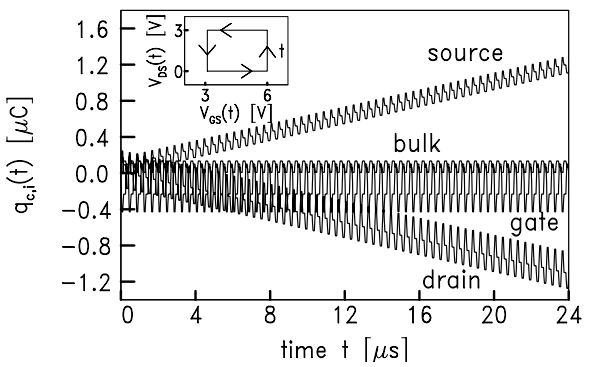

Fig. 6. Integral of the charging current through the drain- source-, gate- and bulk terminal of a laterally non-uniform MOSFET with a diffused doping profile according to (1) with $D = 2.78$, for 60 closed voltage cycles in time according to the inset ($t_{\rm cycle} = 0.4$ μs), obtained using the segmentation model.

valid for $0 < x < L$, where W is the width of the device, L is its length, μ the electron mobility, $Q_{\rm inv}$ the inversion charge per unit area, and $V = V(x,t)$ is the quasi-Fermi potential. With the source terminal positioned at $x = 0$ and the drain terminal at $x = L$, the boundary conditions for the quasi-Fermi potential are

$$V(0,t) = V_{\rm SB}(t), \qquad V(L,t) = V_{\rm DB}(t). \tag{7}$$

Under the assumption of no leakage currents, the gate current $I_{\rm G} = I_{\rm G}(t)$ is given by

$$I_{\rm G} = -W\frac{\rm d}{{\rm d}t}\left\{\int_0^L Q_{\rm tot}\,{\rm d}x\right\}, \tag{8}$$

where $Q_{\rm tot} = Q_{\rm inv} + Q_{\rm bulk}$ represents the total charge per unit area underneath the oxide, with $Q_{\rm bulk}$ the sum of the depletion- and accumulation charge per unit area. In the model a charge-sheet approach based on surface-potential formulations is taken. The surface potential $\psi_{\rm s}$ is determined in terms of the gate-bulk bias $V_{\rm GB}$ and the quasi-Fermi potential V from Poisson's equation and Gauss' law according to [17].

In case the MOSFET has a diffused doping profile, the doping concentration N_A is dependent on the lateral position x along the channel; see (1). As a result, the inversion charge and the total charge can be written as

$$Q_{\rm inv} = Q_{\rm inv}\left(V, V_{\rm GB}, x\right), \qquad Q_{\rm tot} = Q_{\rm tot}\left(V, V_{\rm GB}, x\right), \tag{9}$$

i.e., with an *explicit* dependence on the lateral position x. For reasons of simplicity, we assume that the electron mobility does not depend on the doping concentration, and we neglect mobility reduction due to the longitudinal- and transversal electrical field. We remark that the approach can be extended to also include the mobility effects. For instance, the electron mobility can be taken dependent on the doping concentration N_A [18], so that it also becomes explicitly dependent on the lateral position x. Furthermore, mobility reduction due to the electrical fields can be incorporated through a dependence on the effective, global longitudinal- and transversal electrical field [12], so that it becomes explicitly dependent on the terminal voltages. Subsequently, the small-signal analysis for

determination of the capacitances can be elaborated analogously as has been done here for a uniform and constant mobility.

To determine the capacitances, we apply small-signal voltages to the terminals of the device according to

$$\begin{aligned} V_{\rm GB}(t) &= \overline{V}_{\rm GB} + \overline{v}_{\rm GB}\,{\rm e}^{j\omega t},\\ V_{\rm DB}(t) &= \overline{V}_{\rm DB} + \overline{v}_{\rm DB}\,{\rm e}^{j\omega t},\\ V_{\rm SB}(t) &= \overline{V}_{\rm SB} + \overline{v}_{\rm SB}\,{\rm e}^{j\omega t}, \end{aligned} \tag{10}$$

for given stationary gate-bulk bias $\overline{V}_{\rm GB}$, drain-bulk bias $\overline{V}_{\rm DB}$ and source-bulk bias $\overline{V}_{\rm SB}$, and small-signal amplitudes $\overline{v}_{\rm GB}$, $\overline{v}_{\rm DB}$ and $\overline{v}_{\rm SB}$. Here, $\omega = 2\pi f$ is the angular frequency. Due to the perturbation, the drain-to-source current, the gate current and the quasi-Fermi potential are perturbed according to

$$\begin{aligned} I(x,t) &= \overline{I}(x) + [i_1(x) + j\,\omega\, i_2(x)]\ {\rm e}^{j\omega t},\\ V(x,t) &= \overline{V}(x) + [v_1(x) + j\,\omega\, v_2(x)]\ {\rm e}^{j\omega t},\\ i_{\rm G}(t) &= \overline{I}_{\rm G} + [i_{\rm G1} + j\,\omega\, i_{\rm G2}]\ {\rm e}^{j\omega t}, \end{aligned} \tag{11}$$

where the variables with a bar correspond to the dc-solution. This dc-solution is given by

$$\begin{cases} \overline{I} = -W\,\mu\, Q_{\rm inv}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\ \dfrac{{\rm d}\overline{V}(x)}{{\rm d}x},\\ \dfrac{{\rm d}\overline{I}(x)}{{\rm d}x} = 0, \end{cases} \tag{12}$$

with boundary conditions $\overline{V}(0) = \overline{V}_{\rm SB}$ and $\overline{V}(L) = \overline{V}_{\rm DB}$, and the dc-gate current equal to zero, i.e.

$$\overline{I}_{\rm G} = 0. \tag{13}$$

Substitution of (11) into (6) and (8) yields, after subtraction of the dc-solution and under neglect of the higher-order terms in v_1, v_2 and $\overline{v}_{\rm GB}$, the following 6 equations for the 6 unknowns i_1, i_2, v_1 , v_2, $i_{\rm G1}$ and $i_{\rm G2}$,

$$\begin{cases} i_1(x) = -W\,\mu\,\left[Q_{\rm inv}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\dfrac{{\rm d}v_1(x)}{{\rm d}x}\right.\\ \qquad\qquad + v_1(x)\,\dfrac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\dfrac{{\rm d}\overline{V}(x)}{{\rm d}x}\\ \qquad\qquad \left. + \overline{v}_{\rm GB}\,\dfrac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\dfrac{{\rm d}\overline{V}(x)}{{\rm d}x}\right],\\ \dfrac{{\rm d}i_1(x)}{{\rm d}x} = 0, \end{cases} \tag{14}$$

$$\begin{cases} i_2(x) = -W\,\mu\,\left[Q_{\rm inv}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\dfrac{{\rm d}v_2(x)}{{\rm d}x}\right.\\ \qquad\qquad \left. + v_2(x)\,\dfrac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\dfrac{{\rm d}\overline{V}(x)}{{\rm d}x}\right],\\ \dfrac{{\rm d}i_2(x)}{{\rm d}x} = W\,\left[v_1(x)\,\dfrac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\right.\\ \qquad\qquad \left. + \overline{v}_{\rm GB}\,\dfrac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\right]. \end{cases} \tag{15}$$

$$\begin{cases} i_{\rm G1} = 0,\\ i_{\rm G2} = -W\,\displaystyle\int_0^L \left[v_1(x)\,\frac{\partial Q_{\rm tot}}{\partial V}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\right.\\ \qquad\qquad \left. + \overline{v}_{\rm GB}\,\dfrac{\partial Q_{\rm tot}}{\partial V_{\rm GB}}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\right]{\rm d}x. \end{cases} \tag{16}$$

Notice that $O(\omega^2)$-terms have been neglected, which corresponds to the quasi-static approximation. Thus, the small-signal currents are dependent on the dc-solution. The boundary condition (7) transfers into

$$\begin{aligned} v_1(0) &= \overline{v}_{\rm SB}, & v_1(L) &= \overline{v}_{\rm DB},\\ v_2(0) &= 0, & v_2(L) &= 0. \end{aligned} \tag{17}$$

In the Appendix the solution of (14)-(16) for i_1, i_2, v_1 , v_2, $i_{\rm G1}$ and $i_{\rm G2}$, under boundary condition (17) is given.

The real part i_1 of the small-signal current represents the conductances. From the imaginary parts of the small-signal currents, the capacitances are determined, as follows:
For $C_{i\rm G}$, $i = {\rm D, G, S, B}$: $\overline{v}_{\rm DB} = \overline{v}_{\rm SB} = 0$:

$$\begin{aligned} &C_{\rm DG} = -\frac{i_2(L)}{\overline{v}_{\rm GB}}, \quad C_{\rm SG} = \frac{i_2(0)}{\overline{v}_{\rm GB}}, \quad C_{\rm GG} = \frac{i_{\rm G2}}{\overline{v}_{\rm GB}},\\ &C_{\rm BG} = C_{\rm GG} - C_{\rm DG} - C_{\rm SG}. \end{aligned} \tag{18}$$

For $C_{i\rm D}$, $i = {\rm D, G, S, B}$: $\overline{v}_{\rm GB} = \overline{v}_{\rm SB} = 0$

$$\begin{aligned} &C_{\rm DD} = \frac{i_2(L)}{\overline{v}_{\rm DB}}, \quad C_{\rm SD} = \frac{i_2(0)}{\overline{v}_{\rm DB}}, \quad C_{\rm GD} = -\frac{i_{\rm G2}}{\overline{v}_{\rm DB}},\\ &C_{\rm BD} = C_{\rm DD} - C_{\rm SD} - C_{\rm GD} \end{aligned} \tag{19}$$

For $C_{i\rm S}$, $i = {\rm D, G, S, B}$: $\overline{v}_{\rm GB} = \overline{v}_{\rm DB} = 0$

$$\begin{aligned} &C_{\rm DS} = -\frac{i_2(L)}{\overline{v}_{\rm SB}}, \quad C_{\rm SS} = -\frac{i_2(0)}{\overline{v}_{\rm SB}}, \quad C_{\rm GS} = -\frac{i_{\rm G2}}{\overline{v}_{\rm SB}},\\ &C_{\rm BS} = C_{\rm SS} - C_{\rm DS} - C_{\rm GS} \end{aligned} \tag{20}$$

For $C_{i\rm B}$, $i = {\rm D, G, S, B}$:

$$\begin{aligned} &C_{\rm DB} = C_{\rm DD} - C_{\rm DG} - C_{\rm DS}, \quad C_{\rm SB} = C_{\rm SS} - C_{\rm SG} - C_{\rm SD},\\ &C_{\rm GB} = C_{\rm GG} - C_{\rm GD} - C_{\rm GS}, \quad C_{\rm BB} = C_{\rm BS} + C_{\rm BG} + C_{\rm BD}. \end{aligned} \tag{21}$$

Finally, we show how the lateral non-uniformity influences the capacitances in comparison to those obtained via the classical Ward-Dutton charge partitioning scheme. To that end, we consider, without loss of generality, a perturbation at the gate terminal. Since the perturbation is in time, the term between square brackets in (32) satisfies

$$\begin{aligned} &v_1(x)\,\frac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right) + \overline{v}_{\rm GB}\,\frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}\left(\overline{V}(x), \overline{V}_{\rm GB}, x\right)\\ &\qquad = \frac{\rm d}{{\rm d}\,{\rm e}^{j\,\omega\, t}}\left\{Q_{\rm inv}\left(V(x,t), V_{\rm GB}(t), x\right)\right\}\\ &\qquad = \overline{v}_{\rm GB}\,\frac{\rm d}{{\rm d}V_{\rm GB}(t)}\left\{Q_{\rm inv}\left(V(x,t), V_{\rm GB}(t), x\right)\right\}, \end{aligned} \tag{22}$$

under neglect of higher-order terms. Substitution of (22) into (32), with the time-dependent potentials replaced by the stationary ones, yields by use of (18) for the source- and drain

related capacitances

$$C_{\rm SG} = \frac{W\,\mu}{L}\int_0^L \frac{v_2(x)}{\overline{v}_{\rm GB}}\,\frac{\partial Q_{\rm inv}}{\partial x}\left(\overline{V}_{\rm dc},\overline{V}_{\rm GB},x\right)\mathrm{d}x$$
$$-\frac{\mathrm{d}}{\mathrm{d}\overline{V}_{\rm GB}}\left\{W\int_0^L\left(1-\frac{x}{L}\right)Q_{\rm inv}\left(\overline{V}_{\rm dc},\overline{V}_{\rm GB},x\right)\mathrm{d}x\right\}$$
$$C_{\rm DG} = -\frac{W\,\mu}{L}\int_0^L \frac{v_2(x)}{\overline{v}_{\rm GB}}\,\frac{\partial Q_{\rm inv}}{\partial x}\left(\overline{V}_{\rm dc},\overline{V}_{\rm GB},x\right)\mathrm{d}x$$
$$-\frac{\mathrm{d}}{\mathrm{d}\overline{V}_{\rm GB}}\left\{W\int_0^L\frac{x}{L}\,Q_{\rm inv}\left(\overline{V}_{\rm dc},\overline{V}_{\rm GB},x\right)\mathrm{d}x\right\}, \tag{23}$$

where we have written $\overline{V}_{\rm dc} = \overline{V}_{\rm dc}\left(x,\overline{V}_{\rm GB}\right) = \overline{V}(x)$ to refer to the dependency of $\overline{V}(x)$ on $\overline{V}_{\rm GB}$. Since for a laterally non-uniform MOS device $\partial Q_{\rm inv}/\partial x \neq 0$, the first term in the right-hand side of (23) thus represents the correction to the capacitances obtained from the classical Ward-Dutton charge partitioning scheme.

To determine the gate- and bulk related capacitances for a perturbation at the gate terminal, we notice that (22) also holds for the depletion and accumulation charge $Q_{\rm bulk}$ as well as for the total charge $Q_{\rm tot}$. As a result, by use of (16) and (18) we obtain for the gate- and bulk related capacitances

$$C_{\rm GG} = \frac{\mathrm{d}}{\mathrm{d}\overline{V}_{\rm GB}}\left\{-W\int_0^L Q_{\rm tot}\left(\overline{V}_{\rm dc},\overline{V}_{\rm GB},x\right)\mathrm{d}x\right\},$$
$$C_{\rm BG} = -\frac{\mathrm{d}}{\mathrm{d}\overline{V}_{\rm GB}}\left\{W\int_0^L Q_{\rm bulk}\left(\overline{V}_{\rm dc},\overline{V}_{\rm GB},x\right)\mathrm{d}x\right\}. \tag{24}$$

Thus, the terms between brackets in (24) are the terminal gate- and bulk charge $Q_{\rm G}$ and $Q_{\rm B}$, respectively, from which the corresponding capacitances can be derived. Notice that the lateral non-uniformity is included via the dependence on the lateral position.

VI. Incorporation of a Capacitance Model into Circuit Simulators

Conventional circuit simulators are based on terminal charge models. However, in Sec. IV we have shown that for laterally non-uniform MOS devices no terminal charge model exists. Therefore, we have developed a method to implement the capacitance model directly into these circuit simulators; see Fig. 7. In [10] we have shown for a three-terminal device with a laterally diffused doping profile that this method indeed yields for a closed voltage cycle in time a non-zero charging current through the source- and drain terminal and a zero charging current through the gate terminal. Furthermore, we have shown in [10] that this method yields exactly the same results as a circuit simulation using the segmentation approach. Thus, capacitance models can be successfully implemented into conventional charge-based circuit simulators.

VII. Results

In this section the capacitances calculated from the model equations of Sec. V are shown in comparison to those obtained from high-frequency measurements (Figs. 8 and 9), 2-D device simulations (Figs. 10 and 11), and circuit simulations using the segmentation approach (Figs. 12 and 13). For more plots showing the comparison with 2-D device simulations and circuit simulations using the segmentation approach we refer to [10]. In the model, a diffused doping profile according to (1) is taken. In this way, $D = 0$ corresponds to the uniform case, while $D > 0$ represents a device with a laterally diffused doping profile decreasing from source to drain.

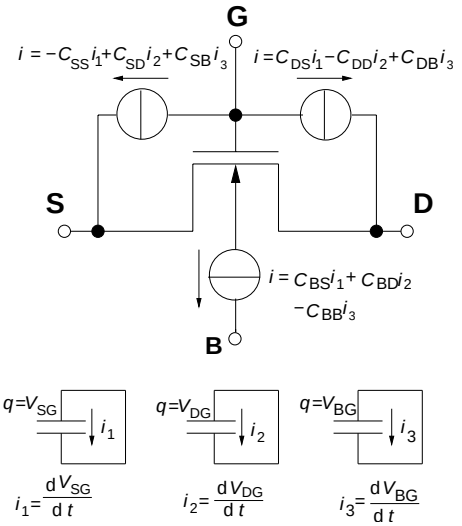

Fig. 7. Equivalent circuit for a MOS device illustrating the method to implement a capacitance model into circuit simulators.

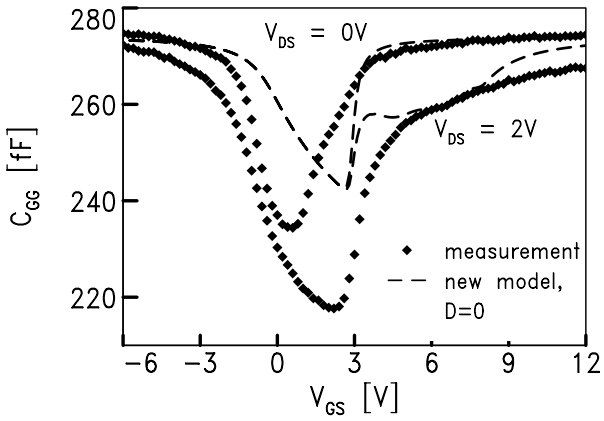

Fig. 8. Measured (symbols) gate-gate capacitance of a MOSFET with a diffused doping profile, for $V_{\rm DS} = 0$ and 2 V. The dashed line represents the simulated capacitance of a uniform MOSFET ($D = 0$), using the new model.

In Figs. 8 and 9 measurements are shown of a conventional MOSFET (thus without drift region) but with a diffused doping profile. The measurements were performed on dedicated test structures, by use of an S-parameter analyzer at a frequency of $f = 1$ GHz. The device has an oxide thickness of 40 nm, and a threshold voltage of about 3 V. In Fig. 8 we observe that the model with a uniform doping ($D = 0$) does not adequately predict the measured capacitance values. The plot reveals that especially in depletion the diffused doping profile has a strong impact on these capacitance values. In Fig. 9, on the other hand, we observe that the new model for a laterally

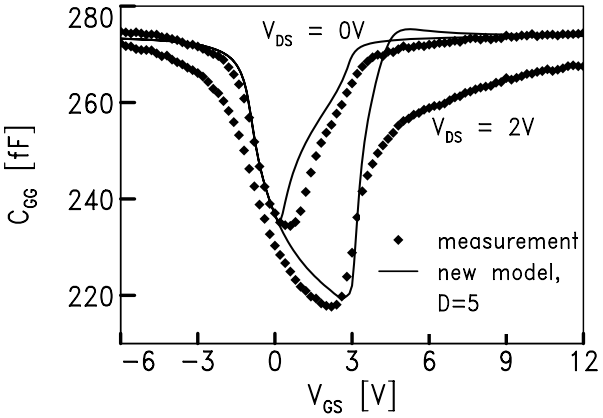

Fig. 9. Comparison of the gate-gate capacitance of a MOSFET with a diffused doping profile, between measurements (symbols) and the new model (solid lines) with $D = 5$.

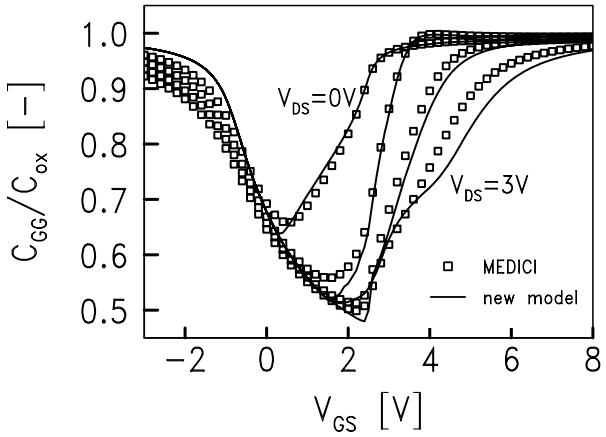

Fig. 11. Normalised gate-gate capacitance of the new model (solid lines) compared to device simulations (symbols), for $V_{\rm DS} = 0$, 1, 2 and 3 V. The device has a laterally diffused doping profile with $D = 2.78$.

non-uniform MOSFET with $D = 5$ accurately describes the effect of the diffused doping profile. In strong inversion for $V_{\rm DS} = 2$ V, however, the model over-estimates the measured capacitance. Possible reasons are the neglect of mobility reduction due to the longitudinal and transversal fields, and the assumption that the electron mobility is independent of the doping concentration.

To omit the mobility effects, we compare the new capacitance model with 2D-device simulations (using MEDICI) in which we take a constant and uniform mobility. In Figs. 10 and 11 we observe that the capacitances obtained from the new model compare very well to the ones obtained from the device simulations, for both a laterally non-uniform device and a uniform device. Furthermore, in Fig. 10 the influence of the diffused doping profile is clearly seen: With the maximum value of $C_{\rm DG}$ equal to $0.5 \times C_{\rm ox}$ for the uniform device, but equal to $0.7 \times C_{\rm ox}$ for the laterally non-uniform device, an increase of about 40% in maximum drain-gate capacitance is obtained due to the lateral non-uniformity.

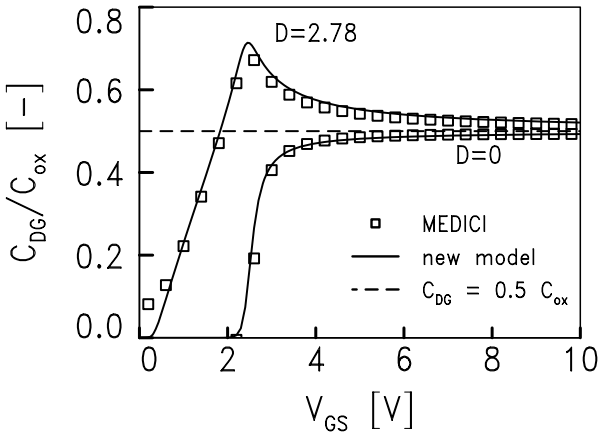

Fig. 10. Comparison of the normalized drain-gate capacitance between MEDICI device simulations (symbols) and the new model (solid lines), for $V_{\rm DS} = 0$ V. Results are shown for a laterally diffused doping profile ($D = 2.78$) and a uniform doping profile ($D = 0$).

To exclude possible 2D-effects and make a one-to-one comparison, we finally compare the new capacitance model with circuit simulations using the segmentation approach. In Figs. 12 and 13 we observe that the capacitances obtained from the new model compare very well to the ones obtained from the segmentation model, for both a laterally non-uniform device and a uniform device. Furthermore, in Fig. 12 the influence of the diffused doping profile is clearly seen: The lateral non-uniformity causes the maximum value of $C_{\rm DD}$ to exceed above the total oxide capacitance, up to a value of $1.3 \times C_{\rm ox}$.

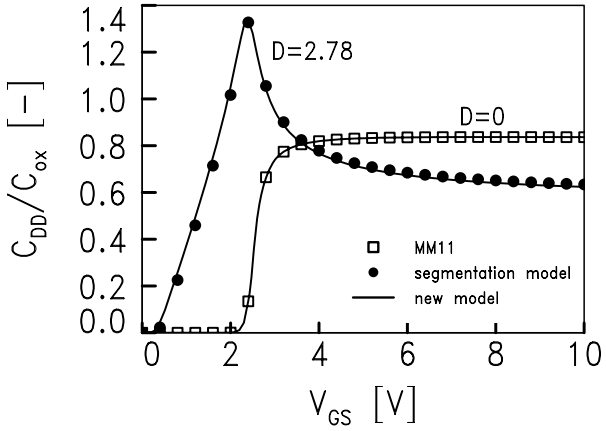

Fig. 12. Normalised drain-drain capacitance for $V_{\rm DS} = 0$ V, obtained by the new model (solid lines) in comparison to MOS Model 11 for the uniform case ($D = 0$), and to the segmentation model for a laterally diffused doping profile ($D = 2.78$), both represented by the symbols.

VIII. Conclusions

In this paper, we have shown that laterally non-uniform channel doping profiles in, for instance, LDMOS devices lead to a capacitance behavior that is fundamentally different from that of MOSFETs with uniform channels. Furthermore, we have demonstrated that for these devices as a consequence of the lateral non-uniformity, no terminal source- and drain charge exists. Therefore, we have derived for MOS devices with a laterally non-uniform channel doping profile a capacitance model. This model is based on surface-potential

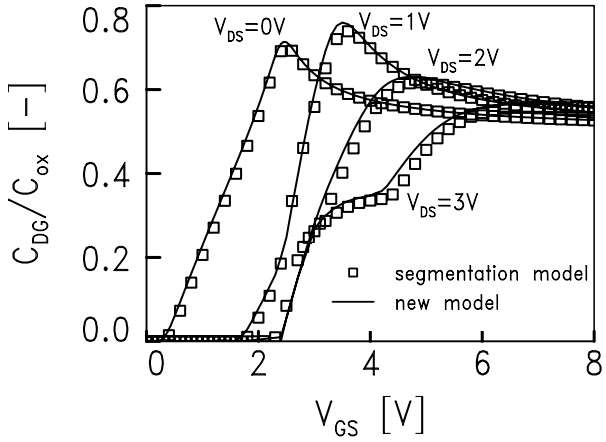

Fig. 13. Normalised drain-gate capacitance of the new model (solid lines) compared to segmentation model (symbols), for a diffused doping profile according to (1) with $D = 2.78$.

formulations. Next, we have presented a method to implement the capacitance model into standard charge-based circuit simulators. Finally, a comparison with 2-D device simulations and a segmentation model demonstrates that for a constant mobility the typical capacitance behavior of laterally non-uniform MOS devices is accurately predicted by the capacitance model. A comparison with high-frequency measurements shows for low drain-source bias conditions a good agreement in all regimes ranging from accumulation and depletion to strong inversion. At elevated drain-source voltages, however, the model agrees less in strong inversion, which is is ascribed to the simplifications made in the model for the electron mobility.

APPENDIX

The solution of (14) for v_1 and i_1 is given by

$$\begin{aligned} i_1(x) &= \frac{W\,\mu\,C'_{\rm ox}}{L}\,C, \\ v_1(x) &= \mathrm{e}^{\Gamma(x)}\,\left(\overline{v}_{\rm SB} + C\;T(x) - \overline{v}_{\rm GB}\,S(x)\right), \end{aligned} \tag{25}$$

where the functions Γ, T and S are given by

$$\begin{aligned} \Gamma(x) &= -\int_0^x \frac{\frac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(s),\overline{V}_{\rm GB},s\right)}{Q_{\rm inv}\left(\overline{V}(s),\overline{V}_{\rm GB},s\right)}\frac{\mathrm{d}\overline{V}(s)}{\mathrm{d}s}\,\mathrm{d}s, \\ T(x) &= -\frac{C'_{\rm ox}}{L}\int_0^x \frac{\mathrm{e}^{-\Gamma(s)}}{Q_{\rm inv}\left(\overline{V}(s),\overline{V}_{\rm GB},s\right)}\,\mathrm{d}s, \\ S(x) &= \int_0^x \frac{\frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}\left(\overline{V}(s),\overline{V}_{\rm GB},s\right)}{Q_{\rm inv}\left(\overline{V}(s),\overline{V}_{\rm GB},s\right)}\frac{\mathrm{d}\overline{V}(s)}{\mathrm{d}s}\,\mathrm{e}^{-\Gamma(s)}\,\mathrm{d}s. \end{aligned} \tag{26}$$

and the constant C is determined from the boundary condition $v_1(L) = \overline{v}_{\rm DB}$, i.e.

$$C = \frac{1}{T(L)}\left(\overline{v}_{\rm DB}\,\mathrm{e}^{-\Gamma(L)} - \overline{v}_{\rm SB} + \overline{v}_{\rm GB}\,S(L)\right). \tag{27}$$

The solution of (15) for v_2 is given by

$$v_2(x) = \mathrm{e}^{\Gamma(x)}\,u_2(x), \tag{28}$$

where u_2, under boundary condition $u_2(0) = 0$, is given by

$$\begin{aligned} -\frac{C'_{\rm ox}}{L}\,u_2(x) &= Q_{\rm inv}\left(\overline{V}(0),\overline{V}_{\rm GB},0\right)\;u'_2(0)\,T(x) \\ &-\frac{T(x)}{\mu}\int_0^x\left[v_1(s)\,\frac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(s),\overline{V}_{\rm GB},s\right)\right. \\ &\left.+\,\overline{v}_{\rm GB}\,\frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}\left(\overline{V}(s),\overline{V}_{\rm GB},s\right)\right]\left(1-\frac{T(s)}{T(x)}\right)\mathrm{d}s. \end{aligned} \tag{29}$$

The value $u'_2(0)$ is determined from the boundary condition $u_2(L) = 0$. Thus, by combining (25)-(29) with (15) and (16), we have determined the small-signal quasi-Fermi potentials v_1 and v_2, and the small-signal currents i_1, i_2, $i_{\rm G1}$ and $i_{\rm G2}$.

For the derivation of the capacitances we determine the imaginary parts $i_2(0)$ and $i_2(L)$ of the small-signal currents at the source- and drain side. To that end, we integrate the second equation of (15) twice with respect to x, and obtain

$$\begin{aligned} i_2(0) &= \frac{1}{L}\int_0^L i_2(x)\mathrm{d}x \\ &-W\int_0^L\left(1-\frac{x}{L}\right)\left[v_1(x)\,\frac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right. \\ &\left.+\,\overline{v}_{\rm GB}\,\frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right]\mathrm{d}x, \\ i_2(L) &= \frac{1}{L}\int_0^L i_2(x)\mathrm{d}x \\ &+W\int_0^L\frac{x}{L}\left[v_1(x)\,\frac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right. \\ &\left.+\,\overline{v}_{\rm GB}\,\frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right]\mathrm{d}x. \end{aligned} \tag{30}$$

Subsequently, with the first equation of (15) rewritten as

$$\begin{aligned} i_2(x) = -W\,\mu\left[\frac{\mathrm{d}}{\mathrm{d}x}\left\{v_2(x)\,Q_{\rm inv}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right\}\right. \\ \left.-v_2(x)\frac{\partial Q_{\rm inv}}{\partial x}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right], \end{aligned} \tag{31}$$

substitution of (31) into (30) yields, under the boundary condition $v_2(0) = v_2(L) = 0$,

$$\begin{aligned} i_2(0) &= \frac{W\,\mu}{L}\int_0^L v_2(x)\,\frac{\partial Q_{\rm inv}}{\partial x}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\mathrm{d}x \\ &-W\int_0^L\left(1-\frac{x}{L}\right)\left[v_1(x)\,\frac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right. \\ &\left.+\,\overline{v}_{\rm GB}\,\frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right]\mathrm{d}x \\ i_2(L) &= \frac{W\,\mu}{L}\int_0^L v_2(x)\,\frac{\partial Q_{\rm inv}}{\partial x}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\mathrm{d}x \\ &+W\int_0^L\frac{x}{L}\left[v_1(x)\,\frac{\partial Q_{\rm inv}}{\partial V}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right. \\ &\left.+\,\overline{v}_{\rm GB}\,\frac{\partial Q_{\rm inv}}{\partial V_{\rm GB}}\left(\overline{V}(x),\overline{V}_{\rm GB},x\right)\right]\mathrm{d}x. \end{aligned} \tag{32}$$

Notice that in a laterally non-uniform MOS device $\partial Q_{\rm inv}/\partial x \neq 0$, so that the first terms of (32) do not vanish.

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