Research Article
New Proposal for MCML Based Three-Input Logic Implementation

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This paper presents a new proposal for three-input logic function implementation in MOS current mode logic (MCML) style. The conventional realization of such logic employs three levels of stacked source-coupled transistor pairs. It puts restriction on minimum power supply requirement and results in increased static power. The new proposal presents a circuit element named as quad-tail cell which reduces number of stacked source-coupled transistor levels by two. A three-input exclusive-OR (XOR) gate, a vital element in digital system design, is chosen to elaborate the approach. Its behavior is analyzed and SPICE simulations using TSMC 180 nm CMOS technology parameters are included to support the theoretical concept. The performance of the proposed circuit is compared with its counterparts based on CMOS complementary pass transistor logic, conventional MCML, and cascading of existing two input tripple-tail XOR cells and applying triple-tail concept in conventional MCML topology. It is found that the proposed XOR gate performs best in terms of most of the performance parameters. The sensitivity of the proposed XOR gate towards process variation shows a variation of 1.54 between the best and worst case. As an extension, a realization of 4 : 1 multiplexer has also been included.

1. Introduction

MCML style finds application in communication systems, optical fiber links, digital to analog converter, microprocessors, and signal processors [1–3]. As compared to static CMOS logic, MCML has several advantageous features such as improved signal integrity, reduced power consumption, better power delay product at high frequencies, stability with technology generations, and improved security in cryptography applications [4–9]. A MCML gate consists of three main parts, namely, a pull down network (PDN), a current source, and a load. The PDN implements the logic function; the current source generates the constant bias current while the load performs the current-to-voltage conversion.

The logic function is realized using series-gating approach which suggests stacking of the source-coupled transistors pairs in the PDN. The number of stacked levels has a direct correspondence with number of inputs in the logic function. As the number of inputs becomes larger, there is increase in the number of stacked levels (NSL). For proper operation of MCML gate, a minimum power supply is required which is decided by the value of NSL and higher NSL result in larger minimum power supply. This serves as a main motivation behind using low voltage topology as lower power supply will result in reduced power consumption since the latter is computed as the product of bias current and power supply. Few low voltage techniques are available in the open literature [10–16]. The techniques [10–13] provide single ended output. A NOR based logic realization is proposed in [10, 11] to avoid stacking but it requires multistage realization of logic function. Additional current mirror, voltage, and current source are employed in [12, 13] to avoid stacking. The triple-tail cell concept is introduced in [14–16] to reduce NSL by one for the two-level MCML gates implementation. This paper introduces a new methodology for reducing the value of NSL by two and presents a quad-tail cell for this purpose. This method therefore allows three-input logic function realization using single level of source-coupled pairs and ultimately resulting in significant reduction in minimum power supply. A total of four proposed quad-tail
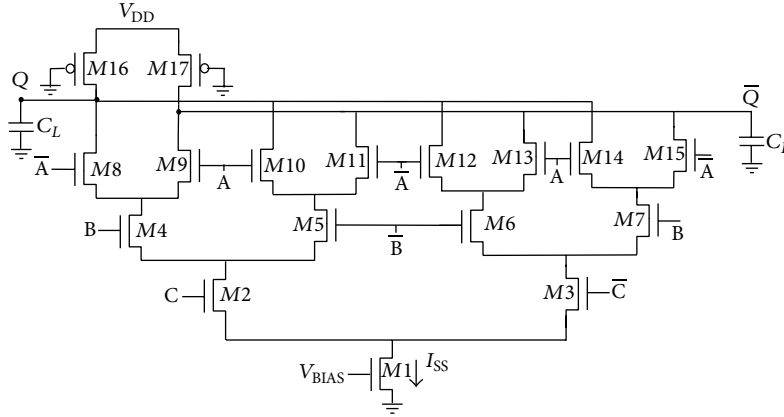
FIGURE 1: Conventional three-input MCML XOR gate.

cells are used for three-input logic function. The outlined method is generic in nature and can be applied to realize any three-input function.

The paper first discusses the basic realization of the three-input logic function in MCML style in Section 2. XOR gate is chosen for the purpose. Thereafter, Section 3 presents the new quad-tail cell put forward and its usefulness is illustrated through MCML XOR gate realization. The operation of the proposed XOR gate is explained and analytical formulations for the minimum power supply and voltage swing are put forward. Its performance comparison with the CMOS complementary pass transistor logic (CPL) based XOR gate, traditional MCML topology, and the two additional topologies is included in Section 4. A discussion on the general approach for implementing complex logic function in MCML style is also included. Extensive SPICE simulations are carried out to validate the proposed theory. Section 5 concludes the paper.

2. Conventional Three-Input MCML Gate Realization

The basic architecture of MCML gate consists of a pull down network (PDN), a current source, and a load as shown in Figure 1(a). The PDN implements the logic function, the current source maintains a constant bias current, and the load performs the current-to-voltage conversion [4]. The gate works on the principle of current steering. Depending upon the inputs, the bias current is steered to one of the output branches and produces the output accordingly. The logic function is realized by using series-gating approach [17]. It is a systematic and a general approach wherein a logic function is implemented as a network of source-coupled transistor pairs having all transistor paths associated with the possible input combinations and then properly connecting each of the upper drain nodes to the output nodes. Based on this, the schematic of MCML XOR gate with differential inputs A, B, and C is shown in Figure 1. The PDN has three levels of source-coupled transistor pairs ($M2$–$M15$), the load transistors ($M16$, $M17$), and a constant current source $M1$ that generates the bias current I_{SS}. The differential inputs A, B, and

C drive the uppermost ($M8$–$M15$), middle ($M4$–$M7$), and lowest ($M2$-$M3$) levels, respectively. Consider, for instance, that all the inputs are high. Under this condition, the bias current is steered in transistors $M2$, $M4$, and $M9$ such that high and low voltages are obtained at the nodes Q and $\overline{Q}$ through the load transistors.

The minimum supply voltage $V_{\text{DD\_MIN\_CON}}$ for the gate (Figure 1) is defined as the lowest voltage at which all the transistors in the three levels and the current source operate in the saturation region [18] and is computed as

$$V_{\text{DD\_MIN\_CON}} = 4V_{\text{BIAS}} - 3V_{\text{T}}, \tag{1a}$$

where V_{T} is the threshold voltage of the transistors $M1$–$M15$ and V_{BIAS} is the biasing voltage of $M1$.

The voltage swing of the MCML gate is determined as the difference between the high and the low differential output voltages and is evaluated as

$$V_{\text{SWING\_CON}} = 2I_{\text{SS}}R_{\text{P\_CON}}, \tag{1b}$$

where $R_{\text{P\_CON}}$ represents the resistance of the PMOS load transistors operating in the linear region [17].

3. The Proposal

A new approach to realize three-input MCML gate is presented in this section. The realization employs a novel circuit element named quad-tail cell to reduce the number of source-coupled transistor levels.

3.1. Quad-Tail Cell. A quad-tail cell is an extension of the triple-tail cell concept [14–16] and consists of four source-coupled transistors ($M1$–$M4$) as shown in Figure 2. In the cell, the activation/deactivation of the two outer transistors ($M1$, $M2$) is controlled by the two internal transistors ($M3$, $M4$). To elaborate this, consider when either one input among Y and Z is high or both these inputs assume high value. Under these circumstances, the current I_{SS} is steered through transistors $M3$ or/and $M4$; and the transistors $M1$ and $M2$ remain deactivated. Conversely, if both the inputs Y and Z are low, the current I_{SS} will steer to one of the two transistors
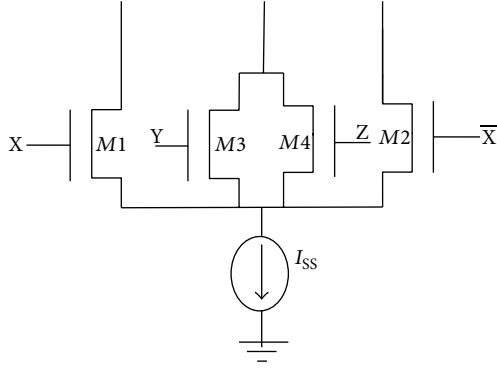
FIGURE 2: Proposed quad-tail cell.

($M1$, $M2$) depending upon the value of the input X. The requirement for the proper activation/deactivation of the quad-tail cell is similar to triple-tail cell; that is, the aspect ratio of internal transistors $M3$ and $M4$ should be larger than the others by a factor of N.

3.2. Proposed XOR Gate.

A three-input XOR gate is considered to illustrate the use of quad-tail cell and its complete schematic is shown in Figure 3. It uses four quad-tail cells ($Q1$–$Q4$) each biased by current source of $I_{SS}/4$ value. The inputs connection to the internal transistors of the quad-tail cells is done in a manner so that at any instance of time the outermost transistors in only one quad-tail cell get activated. To elaborate this further, consider that all the inputs A, B, and C are high. In this condition, the outermost transistors of only $Q1$ are activated while, for the rest ($Q2$–$Q4$), the bias current is steered to the internal transistors making deactivation of corresponding outermost transistors.

The minimum supply voltage, $V_{DD\_MIN\_QC}$, for the proposed three-input MCML XOR gate, using the method outlined in [18], is computed as

$$V_{DD\_MIN\_QC} = 2V_{BIAS} - V_T, \qquad (2)$$

where V_T is the threshold voltage of transistors $M1$–$M12$ and V_{BIAS} is the biasing voltage of $M1$–$M4$.

The voltage swing (V_{SWING}) of a MCML gate is defined as the difference of high differential output voltage (V_{OH}) and the low differential output voltage (V_{OL}) [17]. By analyzing the circuit, the differential output voltage ($V_Q - \overline{V_Q}$) for the proposed XOR gate can be calculated as

$$V_Q - \overline{V_Q} = R_P \left[(i_{D,6} + i_{D,8} + i_{D,10} + i_{D,12}) - (i_{D,5} + i_{D,7} + i_{D,9} + i_{D,11}) \right], \qquad (3)$$

where $i_{D,k}$ is the current through transistor Mk, where $k = 5$–12. The expression requires the determination of the above currents for all the input combinations. To simplify the calculations, the proposed topology is examined by simultaneously considering the input combinations of differential inputs B and C.

Case 1 (differential inputs B and C are high). In this condition, the outermost transistors of $Q1$ ($M5$-$M6$) are activated. For high value of differential input A, the transistor $M5$ is OFF and $M6$ is ON. Thus, their currents can be written as

$$i_{D,5} = 0;$$
$$i_{D,6} = \frac{I_{SS}}{4}. \qquad (4a)$$

At the same time, the quad-tail cells $Q2$–$Q4$ are deactivated via the turning ON of their respective inner transistors. But since the complete deactivation of the quad-tail cell cannot be achieved, therefore, small current still flows in the outer transistor of these cells which needs to be considered for calculating the differential output voltage. So, for given factor N, the current flowing in the transistors $M7$–$M12$ can be computed as

$$i_{D,7} = \frac{I_{SS}}{4} \frac{1}{1+N};$$
$$i_{D,8} = 0;$$
$$i_{D,9} = \frac{I_{SS}}{4} \frac{1}{1+N};$$
$$i_{D,10} = 0; \qquad (4b)$$
$$i_{D,11} = 0;$$
$$i_{D,12} = \frac{I_{SS}}{4} \frac{1}{1+2N}.$$

Substituting these current values in the output voltage expression, we get high differential output voltage (V_{OH}) as

$$V_{OH} = V_Q - \overline{V_Q} = \frac{I_{SS}}{4} \frac{N-1}{N+1} R_P. \qquad (4c)$$

Similarly, the current through transistors $M5$–$M12$, for low value of the differential input A, is given as

$$i_{D5} = \frac{I_{SS}}{4};$$
$$i_{D6} = 0;$$
$$i_{D7} = 0;$$
$$i_{D8} = \frac{I_{SS}}{4} \frac{1}{1+N};$$
$$i_{D9} = 0; \qquad (5a)$$
$$i_{D10} = \frac{I_{SS}}{4} \frac{1}{1+N};$$
$$i_{D11} = \frac{I_{SS}}{4} \frac{1}{1+2N};$$
$$i_{D12} = 0$$

leading to low differential output voltage (V_{OL}) as

$$V_{OL} = V_Q - \overline{V_Q} = -\frac{I_{SS}}{4} \frac{N-1}{N+1} R_P. \qquad (5b)$$
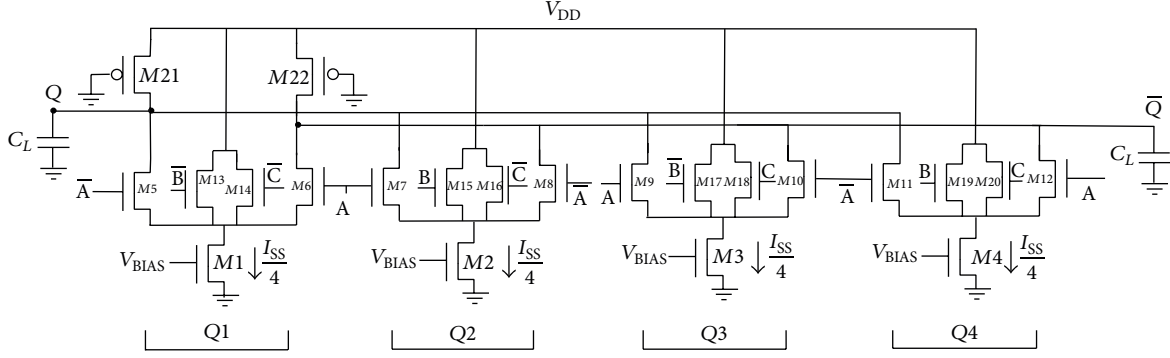
Figure 3: Proposed quad-tail cell based three-input MCML XOR gate.

Case 2 (differential inputs B and C are low). In this condition, the outer transistors ($M11$-$M12$) of Q4 are activated while those of Q1–Q3 ($M6$–$M10$) remain deactivated. For high value differential input A, the current through the transistors ($M5$–$M12$) can be written as

$$
\begin{aligned}
i_{D5} &= 0; \\
i_{D6} &= \frac{I_{SS}}{4}\frac{1}{1+2N}; \\
i_{D7} &= \frac{I_{SS}}{4}\frac{1}{1+N}; \\
i_{D8} &= 0; \\
i_{D9} &= \frac{I_{SS}}{4}\frac{1}{1+N}; \\
i_{D10} &= 0; \\
i_{D11} &= 0; \\
i_{D12} &= \frac{I_{SS}}{4}.
\end{aligned}
\tag{6a}
$$

Substituting these current values in the output voltage expression (3), we get high differential output voltage (V_{OH}) as

$$
V_{OH} = V_Q - \overline{V_Q} = \frac{I_{SS}}{4}\frac{N-1}{N+1}R_P.
\tag{6b}
$$

Similarly, for low value of the input A, the current through the transistors ($M5$–$M12$) can be written as

$$
\begin{aligned}
i_{D5} &= \frac{I_{SS}}{4}\frac{1}{1+2N}; \\
i_{D6} &= 0; \\
i_{D7} &= 0; \\
i_{D8} &= \frac{I_{SS}}{4}\frac{1}{1+N}; \\
i_{D9} &= 0; \\
i_{D10} &= \frac{I_{SS}}{4}\frac{1}{1+N}; \\
i_{D11} &= \frac{I_{SS}}{4}; \\
i_{D12} &= 0.
\end{aligned}
\tag{7a}
$$

Substituting these current values in (3), we get low differential output voltage (V_{OL}) as

$$
V_{OL} = V_Q - \overline{V_Q} = -\frac{I_{SS}}{4}\frac{N-1}{N+1}R_P.
\tag{7b}
$$

Case 3 (differential input B is high and input C is low). In this condition, the outer transistors ($M9$-$M10$) of Q3 are activated while those of Q1, Q2, and Q3 ($M5$–$M8$, $M11$-$M12$) are deactivated. For high value input A, the current through the transistors ($M5$–$M12$) can be written as

$$
\begin{aligned}
i_{D5} &= 0; \\
i_{D6} &= \frac{I_{SS}}{4}\frac{1}{1+N}; \\
i_{D7} &= \frac{I_{SS}}{4}\frac{1}{1+2N}; \\
i_{D8} &= 0; \\
i_{D9} &= \frac{I_{SS}}{4}; \\
i_{D10} &= 0; \\
i_{D11} &= 0; \\
i_{D12} &= \frac{I_{SS}}{4}\frac{1}{1+N}.
\end{aligned}
\tag{8a}
$$

Substituting these current values in the output voltage expression, we get low differential output voltage (V_{OL}) as

$$
V_{OL} = V_Q - \overline{V_Q} = -\frac{I_{SS}}{4}\frac{N-1}{N+1}R_P.
\tag{8b}
$$

Similarly, for low value of the input A, the current through the transistors ($M5$–$M12$) can be written as

$$i_{D5} = \frac{I_{SS}}{4} \frac{1}{1+N};$$

$$i_{D6} = 0;$$

$$i_{D7} = \frac{I_{SS}}{4} \frac{1}{1+2N};$$

$$i_{D8} = 0;$$

$$i_{D9} = 0; \qquad (9a)$$

$$i_{D10} = \frac{I_{SS}}{4};$$

$$i_{D11} = \frac{I_{SS}}{4} \frac{1}{1+N};$$

$$i_{D12} = 0.$$

Substituting these current values in (3), we get high differential output voltage (V_{OH}) as

$$V_{OH} = V_Q - \overline{V_Q} = \frac{I_{SS}}{4} \frac{N-1}{N+1} R_P. \qquad (9b)$$

Case 4 (differential input B is low and input C is high). In this condition, the outer transistors ($M7$-$M8$) of $Q2$ are activated while those of $Q1$, $Q3$, and $Q4$ ($M5$-$M6$, $M9$–$M12$) are deactivated. For high value input A, the current through the transistors ($M5$–$M12$) can be written as

$$i_{D5} = 0;$$

$$i_{D6} = \frac{I_{SS}}{4} \frac{1}{1+N};$$

$$i_{D7} = \frac{I_{SS}}{4};$$

$$i_{D8} = 0;$$

$$i_{D9} = \frac{I_{SS}}{4} \frac{1}{1+2N}; \qquad (10a)$$

$$i_{D10} = 0;$$

$$i_{D11} = 0;$$

$$i_{D12} = \frac{I_{SS}}{4} \frac{1}{1+N}.$$

Substituting these current values in the output voltage expression, we get low differential output voltage (V_{OL}) as

$$V_Q - \overline{V_Q} = V_{OL} = -\frac{I_{SS}}{4} \frac{N-1}{N+1} R_P. \qquad (10b)$$

Similarly, for low value of the input A, the current through the transistors ($M5$–$M12$) can be written as

$$i_{D5} = \frac{I_{SS}}{4} \frac{1}{1+N};$$

$$i_{D6} = 0;$$

$$i_{D7} = 0;$$

$$i_{D8} = \frac{I_{SS}}{4};$$

$$i_{D9} = 0; \qquad (11a)$$

$$i_{D10} = \frac{I_{SS}}{4} \frac{1}{1+2N};$$

$$i_{D11} = \frac{I_{SS}}{4} \frac{1}{1+N};$$

$$i_{D12} = 0.$$

Substituting these current values in (3), we get high differential output voltage (V_{OH}) as

$$V_{OH} = V_Q - \overline{V_Q} = \frac{I_{SS}}{4} \frac{N-1}{N+1} R_P. \qquad (11b)$$

From the above analysis, the voltage swing (V_{SWING_PG}) of the proposed gate can be determined as

$$V_{SWING\_PG} = V_{OH} - V_{OL} = \frac{I_{SS}}{2} \frac{N-1}{N+1} R_P. \qquad (12)$$

This indicates that the voltage swing of the proposed gate is smaller than the conventional MCML gate (see (1b)). So, in order to achieve the same voltage swing as the conventional MCML gate, the load resistance of the proposed gate (R_P) is increased accordingly.

4. Simulations Results and Discussion

In this section, the functionality of the proposed three-input XOR gate is verified through simulations using 180 nm CMOS technology parameters. Its performance is compared with the conventional MCML XOR topology, two more MCML XOR circuits, and CMOS complementary pass transistor (CPL) based XOR topology for the sake of fair comparison. Both the MCML topologies use triple-tail concept to lower the number of source-coupled pair levels. The first topology employs a cascade of two input XOR gates while the second realization reduces the NSL from three to two. All the XOR gates are simulated with their respective minimum power supply and load capacitance of 50 fF. The MCML topologies are designed so that the total current drawn from the power supply is 100 μA and voltage swing is 400 mV. Further, the total current drawn from the power supply per gate is retained at 100 μA for MCML topologies while maintaining voltage swing of 400 mV. The performance comparison is done on the basis of power, propagation delay, power delay product (PDP), transistor count, gate count, and switching current. The simulation of a ring oscillator based
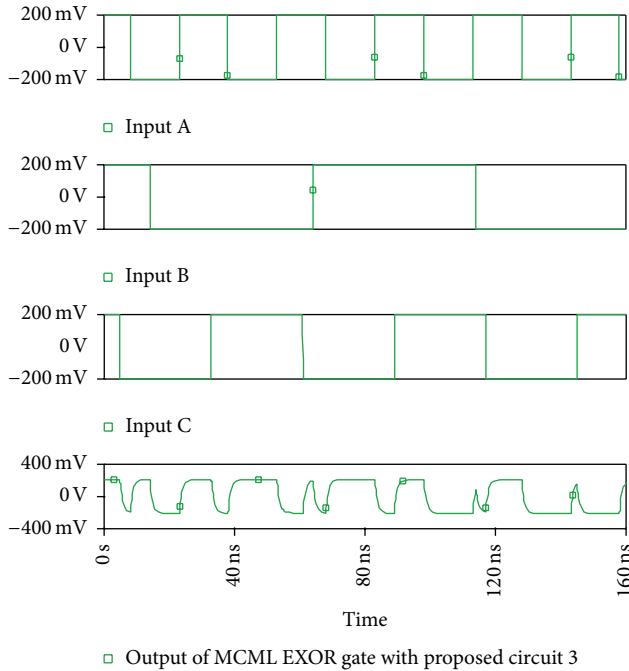
FIGURE 4: Simulation waveforms for the proposed three-input MCML XOR gate.

on the proposed and the conventional XOR gate is performed for completeness. A discussion on the general approach for implementing complex three-input logic function is included.

4.1. Functional Verification of the Proposed Circuit. The functionality of the proposed quad-tail cell based three-input MCML XOR gate is verified through simulations with simulation conditions discussed above. The timing waveforms for differential inputs A, B, and C and the corresponding differential output are shown in Figure 4. It can be observed that differential output voltage is high for all the cases having odd number of high inputs and remains low otherwise. Thus, the proposed MCML XOR gate adheres to desired functionality.

4.2. Performance Comparison. The performance of the proposed XOR gate is compared with the conventional three-input XOR gate (Figure 1). To give broader perspective, two more possible three-input XOR gate circuit realizations are also included. Both realizations use triple-tail concept to lower the number of source-coupled pair levels. The first realization is derived from the fact that the three-input XOR gate functionality can be achieved by cascading the two input XOR gates as shown in Figure 5(a). The inputs A and B are connected to XOR gate X1 while its output and the input C are fed to XOR gate X2. The recent implementation of the two input XOR gates [14–16] is chosen for implementation. The complete MOS based schematic of the three-input XOR gate is shown in Figure 5(b) and is referred to as Topology 1 in the context of the paper.

The second realization extends the triple-tail cell concept to lower the number of source-coupled pair levels from three to two. The resulting topology is shown in Figure 6 and is referred to as Topology 2 in the paper. It consists of two triple-tail cells biased by separate current sources of $I_{SS}/2$ value. The transistors at the lowest level of the conventional three-input XOR gate (Figure 1) are made the activating/deactivating transistors of the triple-tail cells. This leads to two levels of stacked source-coupled transistors in the outer branches of the triple-tail cell. The minimum supply voltage $V_{DD\_MIN\_TP2}$ for Topology 2 of the three-input MCML XOR gate can be obtained by using the method outlined in [18] as

$$V_{DD\_MIN\_TP2} = 3V_{BIAS} - 2V_T, \qquad (13)$$

where V_T is the threshold voltage of transistors $M1$–$M14$ and V_{BIAS} is the biasing voltage of $M1$-$M2$.

The performance of the proposed quad-tail cell based three-input MCML XOR gate topology is compared with MCML conventional topology Topology 1, Topology 2, and CMOS CPL based XOR topology with same input conditions. The topologies are powered by their respective minimum power supply. The simulation results are summarized in Table 1 and the following observations are made:

(i) The power supply constraint for proposed XOR gate and Topology 1 is same whereas conventional topology needs largest value and requirement for Topology 2 lies in the middle. This is a direct consequence of presence of NSL; for example, topologies (proposed topology and Topology 1) employ single level while conventional topology and Topology 2 use three and two levels, respectively.

(ii) Since all the topologies are designed to draw 100 μA current from the power supply, therefore the topologies (proposed topology and Topology 1) consume same power which is lower than the remaining two.

(iii) It is clear from above point that the topologies (proposed topology and Topology 1) consume the least power among those listed in Table 1. In terms of the propagation delay, proposed topology shows significant improvement which may be attributed to reduced number of stages. This accounts for lowest power delay product values (PDP).

(iv) Though gate count is equal for conventional topology, Topology 2, and proposed topology, the proposed topology performs best in terms of propagation delay, power, and PDP.

(v) The transistor count in proposed topology is highest among all.

(vi) The delay in MCML based conventional XOR gate and Topology 1 is comparatively higher than that in proposed topology and Topology 2. It is due to the fact that there are three stacked source-coupled transistors pair levels which contribute to large parasitic capacitance at the output node. The delay in Topology 1 is due to cascading of two XOR gates. Though the proposed topology and Topology 2 employ a single

TABLE 1: Summary of the results.

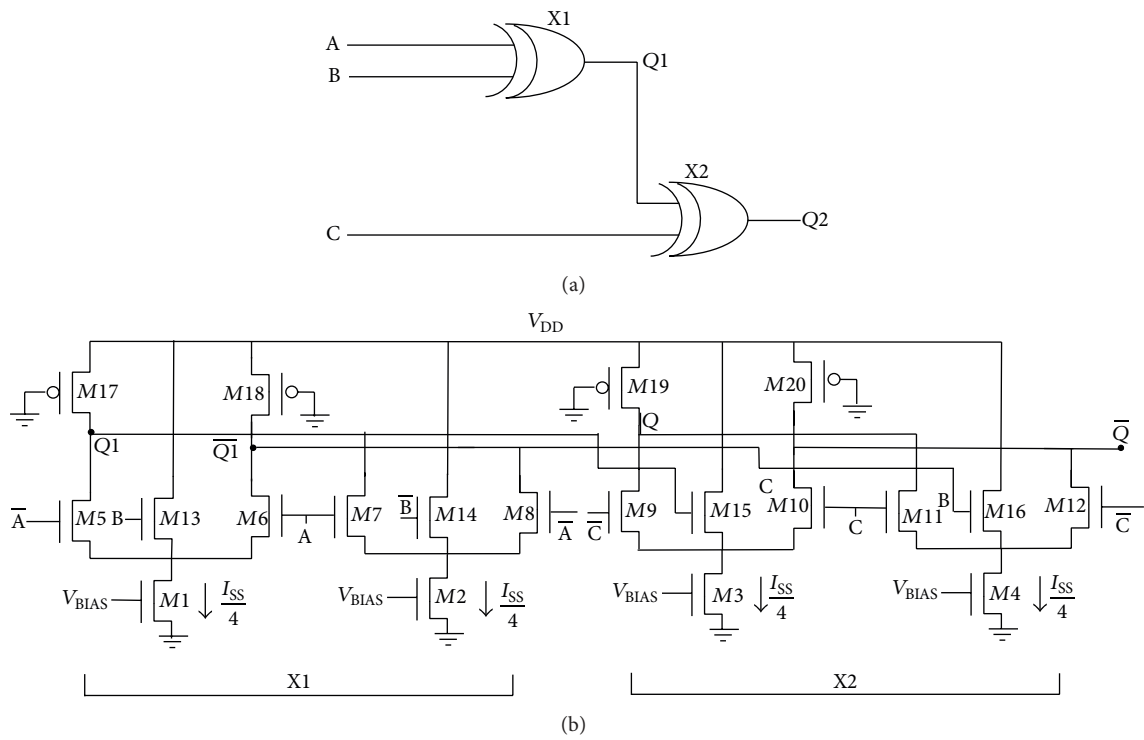| Parameter	Circuit				
	Conventional MCML	Topology 1	Topology 2	Proposed	CMOS CPL
Supply voltage (V_{DD})	1.7 V	1.1 V	1.4 V	1.1 V	1.0 V
Power consumption (μW)	170	110	140	110	44
Propagation delay (ps)	1178	1049	732	614	4017
Power delay product (fJ)	166.770	115.390	102.480	67.540	176.748
Gate count	1	2	1	1	1
Transistor count	17	20	18	22	18
Switching current (μA)	5	40	25	20	42

(a)

(b)

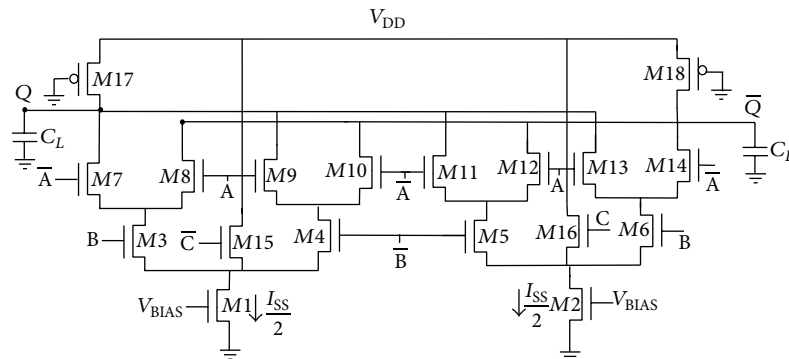FIGURE 5: Topology 1: (a) gate level schematic and (b) complete MOS schematic.

FIGURE 6: Complete MOS level schematic of Topology 2.

TABLE 2: Effect of process variation on propagation delay and voltage swing of three-input MCML XOR gate designs.

| XOR gate topology | NMOS | T | F | S | F | S |
	PMOS	T	F	S	S	F
Propagation delay (ps)						
Conventional		1178	976	1586	1091	1417
Topology 1		1049	971	1253	1071	1126
Topology 2		732	627	930	723	806
Proposed		614	430	664	659	661
Voltage swing (mV)						
Conventional		400	444	290	580	264
Topology 1		400	434	286	572	250
Topology 2		400	454	296	576	256
Proposed		400	424	298	550	216

FIGURE 7: Ring oscillator output by using proposed XOR gate.

gate, parasitic contribution in latter topology is higher than former one. This explains lowest delay of the proposed XOR gate topology among all.

(vii) All the MCML based XOR gate topologies produce less switching current in comparison to CMOS CPL based due to the presence of constant current source. The results thus confirm the preference of MCML based topologies in low noise mixed-signal environments over the CMOS based counterparts [5, 19].

(viii) The CMOS CPL based XOR gate consumes the lowest power but shows high delay and PDP values in comparison to all MCML based XOR gate topologies. Therefore, it is not considered further in the proposal.

To examine the sensitivity of different XOR realization performance towards process variation, the propagation delay and the voltage swing obtained through simulations are comprehended in Table 2. The variation between the best and worst case in the propagation delay is by a factor of 1.63, 1.29, 1.48, and 1.54, respectively, for conventional topology, Topologies 1 and 2, and the proposed one. Analogously, the corresponding factors for voltage swing are 2.19, 2.28, 2.25, and 2.54 for conventional topology, Topologies 1 and 2, and the proposed one. The voltage swing values should be more than $1.4 V_{\text{dssat}}$, where V_{dssat} is the saturation drain-source voltage of the differential transistor pair for functionality to remain intact [20]. It may further be noted that the proposed MCML gates can maintain constant voltage swing against process variation by modifying their load section by using adaptive bias controller as suggested in [21, 22].

The behavior of proposed XOR gate is also investigated by configuring it as an inverter and cascading five such inverters in a loop to obtain five-stage ring oscillator (RO). The timing waveform is shown in Figure 7. RO is also constructed with conventional XOR gate with similar connections. It also gives oscillations and timing waveform is similar to that of Figure 7 which is omitted for the sake of brevity. To verify the functionality of RO constructed with proposed and conventional topologies at all PVT corners, a number of simulations have been performed and the results are comprehended in Table 3. It can be observed that the oscillations are achieved at all
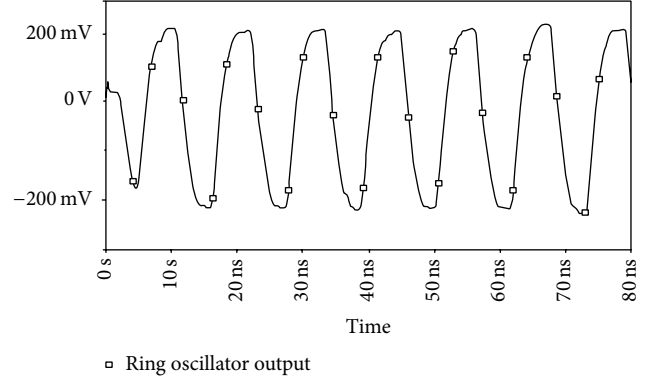
the process corners and the values exhibit the same trend as shown in Table 2 for individual gate simulation.

To compare the behavior of the proposed gate with conventional XOR gate under same parasitic contribution case, both gates are redesigned for this and five-stage ROs are constructed. The oscillation frequencies of 5.1 MHz and 71 MHz are observed for the proposed and the conventional topologies, respectively. The corresponding power consumption values are 550 μW and 850 μW for the proposed and the conventional topologies, respectively. These observations can be supported with the following discussion: the voltage swing, propagation delay, and the power are represented as $V_{\text{SWING\_X}}$, $t_{\text{PD\_X}}$, and P_{X}, where X corresponds to CON and PG for conventional and proposed topologies. Using first-order approximations, the values of $t_{\text{PD\_CON}}$ and $t_{\text{PD\_PG}}$ are computed, respectively, as

$$t_{\text{PD\_PG}} = 0.69 R_{\text{P}} \left(C_{\text{PC}} + C_{\text{Load}} \right),$$
$$t_{\text{PD\_CON}} = 0.69 R_{\text{P\_CON}} \left(C_{\text{PC}} + C_{\text{Load}} \right), \tag{14}$$

where $R_{\text{P\_CON}}$ and R_{P} refer to load resistances of conventional and proposed topologies and C_{Load} and C_{PC} represent load and parasitic capacitance, respectively.

The ratio of $t_{\text{PD\_PG}}$ and $t_{\text{PD\_CON}}$ is computed as

$$\frac{t_{\text{PD\_PG}}}{t_{\text{PD\_CON}}} = \frac{0.69 R_{\text{P}} \left(C_{\text{PC}} + C_{\text{Load}} \right)}{0.69 R_{\text{CON}} \left(C_{\text{PC}} + C_{\text{Load}} \right)} = \frac{R_{\text{P}}}{R_{\text{CON}}}. \tag{15}$$

Taking $N = 2$, this ratio is computed as 12 for $V_{\text{SWING\_CON}} = V_{\text{SWING\_PG}}$. The RO simulation gives value to this ratio as 13.78 giving error of about 15%. Further, as the topologies have been simulated with their respective minimum power supplies ($V_{\text{DD\_MIN\_PG}}$ and $V_{\text{DD\_MIN\_CON}}$), the ratio of power consumption is given by

$$\frac{P_{\text{PG}}}{P_{\text{CON}}} = \frac{V_{\text{DD\_MIN\_PG}} I_{\text{SS}}}{V_{\text{DD\_MIN\_CON}} I_{\text{SS}}} = \frac{V_{\text{DD\_MIN\_PG}}}{V_{\text{DD\_MIN\_CON}}}. \tag{16}$$

The theoretical and simulated values for this ratio are 0.64 and 0.66, respectively. The power efficient design needs the product of power and delay (PDP) to be calculated and a smaller value is indication of this measure [17]. The ratio of

TABLE 3: Oscillation frequency at different PVT corners.

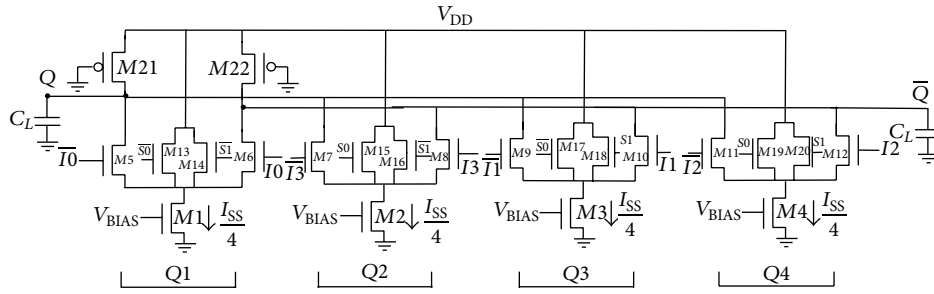| Topology	NMOS	T	F	S	F	S	T	T	T	T
	PMOS	T	F	S	S	F	T	T	T	T
	T (°C)	70	0	125	70	70	70	70	0	125
Conventional										
V_{DD} (V)		1.7	1.87	1.53	1.7	1.7	1.87	1.53	1.7	1.7
Freq. (MHz)		95	108	65	71	66	100	59	125	77
Proposed										
V_{DD} (V)		1.1	1.21	0.99	1.1	1.1	1.21	0.99	1.1	1.1
Freq. (MHz)		140	181	114	125	139	147	90	163	125

FIGURE 8: Multiplexer realization (4 : 1 MUX) based on the proposed approach.

PDP for proposed (PDP_{PG}) and conventional topologies is computed as

$$\frac{\text{PDP}_{\text{PG}}}{\text{PDP}_{\text{CON}}} = \frac{V_{\text{DD\_MIN\_PG}} I_{\text{SS}}}{V_{\text{DD\_MIN\_CON}} I_{\text{SS}}} \frac{0.69 R_{\text{P}} \left(C_{\text{PC}} + C_{\text{Load}} \right)}{0.69 R_{\text{CON}} \left(C_{\text{PC}} + C_{\text{Load}} \right)}$$
$$= \frac{V_{\text{DD\_MIN\_PG}}}{V_{\text{DD\_MIN\_CON}}} \frac{R_{\text{P}}}{R_{\text{CON}}}. \tag{17}$$

The theoretical and simulated values for this ratio are 7.68 and 9, respectively. Thus, the proposed topology is less power efficient if the parasitic contribution of the transistors in the two XOR gate topologies is made equal.

4.3. A Generalized Approach. The proposed quad-tail cell can be used to formulate a general design approach for logic function realization. Four numbers of quad-tail cells can be connected in a configuration given in Figure 8 to realize a 4 : 1 multiplexer. The input lines are marked as $I0$–$I3$, and select lines are denoted by $S0$ and $S1$. The four input lines ($I0$, $I1$, $I2$, and $I3$) form the input to the outer transistors of the quad-tail cells ($Q1$, $Q2$, $Q3$, and $Q4$), respectively, while select lines are tied to inner transistors according to the operation. The availability of the desired input line at the multiplexer output can be achieved by proper activation of the quad-tail cell through select lines $S0$ and $S1$. For instance, the data on the input line $I1$ can be made available at the output of the multiplexer for low and high values of $S0$ and $S1$, respectively. It is well known that any three-input logic function can be implemented using 4 : 1 MUX so the circuit of Figure 8 can practically realize $(2^3)^2$ logic functions. The mapping table for $I0$–$I3$ and $S1$-$S0$ is omitted for the sake of brevity.

5. Conclusion

A new proposal for three-input logic function realization in MCML style is presented. The new proposal reduces the number of stacked source-coupled transistor levels in the logic function realization. A circuit element named quad-tail cell is presented for this purpose and its use in the implementation of three-input exclusive-OR (XOR) gate is elaborated. Its behavior is analyzed and SPICE simulations using TSMC 180 nm CMOS technology parameters are included to support the theoretical concept. The performance of the proposed circuit is compared with the conventional XOR topology along with two more triple-tail cell based topologies. Comparison with CMOS complementary pass transistor logic based XOR gate is also included for the sake of completeness. The performance of all XOR gate realizations is compared and it is found that the proposed XOR gate topology performs best in terms of most of the performance parameters. The sensitivity of different MCML XOR gate realization performance is examined towards process variation which indicates similar values. A discussion on the realization of three-input logic by configuration of a 4 : 1 multiplexer has also been included as an extension of the work.

Competing Interests

The authors declare that they have no competing interests.

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