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New Salicidation Technology With Ni(Pt) Alloy for MOSFETs

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***Abstract*—A novel salicide technology to improve the thermal stability of the conventional Ni silicide has been developed by employing Ni(Pt) alloy salicidation. This technique provides an effective avenue to overcome the low thermal budget (<700 °C) of the conventional Ni salicidation by forming Ni(Pt)Si. The addition of Pt has enhanced the thermal stability of NiSi. Improved sheet resistance of the salicided narrow poly-Si and active lines was achieved up to 750 °C and 700 °C for as-deposited Ni(Pt) thickness of 30 nm and 15 nm, respectively. This successfully extends the rapid thermal processing (RTP) window by delaying the nucleation of $NiSi_2$ and agglomeration. Implementation of Ni(Pt) alloyed silicidation was demonstrated on PMOSFETs with high drive current and low junction leakage.**

***Index Terms*—Ni(Pt)Si, NiSi, salicidation.**

I. Introduction

CURRENTLY, the self-aligned silicide (salicide) process is widely used to lower the gate resistance (and therefore RC delay), to reduce the source/drain parasitic resistance, and increase the drive current of MOS transistors. Scaling of the VLSI technology has caused $TiSi_2$ to encounter incomplete phase transformation from C49 to C54 phase, resulting in higher sheet resistance on very narrow lines. $CoSi_2$ is currently being used due to the absence of sheet resistance degradation on deep submicron lines. However, high Si consumption and junction spiking may limit its applications. NiSi is a silicide material which is of much interest due to the low temperature one step annealing, lower Si consumption, and low sheet resistance which shows no linewidth dependence. Nevertheless, NiSi has been reported to agglomerate at temperatures as low as 600 °C [1], [2] and phase transformation to the high resistivity $NiSi_2$ occurs at temperatures of 750 °C and above [3]. Recently, we have reported the enhanced thermal stability of NiSi by alloying with Pt [4]. In this letter, we report on the implementation of Ni(Pt) alloyed silicide onto device structures to realize the potential of Ni(Pt) alloy silicides in achieving a larger processing window for future silicidation applications. The improved electrical performance of the Ni(Pt) alloyed salicide scheme is reported for PMOSFETs.

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II. Experiment

After the growth of a 6.5-nm gate oxide on (100)-p-type Si substrate, 255-nm poly-Si was deposited using LPCVD. This is followed by gate patterning and source/drain formation. The n^+ and p^+ dopings were carried out by As implant of 2×10^{15} cm^{-2}, 50 keV, and BF_2 implant of 2×10^{15} cm^{-2}, 40 keV, respectively. After thermal activation of the dopants, pure Ni and Ni(Pt) films of thickness 30 nm were sputter deposited on narrow width structures (ranging from 1 μm to 0.23 μm) after a dilute HF dip. In addition, 15 nm of Ni(Pt) was sputtered and salicided on patterned wafers optimized for 0.13 μm technology with sub-0.18 μm structures. The amount of Pt in the alloy is about 5 atomic % from the measurements using RBS (Rutherford Backscattering). Silicidation was carried out at 500 to 800 °C by rapid thermal annealing in N_2 ambient. Unreacted metal was removed using $H_2SO_4 : H_2O_2$ etchants. Sheet resistance of pure Ni and Ni(Pt) salicided poly-Si and active regions was measured as a function of linewidths using Kelvin structures. Electrical characterization was performed on PMOSFETs after salicidation.

III. Results and Discussion

Fig. 1(a) compares the sheet resistance of Ni and Ni(Pt) salicided poly-Si lines as a function of linewidth after various silicidation temperatures. The sheet resistance of the 30 nm Ni and Ni(Pt) salicided poly-Si lines is low and uniform at low silicidation temperature of 500 °C. However, at a higher silicidation temperature of 700 °C, the sheet resistance starts to degrade on the pure Ni salicided narrow poly-Si lines due to agglomeration. On the other hand, the Ni(Pt) salicided poly-Si lines do not exhibit degradation at 700 °C. There is only a small increment in the sheet resistance on the Ni(Pt) salicided lines at 750 °C, above which severe degradation began to start. This is due to the effect of agglomeration, which has detrimental effects on narrow lines. The formation of Ni(Pt)Si at silicidation temperatures above 750 °C has been shown using micro-Raman spectroscopy on these poly-Si lines [5]. Fig. 1(b) shows the sheet resistance of the 15 nm Ni(Pt) on sub-0.18 μm n^+ poly-Si lines. The sheet resistance starts to degrade at 700 °C due to agglomeration. For pure Ni with thickness of 15 nm, the sheet resistance degradation occurs at 600 °C (not shown), in accordance to the results reported by Das *et al.* [1] and Xu *et al.* [2]. The sheet resistance of Ni(Pt)Si at 700 °C is still five to six times lower than that of silicides formed using 15-nm pure Ni ($\sim 100 \Omega/sq$) in [6]. The Ni(Pt)Si

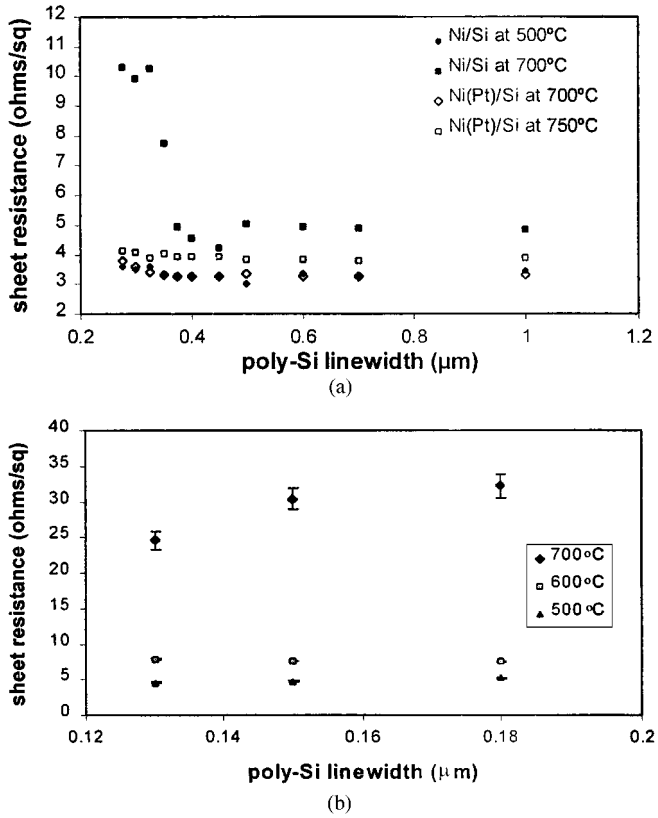

Fig. 1. (a) Sheet resistance of 30 nm of Ni and Ni(Pt) salicided poly-Si as a function of poly-Si linewidth at various salicidation temperatures. (b) Sheet resistance of 15 nm of Ni(Pt) salicided poly-Si lines of sub-0.18 μm at various salicidation temperatures.

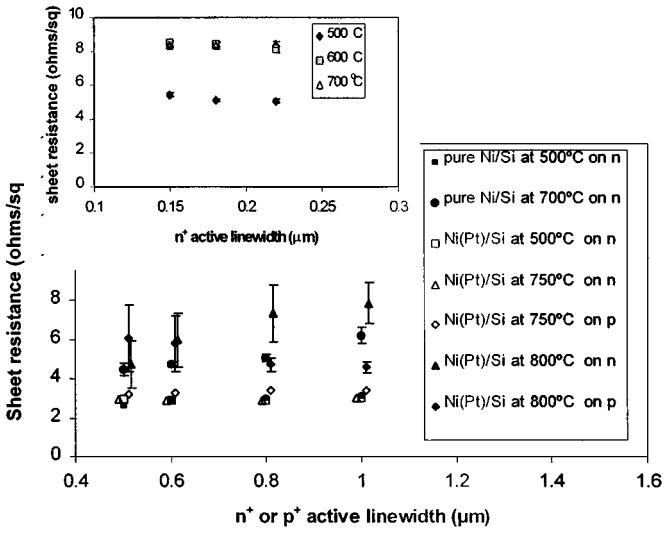

Fig. 2. Sheet resistance of Ni and Ni(Pt) salicided n^+ and p^+ active regions as a function of active linewidth at various salicidation temperatures. Insert plot shows the active resistance of 15 nm of Ni(Pt) on sub-0.25 μm narrow n^+ active lines.

salicided poly-Si lines has retarded agglomeration to a higher temperature than that of pure NiSi when compared at a silicidation temperature of 600–700 °C.

Fig. 2 shows the 30-nm Ni and Ni(Pt) salicided active sheet resistance of various active linewidths at different salicidation temperatures. The Ni(Pt)Si shows low sheet resistance even up

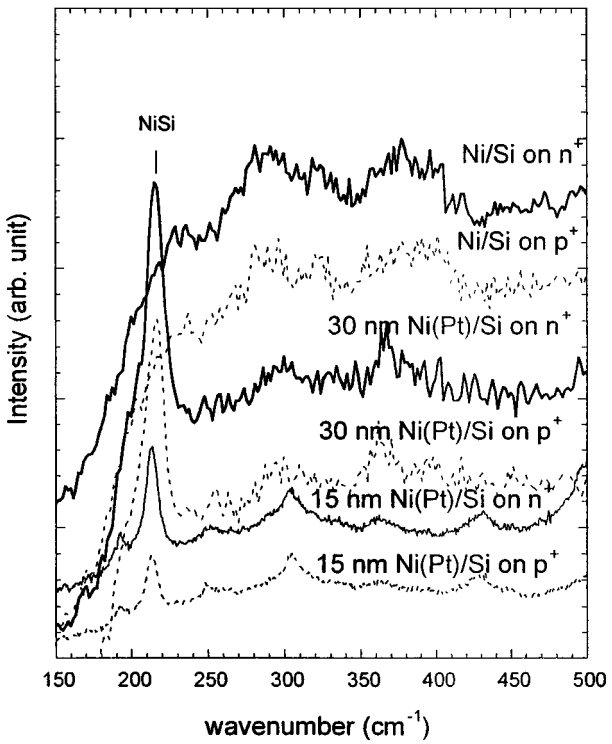

Fig. 3. Micro-Raman spectroscopy on n^+ and p^+ salicided device active regions using Ni and Ni(Pt) at 800 °C.

to annealing temperature of 750 °C on both n^+ and p^+ active lines. Agglomeration started to occur at 800 °C, which is higher than that of pure Ni silicides. Low sheet resistance was also demonstrated using the 15-nm Ni(Pt) on sub-0.25 μm n^+ active lines up to 700 °C as shown in the inserted plot. The phase formation on the n^+ and p^+ active regions was studied using micro-Raman as shown in Fig. 3. A strong Raman peak at 215 cm^{-1} was observed on both n^+ and p^+ active after annealing at temperatures of 800 °C, corroborating the enhanced stability of Ni(Pt)Si even with 15-nm thin Ni(Pt) [7]. On pure Ni salicided active regions, absence of the NiSi Raman peak at 800 °C is due to the formation of $NiSi_2$. It was previously claimed that $NiSi_2$ forms at low temperatures ($\sim$600 °C) especially on the active regions with thin Ni film [2]. The conclusion was drawn merely from the sheet resistance data without phase analysis. This deduction may have neglected the effect of agglomeration on the sheet resistance degradation, especially thin NiSi can agglomeration at such low temperatures. Despite this, we have demonstrated that the addition of Pt has delayed the $NiSi_2$ nucleation on both narrow poly-Si and active regions even for 15-nm thin Ni(Pt) film.

The formation of $NiSi_2$ occurs through a nucleation-controlled process. Nucleation controlled reactions occurred when the change in free energy (ΔG) of a reaction (NiSi + Si $\rightarrow$ $NiSi_2$) can hardly balance the increase in interfacial energy associated with the creation of new phase ($\Delta\sigma = \sigma$ $NiSi_2$/Si $+\sigma$ $NiSi_2$/NiSi $-\sigma$ NiSi/Si). The activation energy for nucleation, $\Delta G*$ is related to $\Delta\sigma^3/\Delta G^2$ during the reaction of NiSi + Si $\rightarrow$ $NiSi_2$. The addition of alloying element may influence both $\Delta\sigma$ and ΔG. A decrease in the free energy (ΔG) term is due to the formation of a pseudobinary silicide solution

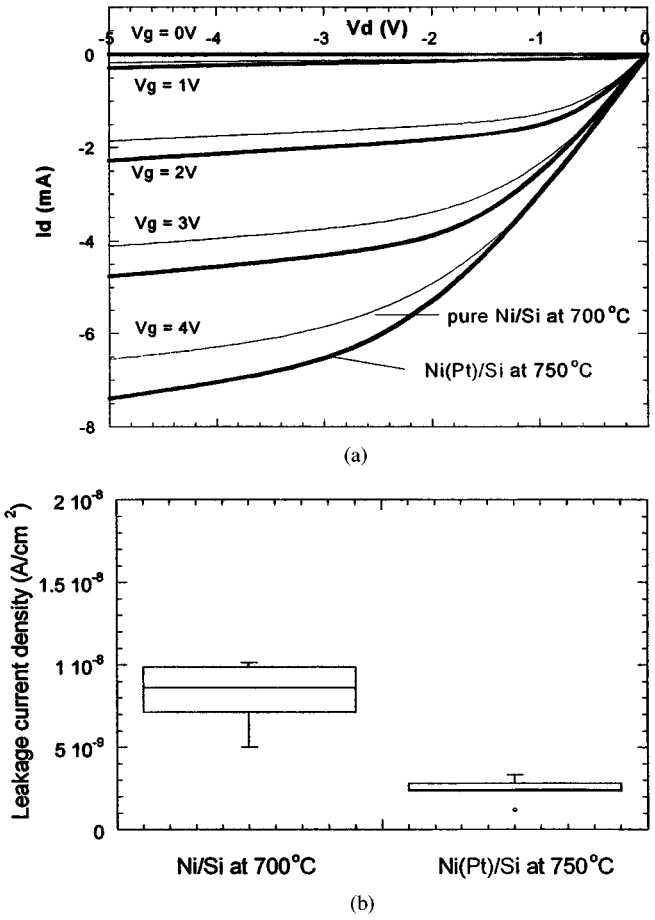

Fig. 4. (a)I_d–V_d characteristics for 0.35 μm PMOS transistors with Ni monosilicide salicidation using Ni- and Ni(Pt) at 700 °C and 750 °C, respectively. (b) Leakage current density for Ni- and Ni(Pt)-salicided junctions at 700 ° and 750 °C, respectively.

Ni(Pt)Si which has a lower free energy (NiSi and PtSi are both orthorhombic silicides). The strong tendency of Ni(Pt)Si to be in texture on Si(100) was ascribed to lower the interfacial energy of Ni(Pt)Si on Si and therefore increases the $\Delta\sigma$ [4], [8].

The Ni(Pt) salicidation scheme was integrated onto PMOSFETs. Fig. 4(a) shows the I_d–V_d characteristics of a 0.35 μm gate length and 25 μm width PMOSFET after salicidation using pure Ni at 700 °C and compared to Ni(Pt) salicidation at 750 °C. Both devices with monosilicide have similar V_{th}. The higher drain current of the device with Ni(Pt)Si is due to the lower sheet resistance of the source and drain region. Fig. 4(b) compares the p^+/n junction leakage current density at reverse bias of 3.6 V at high silicidation temperatures. At 700 °C anneal for pure Ni-salicided junctions, the leakage current density is higher and has a wider distribution than that of Ni(Pt) salicided junctions at 750 °C. The mechanism of p^+/n junction degradation for pure NiSi at 700 °C has been attributed to the formation of some small area Schottky contacts arising from silicide spikes [9]. This provides evidence of the enhanced stability of Ni(Pt)Si with the addition of Pt.

IV. Conclusion

Ni(Pt) alloy silicide was demonstrated to improve the stability Ni(Pt)Si by delaying the $NiSi_2$ nucleation and agglomeration. PMOSFETs have shown improved drive current at high silicidation temperature of 750 °C when compared to pure Ni–salicide anneal at 700 °C. Low junction leakage can be achieved on Ni(Pt)Si junctions even at high processing temperatures. The Ni(Pt) alloy salicidation scheme has been introduced for CMOS applications, the large salicide processing window revealed its great potential for implementation onto a newly merged device (e.g., logic and DRAM) which requires large thermal budget.

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